TOF Electronics PED Request

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Rationale

- TOF needs a very low jitter EIC clock (~5 ps jitter)
  - *but not only TOF* ⇒ Roman Pots, LAPPD based detectors
- TOF's ASIC needs evaluation boards which can interface to the EICROC ASIC
  - *but not only TOF* ⇒ all detectors with ASICs
- TOF also needs a prototyping platform for its RDO & streaming DAQ evolution
  - *but not only TOF* ⇒ *all* detectors
- Since these requests span more than TOF it was decided that the corresponding PED will be submitted through the DAQ Working Group

Status

- a list of required FPGA development kits was discussed within the DAQ WG and the request was submitted to the Project
- BNL (for TOF but *also for potential other detectors*) will receive
  - 2x FPGA Development Kits (Xilinx ZCU106, Ultrascale+ family)
- this will enable TOF to
  - attach the EICROCx ASICs via the FMC connector for evaluation, streaming techniques, etc
    - note that a very similar board is already in use but with an older Xilinx FPGA
  - develop and measure various clock distribution schemes using what we expect will be the “final” RDO FPGA (a Xilinx Ultrascale+ family device)
    - one board acts as a transmitter (ala e.g. FELIX) the other board acts like the clock receiver and subsequent interface to the ASIC clocks (an RDO prototype)
  - develop & evaluate streaming protocols and primitives
    - one board acts as an RDO prototype (“sender”) while the other board acts like a FELIX protoype (“receiver”), both connected via the proposed high rate fiber links

Summary

- the boards are on their way, I quote Jeff from Mar 30:
  - *Orders are out, thanks to Dave Abbot & Jo Schambach*
  - *Clock and timing modules to come in this week or next, 8 week timeline on the FPGA board delivery (Late May)*
- however, we are lacking engineering support for the development of the required firmware as well as the various timing mechanism measurements