TOF Electronics PED Request

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Rationale

- TOF needs a very low jitter EIC clock (~5 ps jitter)
  - *but not only TOF* ⇒ Roman Pots, LAPPD based detectors
  - other detectors also need a way to transmit the clock although without such stringent requirements
- TOF's ASIC needs evaluation boards which can interface to the EICROC ASIC
  - *but not only TOF* ⇒ all detectors with ASICs
- TOF also needs a prototyping platform for its RDO & streaming DAQ evolution
  - *but not only TOF* ⇒ *all* detectors
- ⇒ Since these requests span more than just TOF it was decided that the corresponding PED will be submitted through the DAQ Working Group

Status

- a list of required FPGA development kits was discussed within the DAQ WG and the request was submitted to the Project & approved
- Quoting Jeff from Mar 30
  - *Orders are out, thanks to Dave Abbot & Jo Schambach*
  - *Clock and timing modules to come in this week or next, 8 week timeline on the FPGA board delivery (Late May)*
- TOF (at BNL) will receive
  - 2x FPGA Development Kits (Xilinx ZCU106, Ultrascale+ family)
  - 1x Silicon Labs clock evaluation board Si5394A-EVB

Goals

1. develop and *measure* various clock distribution schemes using what we expect will be the “final” RDO FPGA (a Xilinx Ultrascale+ family device)
   a. one board acts as a transmitter (ala e.g. FELIX), the other board acts like the clock receiver and subsequent interface to the ASIC clocks (an RDO prototype)
   b. effort will mostly be covered by other groups and people who expressed interest within the DAQ WG
      i. William (JLab), Marius (Wuppertal), Jo (ORNL), Pietro et al (Bologna)
      ii. however, this will take more time than originally expected (end of year?)
   c. this is a critical item for TOF (as well as all detectors)
      i. TOF itself is lacking engineering resources to contribute to this effort
2. attach the EICROCx ASICs via the FMC connector for evaluation, streaming techniques, etc
   a. note that a very similar board is already in use but with an older Xilinx FPGA (Prashanth, et al)
   b. EICROC designers have signalled a lack of resources at the moment
      i. TOF is lacking engineering resources for this (critical) effort
3. develop & evaluate streaming protocols and primitives
   a. one board acts as an RDO prototype (“sender”) while the other board acts like a FELIX protoype (“receiver”), both connected via the proposed high rate fiber links
   b. lower priority at this stage but needs to start & continue in subsequent months/years