

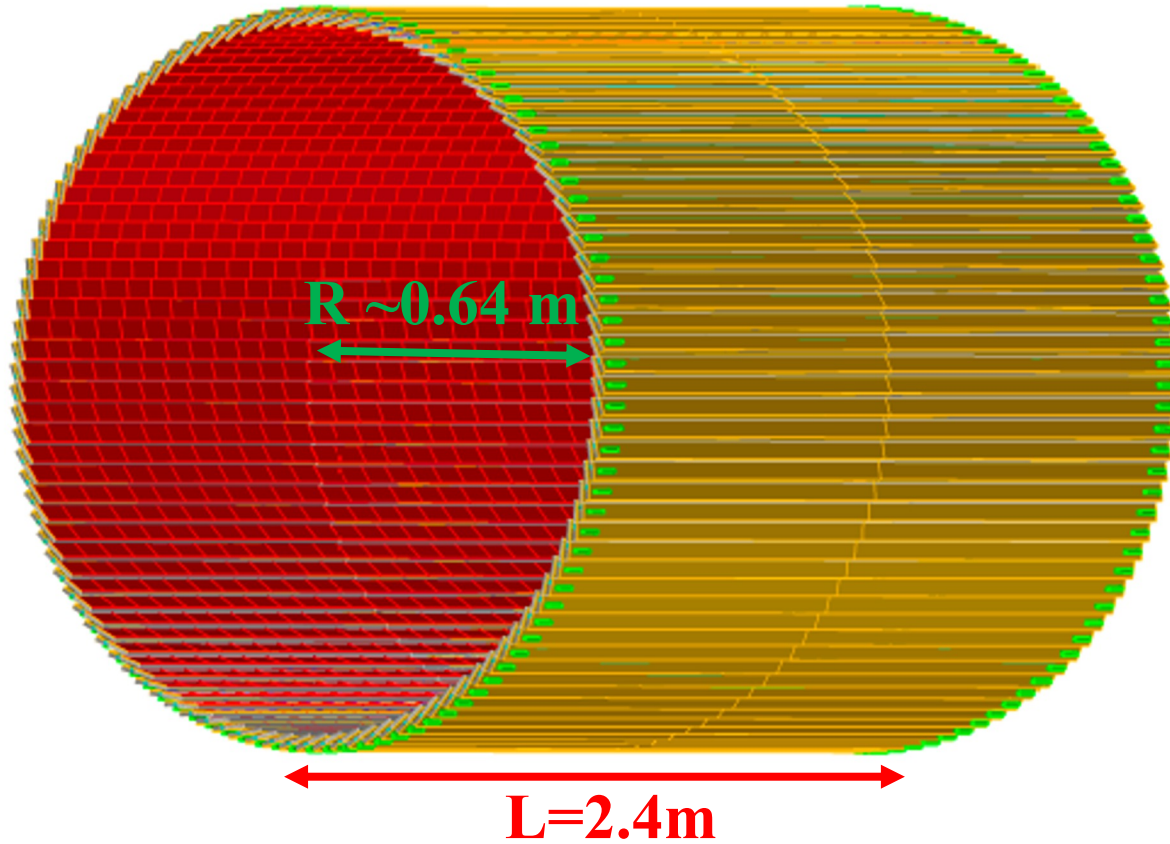
# ePIC TOF DWG -> ePIC TOF DSC

- **ePIC AC-LGAD TOF Detector System**
  - Barrel: 1 cm\*500 um strips, ~10 m<sup>2</sup>, ~2M channels
  - Forward: 500\*500 um<sup>2</sup> pixels, ~1.4 m<sup>2</sup>, ~6M channels
- **TOF Detector Working Group**
  - Convener: Constantin Loizides (ORNL), Frank Geurts (Rice), Wei Li (Rice), Zhenyu Ye (UIC)
  - DAQ contact: Tonko Ljubicic (BNL)
  - Simulation contact: Nicholas Schmidt (ORNL)
  - LGAD consortium, eRD109 (ASIC & Electronics), eRD112 (Sensor & Mechanics)
- **TOF Detector Subsystem Collaboration**
  - **Nominated for DSL and Deputy DSL:** Zhenyu Ye (UIC), Satoshi Yano (Hiroshima University)
  - **In the process of collecting institutional interests/responsibilities and defining working groups/packages**
  - **Institutions:**
    - **USA:** Brookhaven National Laboratory, Los Alamos National Laboratory, Oak Ridge National Laboratory, Ohio State University, Purdue University, Rice University, University of California Santa Cruz, University of Illinois at Chicago
    - **Japan:** Hiroshima University, RIKEN, Shinshu University, University of Tokyo
    - **India:** IIT Mandi, National Institute of Science Education and Research
    - **Taiwan:** National Central University, National Cheng Kung University, National Taiwan University
    - **China:** South China Normal University, University of Science and Technology of China
    - ...

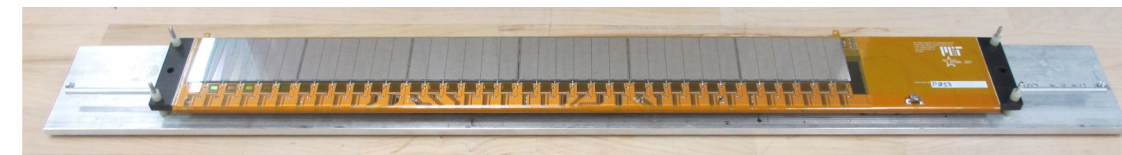
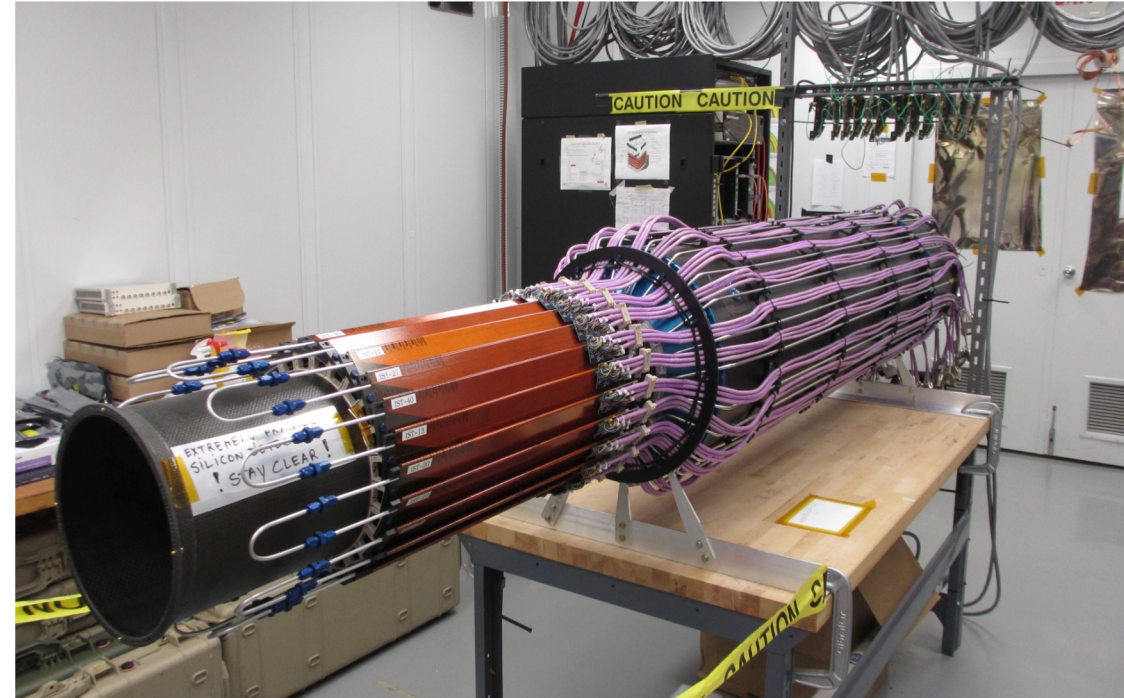
# Barrel TOF Layout

More details: <https://indico.bnl.gov/event/16765/>

ePIC Barrel TOF ( $\sim 1\% X_0$ )



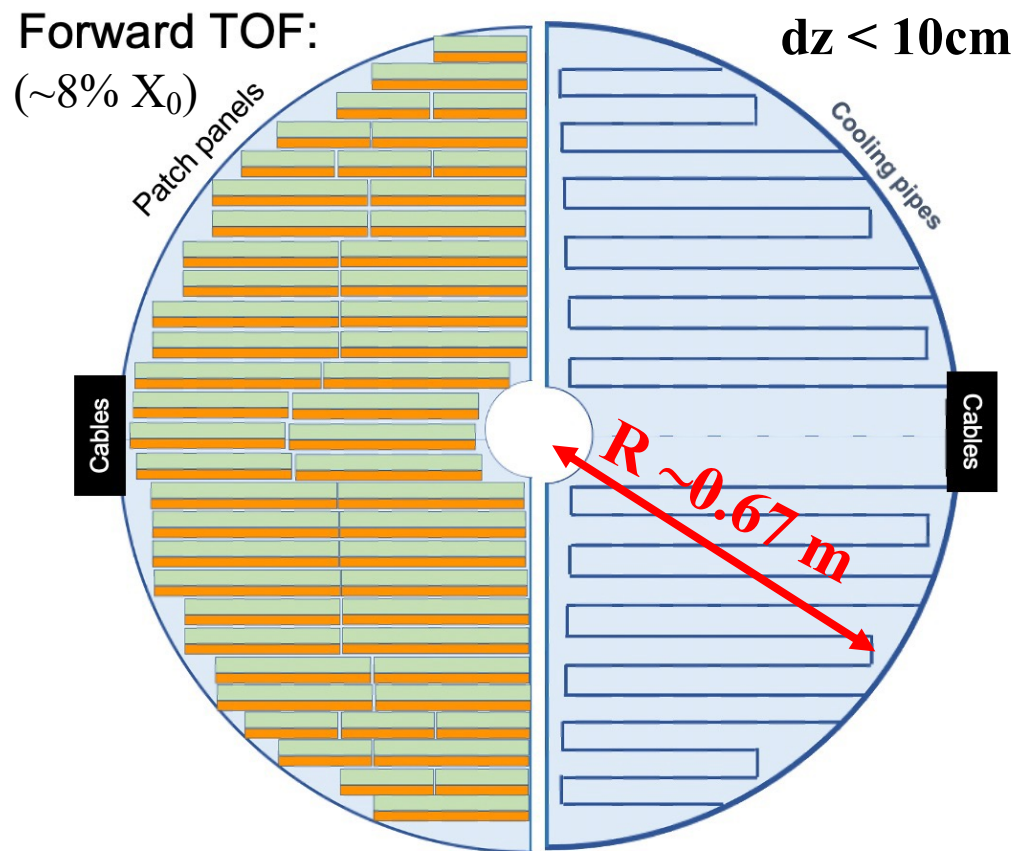
## STAR Intermediate Silicon Tracker



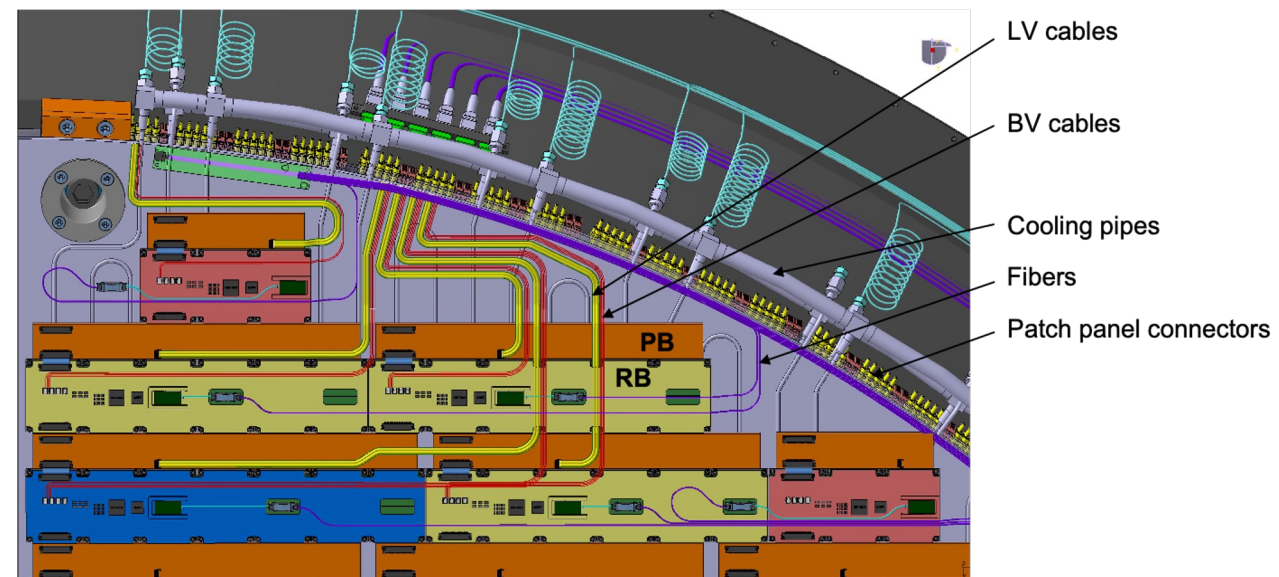
- 288 staves, each with 32 strip sensors wire-bonded to 64 frontend ASICs on low mass Kapton flex and CF support
- Power consumption:  $\sim 4 \text{ kW}$  for  $500\mu\text{m} \times 1\text{cm}$  strips ( $2.4 \text{ kW}$  for ASIC,  $1.0 \text{ kW}$  for DC-DC,  $0.6 \text{ kW}$  for sensor+cable+RB)

# Forward TOF Layout

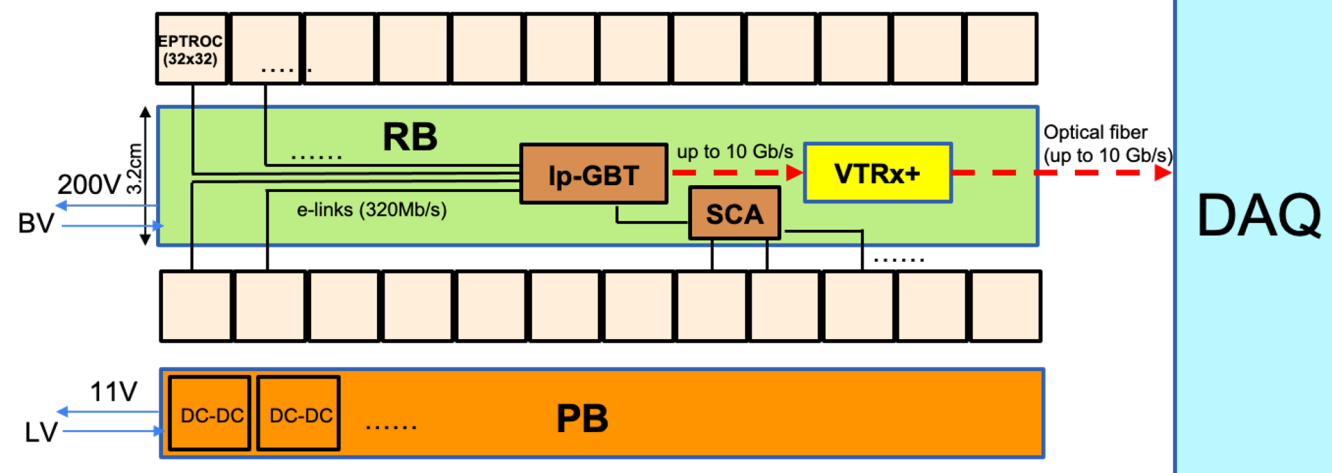
More details: <https://indico.bnl.gov/event/17336/>



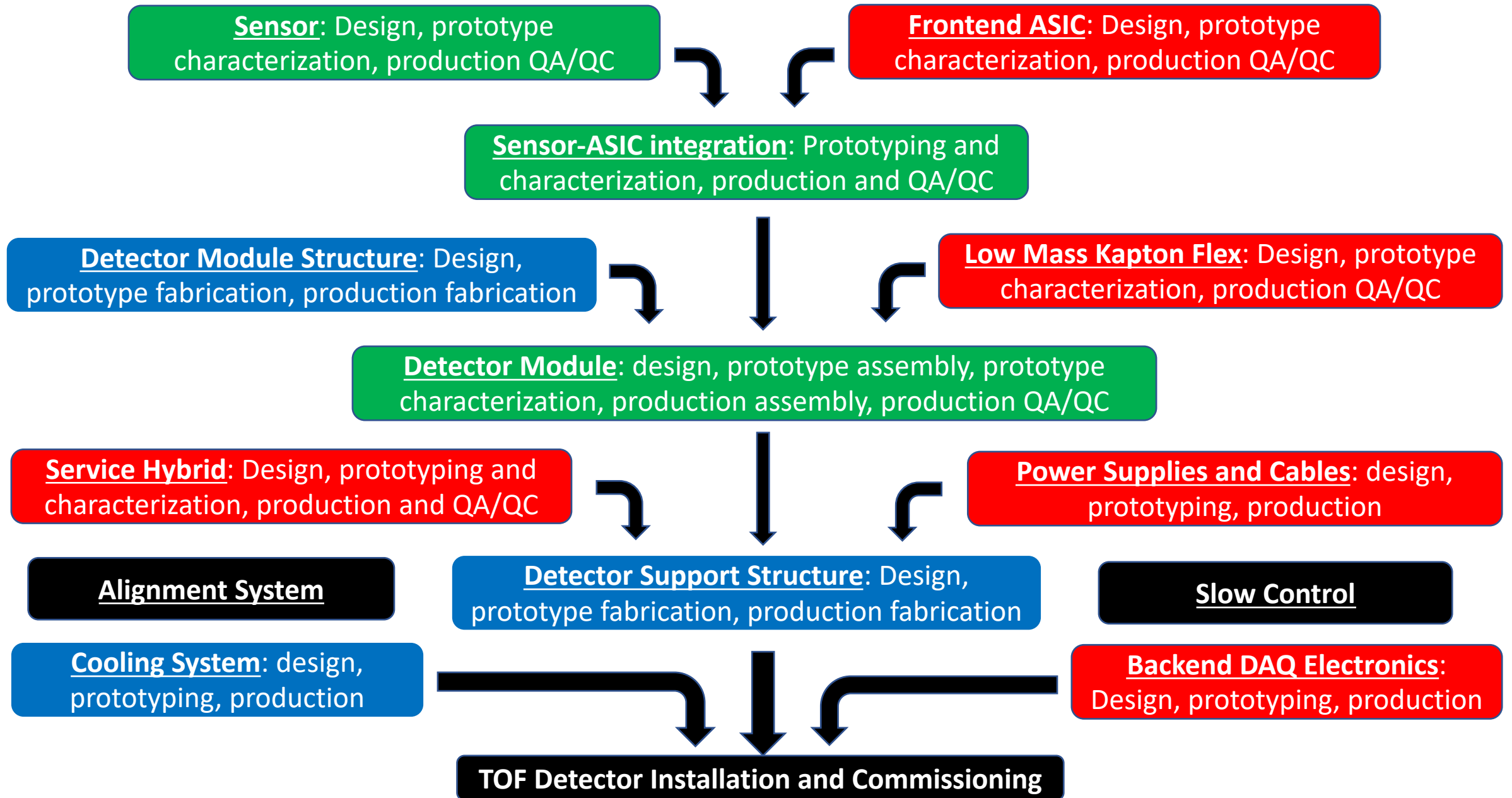
## CMS Endcap Timing Layer



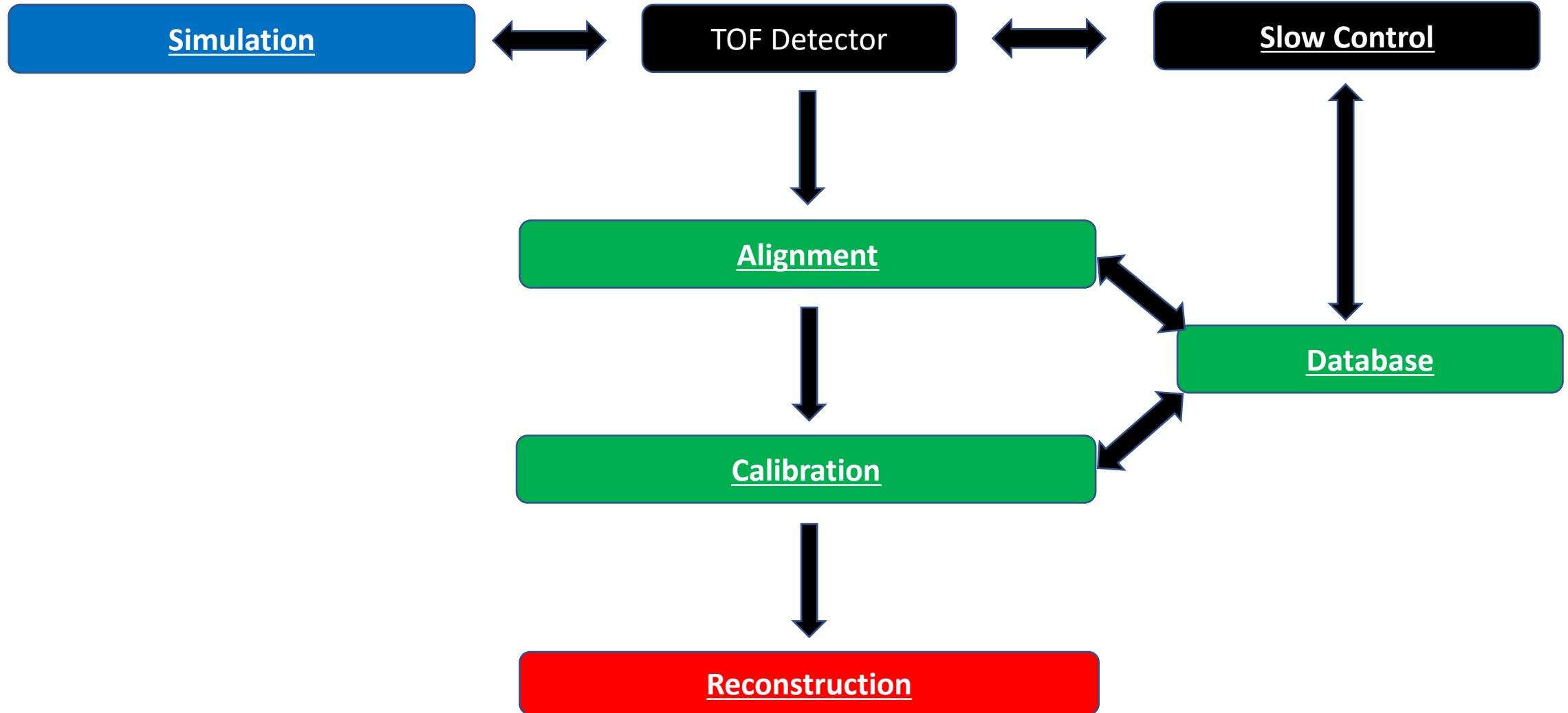
- 212 modules, each with 24 to 96 bump-bonded pixel sensor + ASIC assemblies on Al disk
- Power consumption: 13 kW for  $500 \times 500\ \mu\text{m}^2$  pixels (6 kW for  $800 \times 800\ \mu\text{m}^2$ )



# TOF Detector - Hardware



# TOF Detector - Software



# TOF On-going/Planned Work

[1] <https://wiki.bnl.gov/EPIC/index.php?title=TOFPID>

[2] <https://www.overleaf.com/read/vftxyvjtrvp>

[3] <https://wiki.bnl.gov/conferences/index.php/ProjectRandDFY23>

## Simulation [1]

- DD4HEP geometry, digitization, reconstruction (**ORNL, UIC, Hiroshima, BNL, OSU**)
  - Timing resolution requirement
  - Spatial resolution requirement
  - Material budget requirement

## Project Engineering and Design (PED) [2]

- Mechanical engineering (**NCKU/Purdue, ORNL**)
  - Mechanical support and services
  - Cooling system
- Electric engineering (**BNL within DAQ WG**)
  - Precision clock distribution (<5 ps)
  - Timing chips and streaming readout
  - Readout board

## eRD112 [3]

- Sensor (**BNL-IO, UCSC, UIC/Fermilab, LANL, ORNL, Rice**)
  - BNL-IO, HPK and FBK productions
  - Lab/beam test, irradiation
- Sensor-ASIC integration (**UIC**)
- Module mechanical structure (**NCKU/Purdue**)
  - Low-density composite structure

## eRD109 [3]

- Frontend ASIC:
  - EICROC (**IJCLab/OMEGA, BNL**)
  - FCFD (**Fermilab**)
  - Fast/HPSoC/ASROC (**UCSC**)
- Frontend electronics
  - Low-mass flexible Kapton PCB (**ORNL**)
  - Barrel TOF service hybrid (**ORNL**)
  - Endcap TOF service hybrid (**Rice**)

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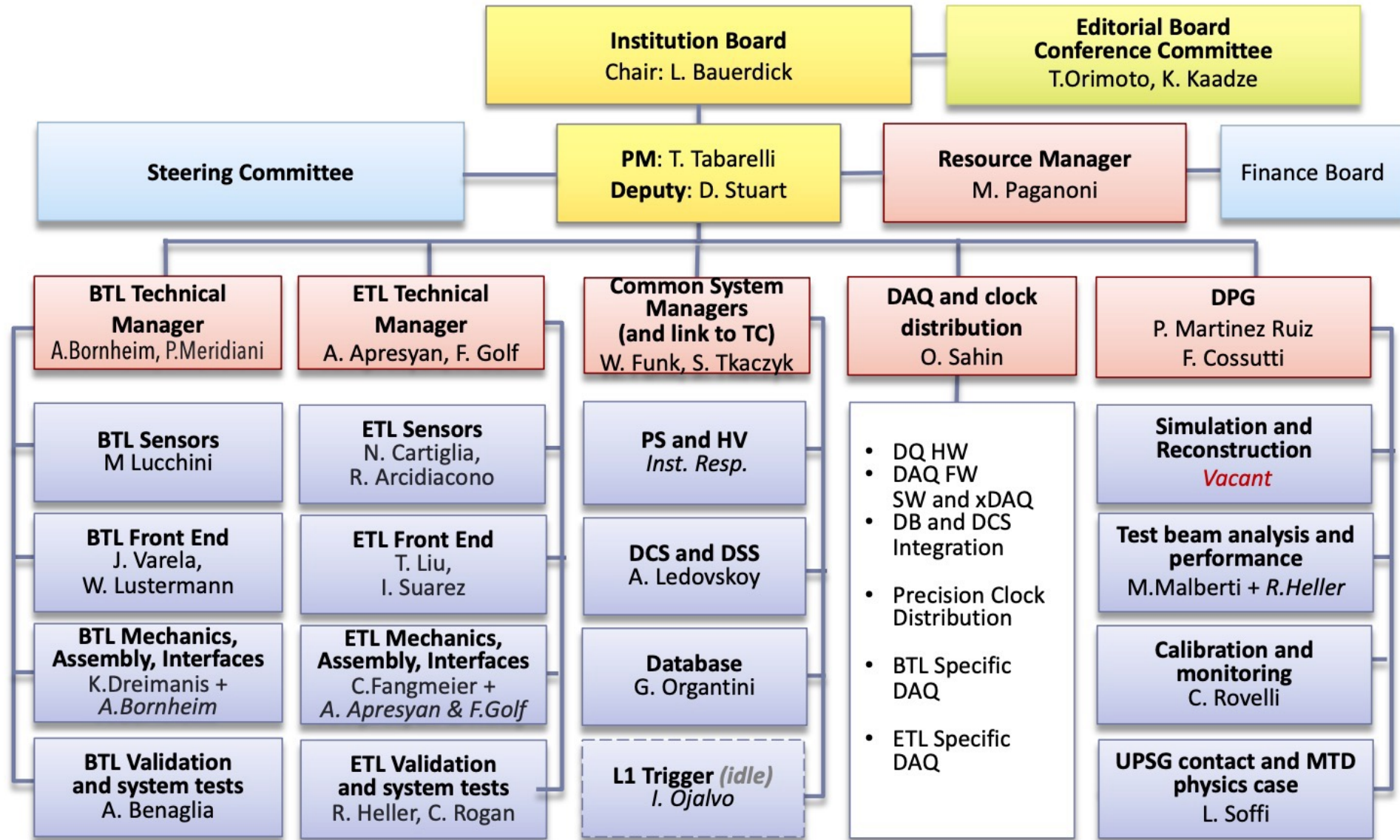
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# Inquiry for Institutions

	A	C	D	E	F	G	H	I	J
1	Institution	TOF & Tracking	Detector Simulation	AC-LGAD Sensor	Frontend ASIC	Mechanical and Cooling	On/Off-detector Electronics	Others	Resources
2	BNL (A. Tricoli)	Yes		Yes	Testing		There is interest in the group to help with the overall architecture and off-detector electronics, e.g. FELIX		2 scientists, 1 and 1/2 postdoc, 1 tech. There is interest from other people, i.e. another scientist and a professional
3	SCIPP/UCSC (B. Schumm)			We are tuning TCAD simulations to be used for sensor design and optimization. We are also performing extensive characterization studies of contemporary prototypes.	We are working with two private firms, under SBIR contracts, to develop two approaches to front-end readout, including CMOS and SiGe. These developments are geared towards improved temporal resolution and low power consumption.		Waveform digitization is included in one of the ASIC projects		Ongoing part-time contributions from two faculty, three postdocs, two senior staff
4	LANL (X. Li)	Yes		Yes. We have established test bench in lab for AC-LGAD characterization. The studies include single sensor and telescope testing with a 90Sr source. We also plan to carry out irradiation tests at the LANL LANSCE facility and a research reactor in UT Austin.	Testing		We could help on the integration and testing.		2 scientists, 1 postdoc to work on this part time, 1 mechanical engineer could provide engineer support.
5	NCKU (Y. Yang)	Yes		Testing.		Yes			
6	ORNL (C.Loizides, F.Bock, K.Read, Oskar Hartbrich)		Yes, including access to computing resources	Testing and characterization. Electronics laboratory with test benches available.	Possible engineering support, with limited availability of experienced ASIC design engineer, depending on funding.	Yes, depending on funding	Yes.		~3 (technical) scientists. Mechanical and electrical engineers available depending on support obtained/identified. Electronics laboratory with test equipment and testing space available.
7	Rice (W. Li, F. Geurts)	Yes	Yes	Yes. sensor testing and characterization			Yes. Specifically, we are interested in service hybrids (readout boards, power boards) leveraging expertise in CMS ETL		2 physicists and 1 postdoc plus part-time contributions from students
8	UIC (Z. Ye, O. Evdokimov)	Yes	Yes	TCAD simulation. Sensor characterization	Possible ASIC designer depending on funding. Testing (extensive experience with CMS ETROC)		off-detector readout electronics leveraging expertise in CMS ETL		part-time contributions from 2 physics faculties, 1 postdoc and 2 PhD students, possible engineering support from ASIC designer, electronics engineer and mechanical technicians with funding
9	NISER, India (Bedaga and Ganesh)	Yes	Yes	Yes. Sensor testing and characterization	ASIC qualification studies	Yes, depending on funding	In-kind contribution in system commissioning and detector integration	data analysis of test beam experiments.	2 Scientist (Ganesh - hardware and Mriganka- physics simulations), 1 electronics engineer (Kirti prasad sharma), 1 electronics (Deepak kumar), 1 mechanical assistant (Debasis barik), and 1 Technician (Subhash)
									We have a cleanroom, labs, equipments, and manpower for



# CMS MIP Timing Detector



Snapshot 2021, July 1st

# Possible Working Group Structure for TOF DSC?

- **Barrel TOF**
  - **Sensor:** sensor, sensor-ASIC integration
  - **Frontend electronics:** ASIC, service hybrid
  - **Detector Module:** module structure, module assembly
- **Forward TOF**
  - **Sensor:** sensor, sensor-ASIC integration
  - **Frontend electronics:** ASIC, service hybrid
  - **Detector Module:** module structure, module assembly
- **Common systems**
  - **Backend Electronics:** power supplies, DAQ system
  - **Mechanics:** support structure, cooling system
  - **Alignment system**
  - **Slow control**
- **Detector Performance**
  - **Simulation and reconstruction**
  - **Database**