

# ROC SlowControl FPGA

NWU Mai Kano

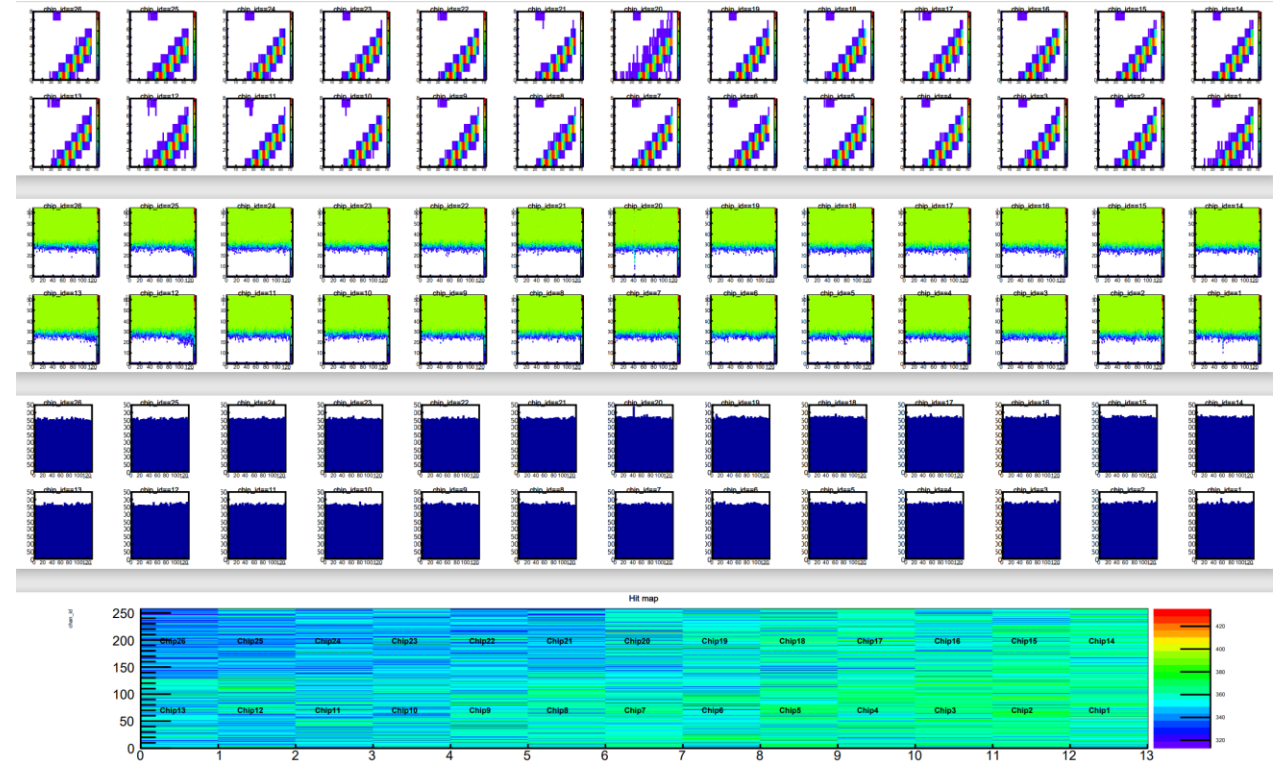
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INTT MT

# ROC    SlowControl FPGA

- There is a problem with Readbacker not working properly in a setup with Bus-Extender. We know the cause is in the ROC, and our goal is to modify the SlowControl FPGA that is sending and receiving Readback data in the ROC.
- I was looking for the ROC code that is used now, which is the original code for the modification.
- Status so far
  - None of the files on the FVTX web site didn't pass the "Verify". Verify is passed when the file written in the ROC and the file selected on the computer are completely matched.
  - I have tried actually writing those code in the ROC, but could not get them to calibrate.

- So I Verified some files found on a PC that was used in FVTX in the past and found a file that passes Verify.
- After writing this code into the ROC, we were able to successfully calibrate it.
- These gave us the ROC codes currently in use that were needed for the modifications.
- My next plan is to compile this code and test if it works properly. Then I plan to improve this code for Readbacker.



This is a picture of the results of calibration test of the program I found and wrote to ROC

I have put the zip file of this code on the sPHENIX wiki.  
sPHENIX wiki → INTT → ROC → ROC FPGA program

The screenshot shows a web browser displaying the sPHENIX wiki page for the ROC FPGA program. The page is titled "ROC FPGA program" and is highlighted with a red rectangle. The page content includes a sidebar with navigation links, a main content area with sections for "1008 ROC Database", "English Instructions", "ROC Debugging TIPS", and "ROC FPGA program". The "ROC FPGA program" section contains a link to a zip file: [https://sphenixdocdb.sdcc.bnl.gov/0000/000042/001/ROC\\_slow\\_control.zip](https://sphenixdocdb.sdcc.bnl.gov/0000/000042/001/ROC_slow_control.zip). Below this, there is a section titled "How to download FPGA programs to the ROC" with instructions on how to obtain the code from the FVTX wiki.

Collaboration

- Meetings
- Listservers
- Speakers Bureau
- Juniors
- Document database

Tools

- What links here
- Related changes
- Upload file
- Special pages
- Printable version
- Permanent link
- Page information
- Cite this page

• ROC Thermometer Mapping [link](#)

## 1008 ROC Database [\[edit\]](#) [\[edit source\]](#)

- ROC Transportation Record ([spreadsheet](#))
- ROC Database: Record of fixation, etc. To edit it, you need to have authorization. Send an e-mail to [genki.nukazuka@riken.jp](mailto:genki.nukazuka@riken.jp)

## English Instructions [\[edit\]](#) [\[edit source\]](#)

- 2022/7/6 Flash Pro Installation Instruction [pdf](#) (1.2MB)
- Download ACTEL How to [How To Download FPGA to ROC Actel](#) (Copy from [fvtx wiki](#))

## ROC Debugging TIPS [\[edit\]](#) [\[edit source\]](#)

- Debugging Calibration Pulse Circuit [pdf](#) (23/3/14)

## ROC FPGA program [\[edit\]](#) [\[edit source\]](#)

- ROC SlowControl FPGA [https://sphenixdocdb.sdcc.bnl.gov/0000/000042/001/ROC\\_slow\\_control.zip](https://sphenixdocdb.sdcc.bnl.gov/0000/000042/001/ROC_slow_control.zip)

## How to download FPGA programs to the ROC [\[edit\]](#) [\[edit source\]](#)

Obtain ROC FPGA from the FVTX wiki

1. Download the codes from [FVTX wiki](#). The entry on the top of the list shown below is the latest version.

The screenshot shows a table of ROC FPGA codes from the FVTX wiki. The table has columns for ROC, FEM, and Comments. The first row is highlighted in blue. The table lists various codes and their corresponding comments.

| ROC  | FEM   | Comments   |
|--|---|--|
| 24-Oct-13<br>Idle Word<br>Code<br>FPGA_A<br>FPGA_B<br>FPGA_C |   | DATA ROC: rebuild of roc code which sends<br>idle words when there is no data<br>read_DAQ. Allow '0' words within a packet.<br>This is needed to account for the status<br>word which is '0' if no buffers get full.<br>Without this fix, packet reading can get out<br>of sync mid-stream.  |
| Can Use<br>Production<br>Code<br>FPGA_A<br>FPGA_B<br>FPGA_C  | Can Use<br>Production<br>Code<br>FPGA_A<br>FPGA_B<br>FPGA_C | FEM, ROC Data FPGA: Same Functionality<br>as 20-Aug-13 except the ROC data library<br>send idle words when not sending data.<br>DAQ delay setting=0 seems to work for<br>this code at LANL.  |
| Can Use<br>Production<br>Code<br>FPGA_A<br>FPGA_B<br>FPGA_C  | Can Use<br>Production<br>Code<br>FPGA_A<br>FPGA_B<br>FPGA_C | FEM, IB: Merge beam clock generation<br>code with a newer version of the FEM_IB<br>code which has the correct clock-edge for<br>SWAT, ROC, FEM. After accurate code<br>posted in July-13, need to use this fixed<br>version from 20-Aug-13. read_DAQ fix the<br>check for edge of packet/word of header to<br>look for 5 words instead of 4. Without this,<br>data collection was messed up whenever a |