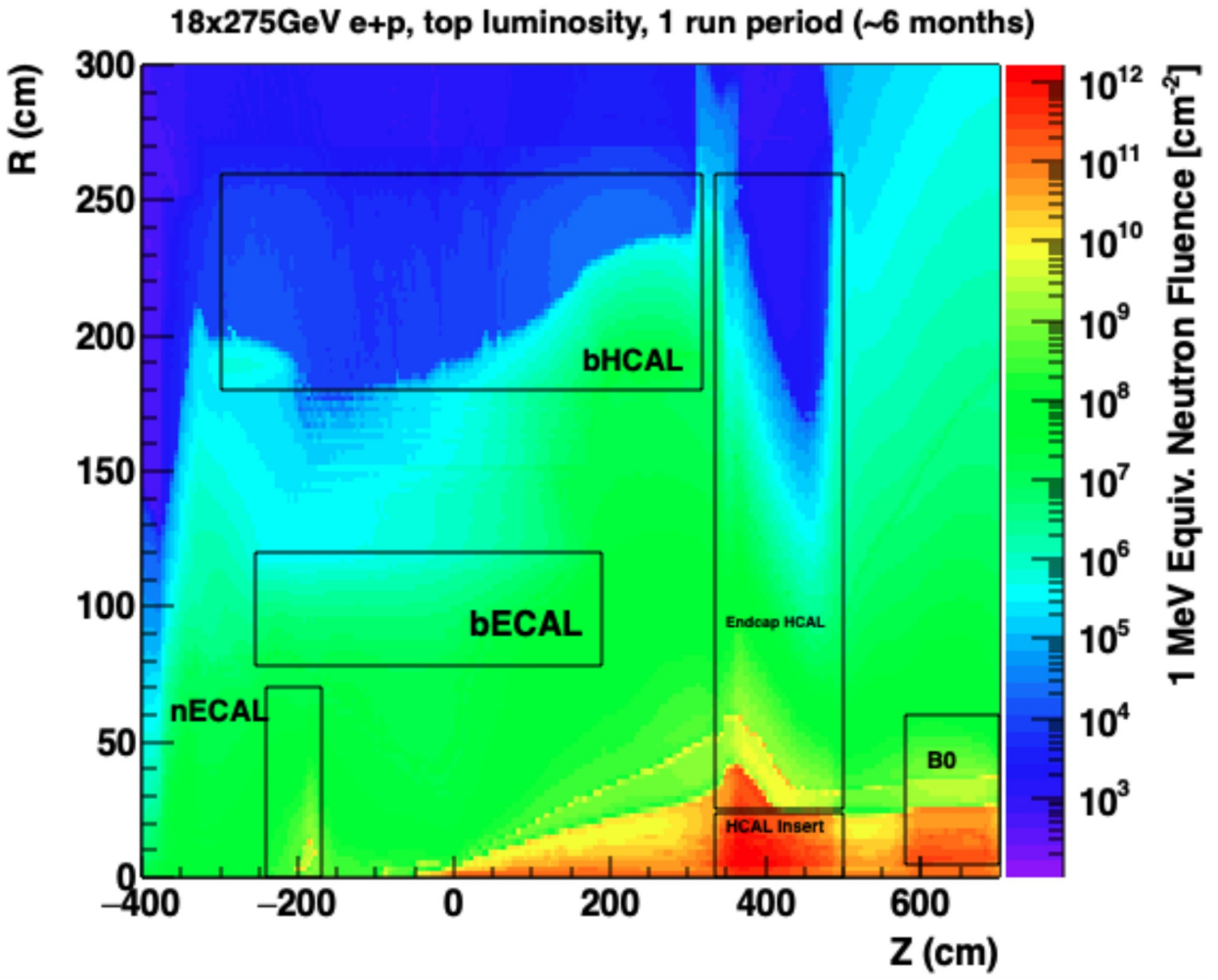
Single Event Upset rates dRICH

P. Antonioli

INFN - Bologna

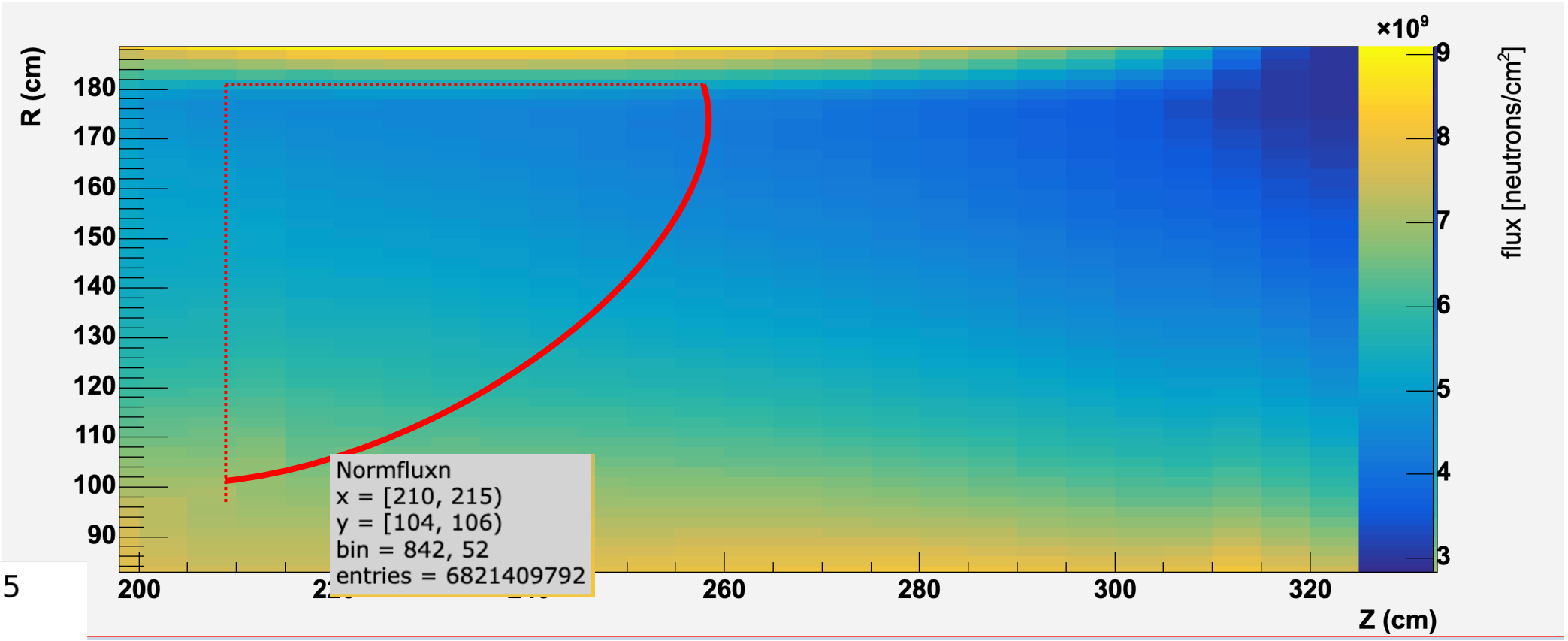
Updated radiation levels

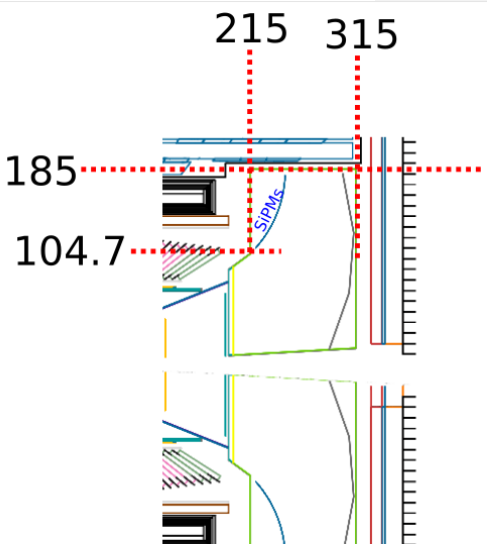
Great work by background group and special thanks to Alex Jentsch
Bookmark this gold mine: https://wiki.bnl.gov/EPIC/index.php?title=Radiation_Doses



Many information now available:
- top lumi
- data on eA, etc..

Neutron fluence at dRICH





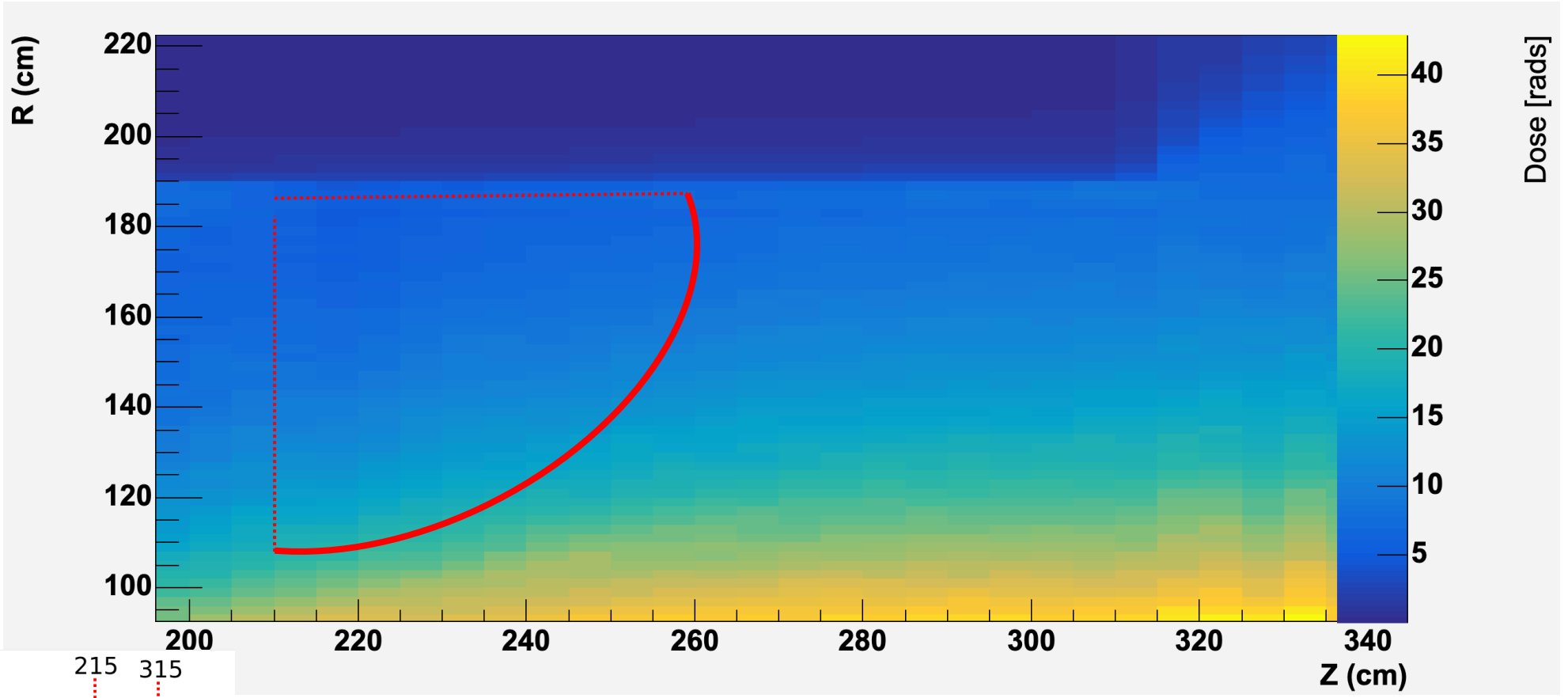
Fluence ~ 6.8 10^9 (max) aver~ 5 10^9 1 MeV $n_{eq.}$ /cm^2

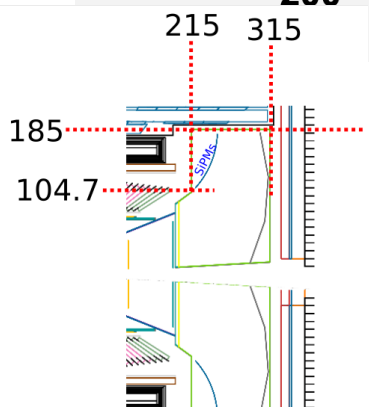
6 months run
Max luminosity in ep

7 10^{10} conservative max after 10 years

Assuming no max luminosity until 2034, 10^{10} fluence could be reached “late 30s”

Total dose at dRICH

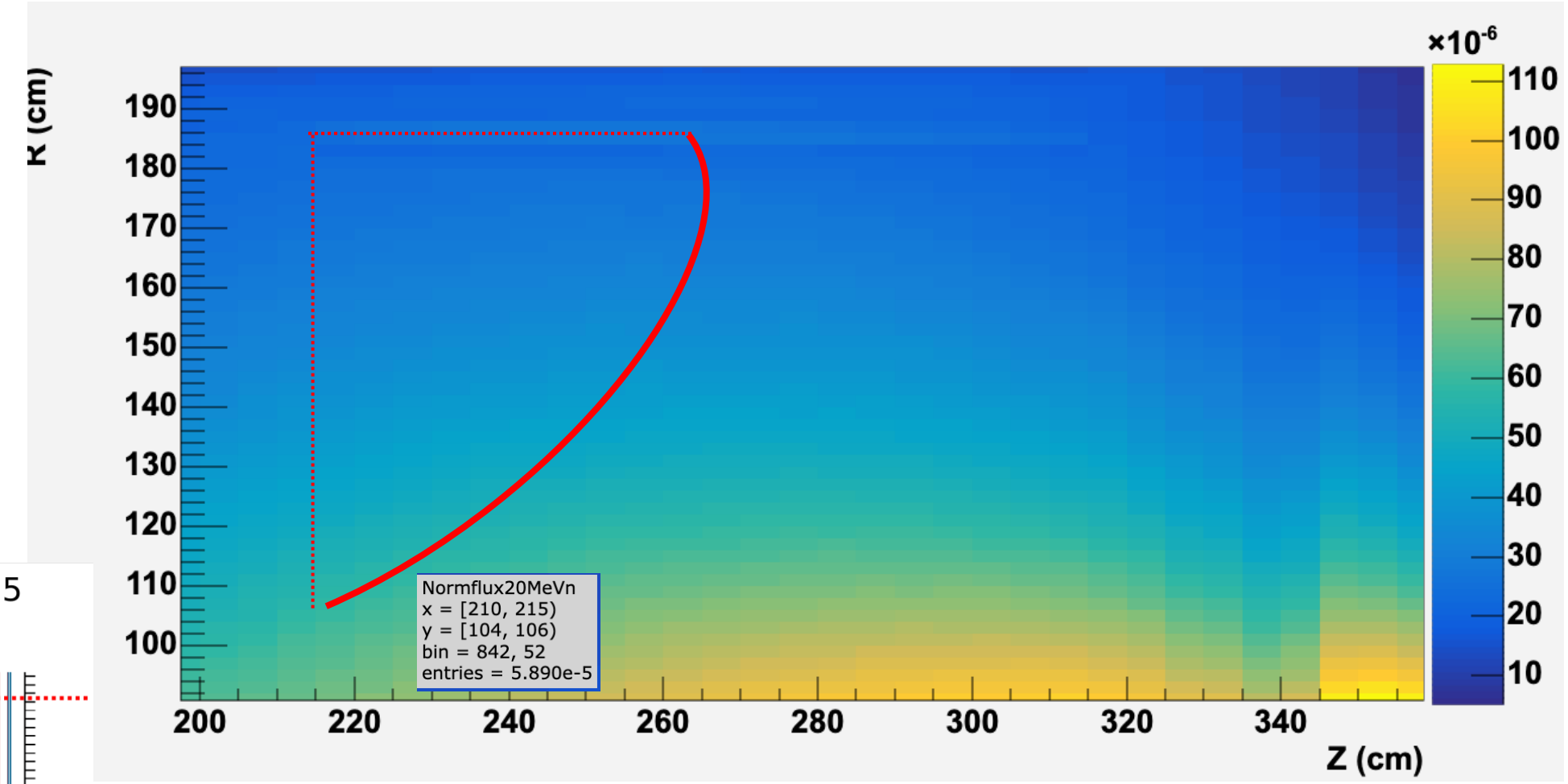


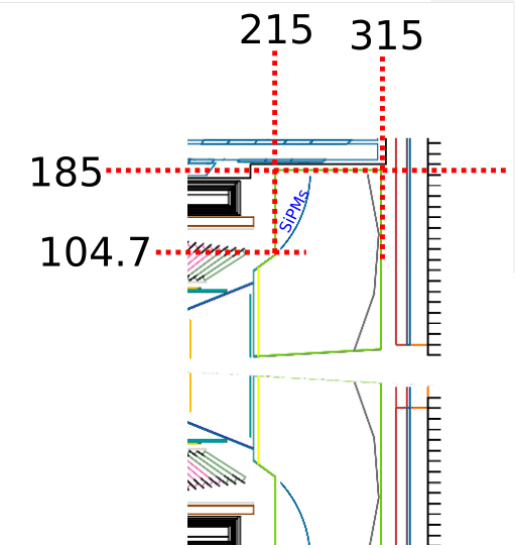


Max 20 rad in 6 months @ 500 kHz

In 10 years 0.2 krad is a reference number

Neutron > 20 MeV

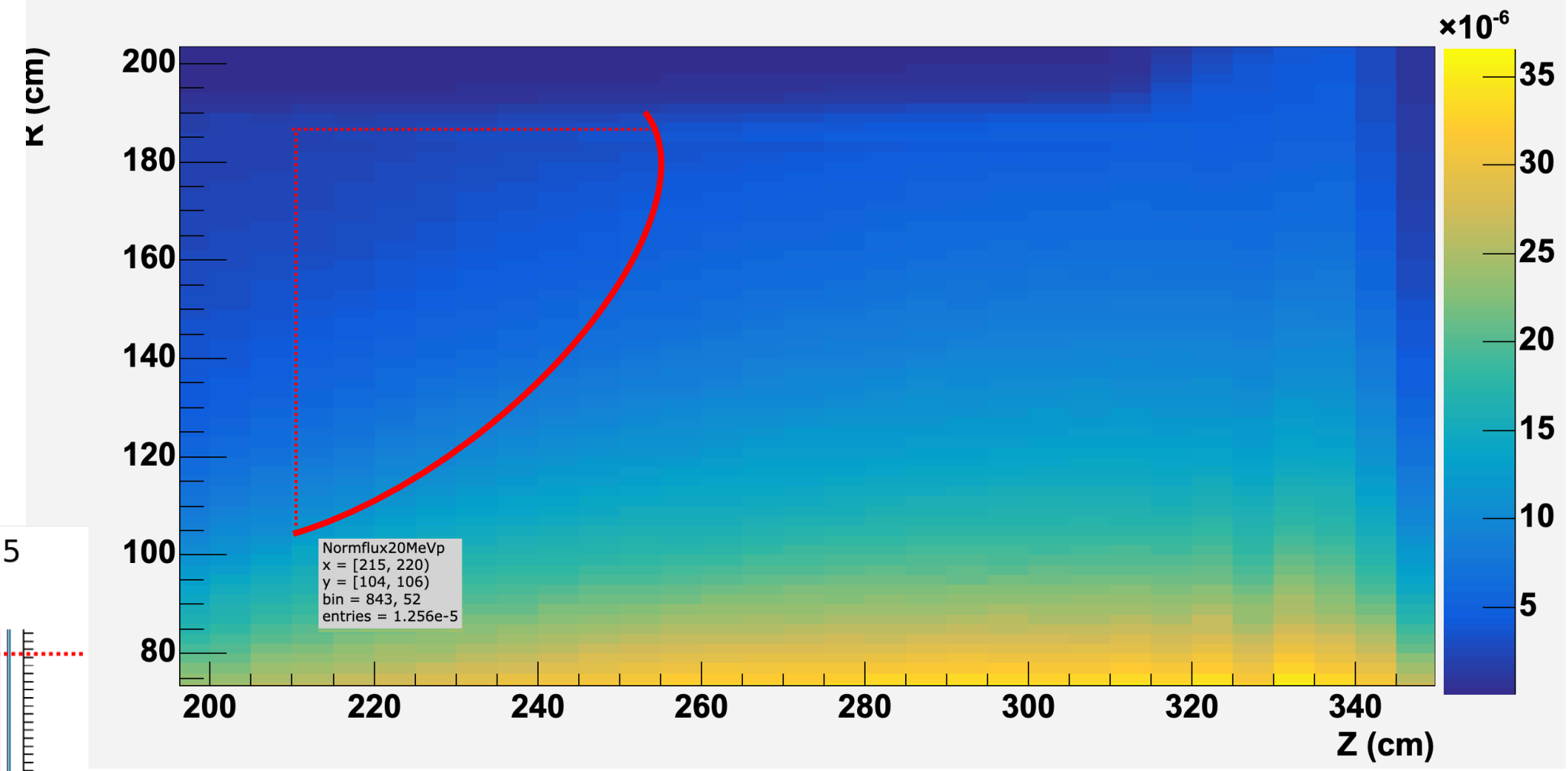


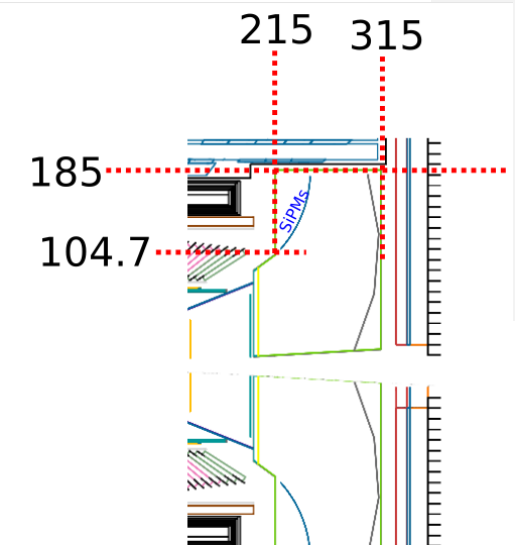


A medium flux value of 5×10^{-5} n>20 MeV / cm^{-2} s^{-1} / collision is pretty conservative

Assuming 500 kHz collision rate ("worst" case) we end up to Φ (n>20 MeV) = 25 cm^{-2} s^{-1}

Proton > 20 MeV





A medium flux value of 1×10^{-5} (p>20 MeV) / cm^{-2} s^{-1} / collision is pretty conservative

Assuming 500 kHz collision rate (“worst” case) we end up to Φ (p>20 MeV) = 5 cm^{-2} s^{-1}

Flux of hadrons (>20 MeV) @ dRICH + SEU rates

Reference flux since now on: Φ (h>20 MeV) = 30 cm^{-2} s^{-1}

Existing measurements on target FPGA: MicroChip PolarFire and Xilinx Artix Ultrascale+

- R. Koga et al, "Heavy Ion and Proton Induced Single Event Effects on Xilinx Zynq UltraScale+ Field Programmable Gate Array (FPGA)" , 10.1109/NSREC.2018.8584319 → SEL reported
- Artix 7: https://www.osti.gov/pages/servlets/purl/1643338
- Ultrascale+: https://www.osti.gov/servlets/purl/1570815 (SEL reported, Weibull fits following irradiation with)
- https://indico.esa.int/event/232/contributions/2162/attachments/1815/2115/SEFUW2018_SEEXCZU3EG_ThomasLange.pdf
- P. Maillard et al, Total Ionizing Dose and Single-Events characterization of Xilinx 20nm Kintex UltraScale, 10.1109/RADECS47380.2019.9745695, → no SEL reported
- A. Scialdone, "FPGA qualification for the LHC radiation environment" , Master Thesis, Politecnico di Torino -→ results on PolarFIre and NanoXplore
- [1] Xilinx → https://docs.xilinx.com/r/en-US/ug116/SEU-and-Soft-Error-Rate-Measurements
- [2] Microsemi → https://www.microsemi.com/document-portal/doc_view/1243481-tr0043-polarfire-neutron-test-results-test-report

Target FPGA	Manufacturer/Tech	Config. Tech.	SEU (cm^2/bit) for CRAM	SEU (cm^2/bit) for BRAM/LSRAM
XCAU10P-2FFVB676E	Xilinx Artix Ultrascale+	RAM	$2.67\ 10^{-16}$	$9.82\ 10^{-16}$ [1]
XCAU15P-2FFVB676E	Xilinx Artix Ultrascale+	RAM	$2.67\ 10^{-16}$	$9.82\ 10^{-16}$ [1]
MPF200T-FCVG484E	Microchip/PolarFire	FLASH	N/A	$1.5\ 10^{-14}$ [2]
MPF200T-FCSG536I	Microchip/PolarFire	FLASH	N/A	$1.5\ 10^{-14}$ [2]

SEU rates in Configuration RAM (Ultrascale+)

Reference flux since now on: Φ (h>20 MeV) = 30 cm^{-2} s^{-1}

Target FPGA	Config. Tech.	SEU (cm2/bit) for RAM	Conf bits	CONF MTBF (s)/FPGA
XCAU10P-2FFVB676E	RAM	2.67 10^{-16}	42799456	2.9E+6
XCAU15P-2FFVB676E	RAM	2 67 10^{-16}	42799456	2.9E+6

1252 FPGA → MTBF in the dRICH → 2300 s → 38.8 minutes

Every 40 minutes a configuration bit of a Artix Ultrascale+ will be upset. Note this is at maximum interaction rate

Still to be pondered pros/cons with respect to PolarFire!

- space on RDO
- performance
- …