Readout & DAQ update toward review

Pietro Antonioli, Davide Falchieri

INFN Bologna

Context of this update to dRICH meeting:

- Preparing for dRICH review (5th July), eRD submissions (7th July) and INFN budgeting (2024 + multi year) various refinements in progress
- Several meetings among groups working on electronics held since last dRICH discussion on DAQ + interim presentation at DAQ WG (June 1st), since 3rd May presentation at dRICH meeting

Outline of this communication:

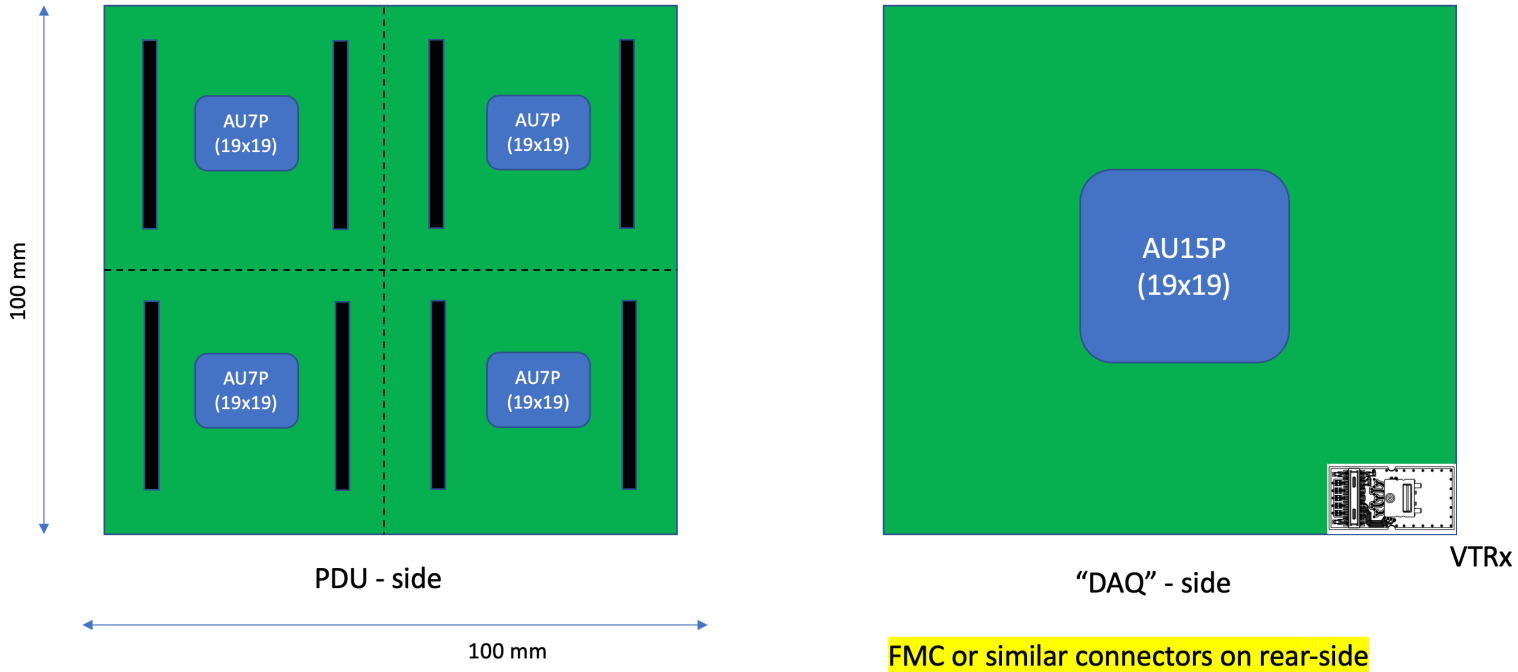
- What to present at dRICH review about DAQ
- Share information update on costs, components, radiation levels

Yellow boxes are not for dRICH review slides but to prepare discussion for dRICH review

Where we were (few weeks ago)

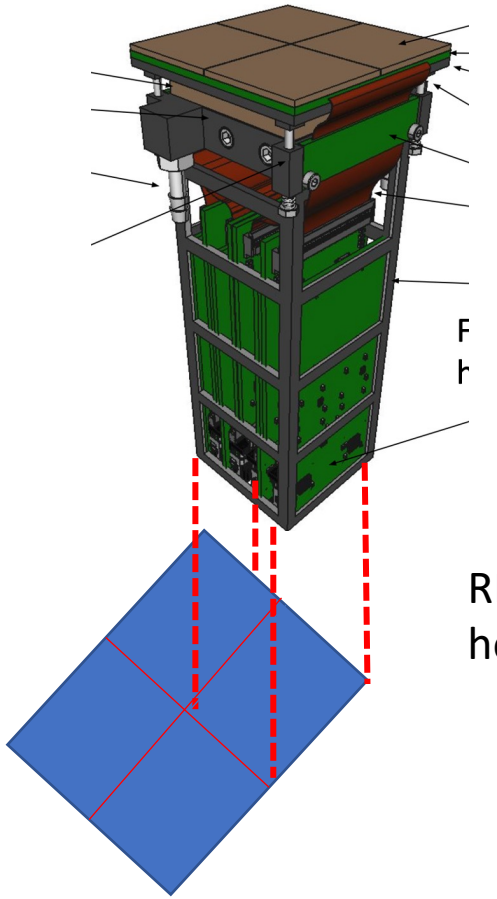
RDO challenges: potential design (2b)

Not for dRICH review



03/05/2023 dRICH meeting 18

RDO made with two cards:
- slave RDO (1 for 1 FPU) (4 piggy backs
- a master RDO (aggregating 4 slave RDO)

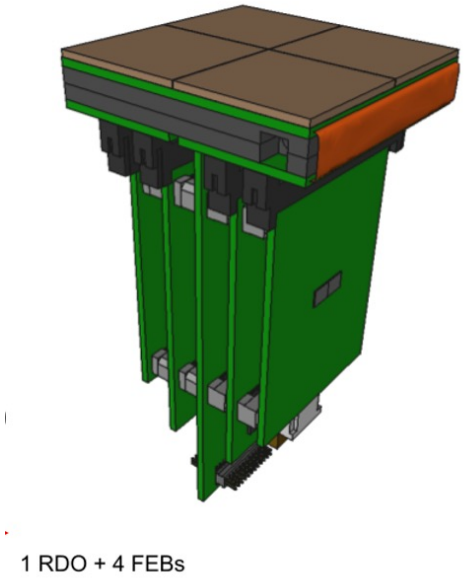


RDO "plugged" horizontally

The need of a two-tier hierarchy of FPGAs descends from PIN I/O requirements

Readout of dRICH PDU

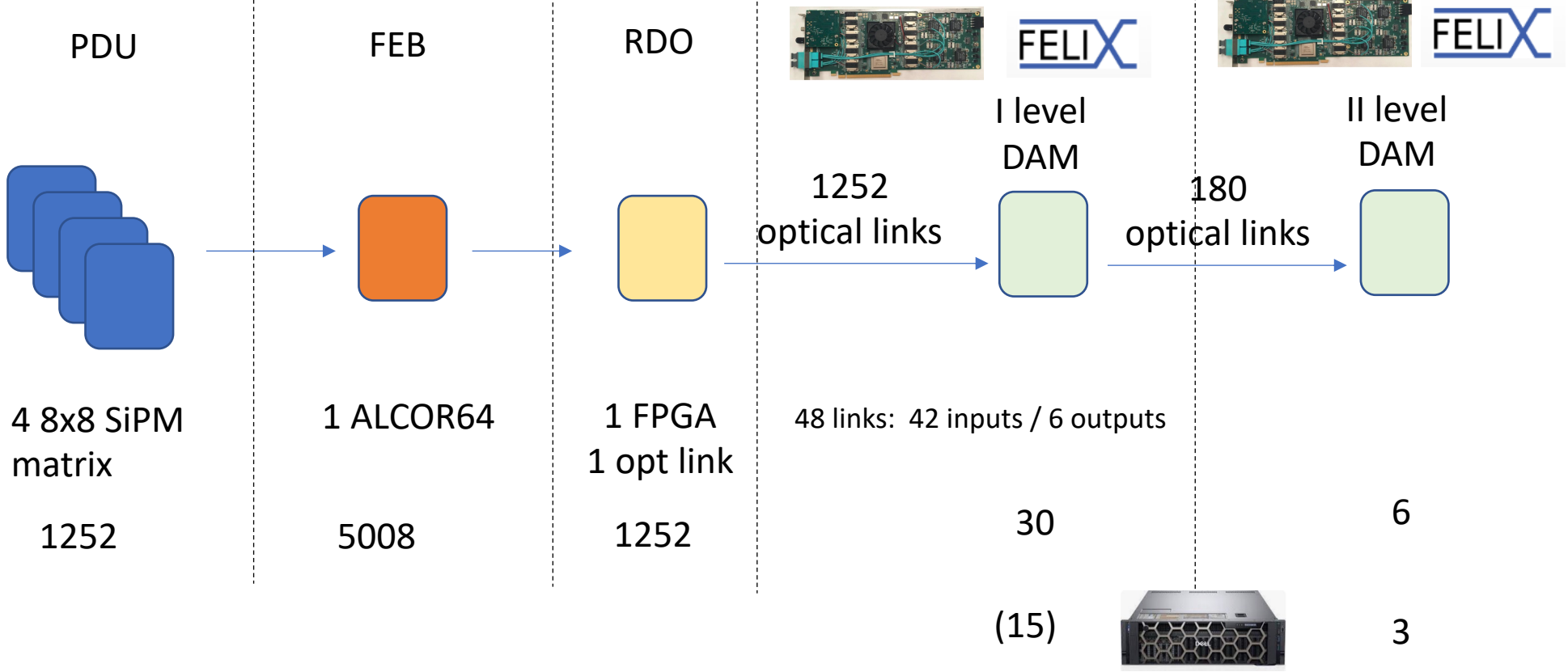
dRICH PDU: Photosensor Detector Unit
- 4 8x8 matrix (3x3 mm2 SiPM) → 256 sensors
- each FEB (4) hosts 1 ALCOR64
- 1 RDO reads 4 ALCOR64



- RDO in the middle of FEB maximizes (smal) area available: RDO is 4 x 9 cm: still challenging but no show stoppers for the moment
- The dRICH electronic - burger :

Realize a RDO demonstrator in 2024 is key milestone toward TDR

dRICH readout organization

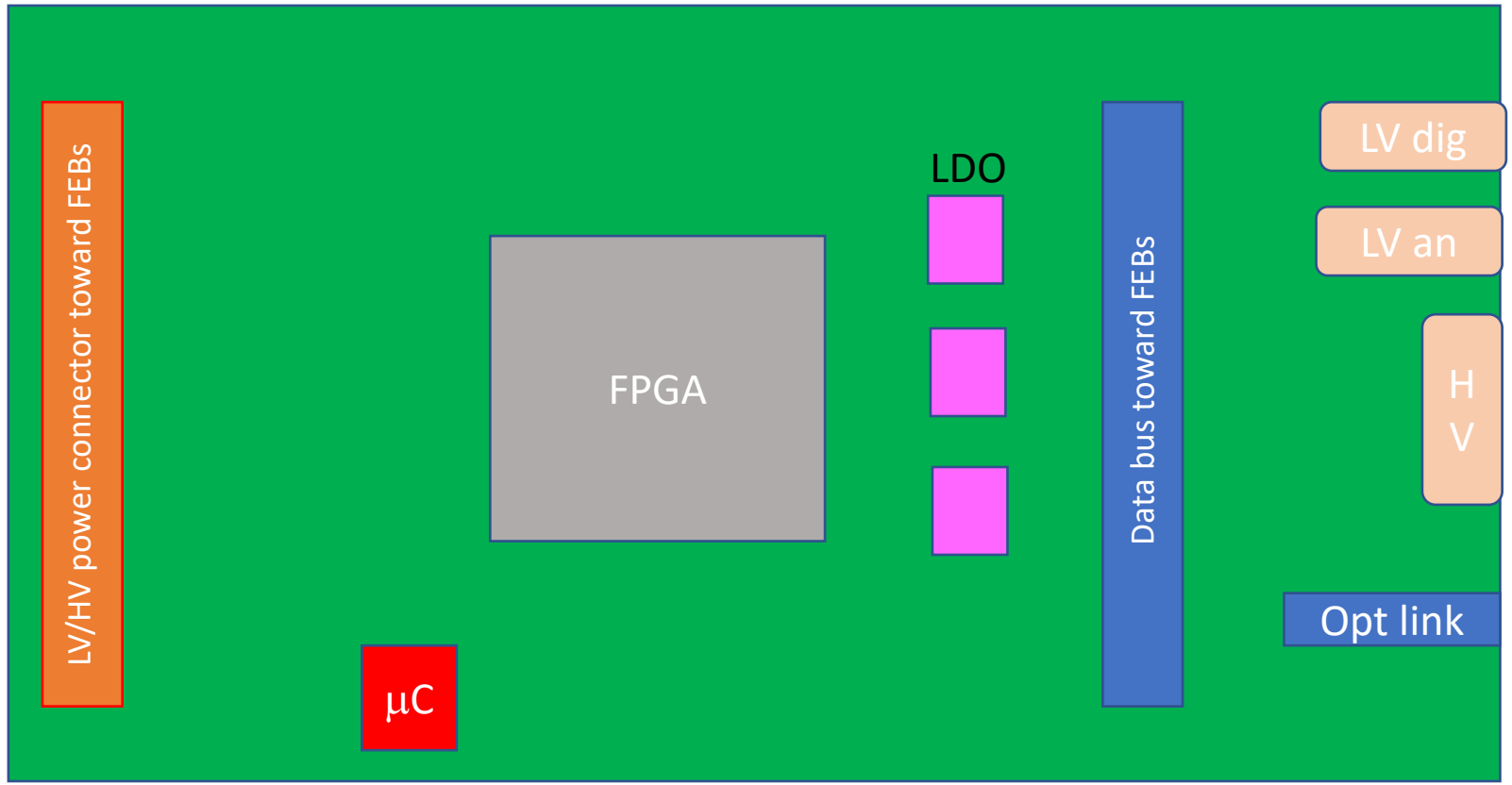


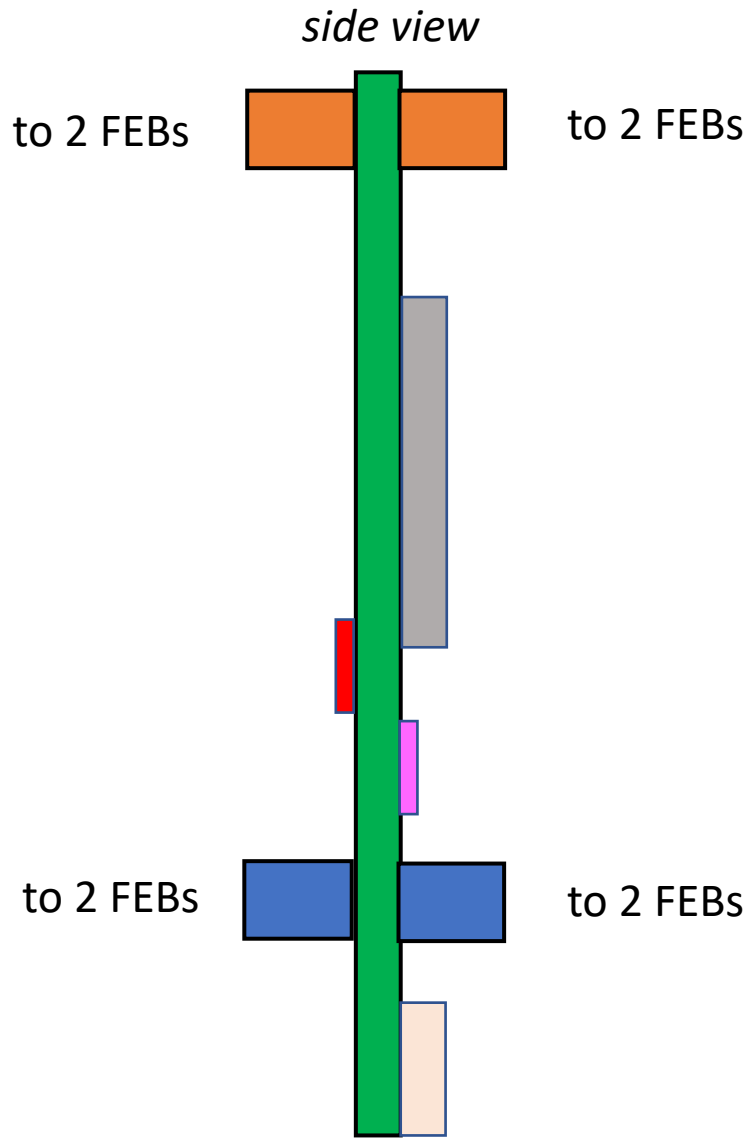
Key features:

- strong modularity (“1 PDU has all”)
- **hierarchy of DAM** used as data concentrator (input got from DAQ WG)
- Big data reduction happens at DAM-L1 using **interaction tagger** (input from EIC project). Throughput is modelled assuming an interaction tagger signal can reach dRICH DAM with max 2 us latency
- Data available @ DAM-L2 are per sector at FPGA level → potential for further algorithms for data reduction
- DAM-L1 might be eventually stored inside hall (in rack enclosure)

These numbers are not the “standard” ones declared so far in some GoogleSheets. What about the review?

dRICH RDO conceptual design





Not on scale, not a placement! RDO prototype foreseen in 2024

dRICH readout modeling

For dRICH review we can expose a subset of all this…
Basic number is input sensor rate… the rest follows…

dRICH daq Modeling

File Modifica Visualizza Inserisci Formato Dati Strumenti Estensioni Guida

	dRICH DAQ parameters	
	RDO boards	1252
	ALCOR64 x RDO	4
	dRICH channels (total)	320512
	Number of DAM L1	30
	Input link in DAM L1	42
	Output links in DAM L1	6
	Number of DAM L2	6
	Input link to DAM L2	30
	Link bandwidth [Gb/s] (assumes PolarFIre)	12,7
	Interaction tagger reduction factor	200
	Interaction tagger latency [s]	2,00E-06
	EIC parameters	
	EIC Clock [MHz]	98,522
	Orbit efficiency (takes into account gap)	0,92

ALCOR parameters		Notes
Front end limit [kHz]	4000	
ALCOR Clock [MHz]	320	It will be 394.08 MHz or 295.55 MHz
Channels/serializer	8	
Bits per hit	64	2 32-bit words per hit (also TOT)
Bits per hit encoding 8/10	80	
Serializer band limit [Mb/s]	640	
Theoretical Serializer limit/ channel [kHz]	1000	this would be with 0 control words
Serializer limit single ch [kHz]	250	this is expected to improve with ALCOR v3
Number of serializer per chip	8	
Channel/chip	64	
Shutter width (ns)	2	

	Bandwidth analysis		Limit	Comments
INPUT	Sensor rate per channel [kHz]	500,00	4.000,00	
	Rate post-shutter [kHz]	92,00	250,00	
	Throughput to serializer [Mb/s]	57,50	640,00	
	Throughput from ALCOR64 [Mb/s]	460,00		limit FPGA dependent, da verificare
	Throughput from RDO [Gb/s]	1,80	12,70	
	Input at each DAM I [Gbps]	75,47	533,40	
	Buffering capacity at DAM I [MB]	0,02		to be checked
	Throughput from DAM I to DAM II [Gbps]	0,38	12,70	this might be higher (from FELIX to FELIX)
	Output to each DAM II (1 DAM II/sector) [Gbps]	11,32	381,00	

	Aggregated dRICH data		Comments
	Total input at DAM I [Gb/s]	2.264,06	This is only "inside" DAM, not to be transferred on PCI
	Total input at DAM II [Gb/s]	67,92	
	Total output from DAM II [Gb/s]	67,92	We might assume here a furter reduction 2 from more stringent time cuts

Message to give:

Throughput under control!

From 2.2 Tbps (at DAM-L2)
at 67 Gbps (at DAM-L1)
@500 kHz sensor

Do we need a slide for this?

Why?

- We get rid of any hardware development for intermediate DAM (“more firmware, less hardware” approach)
- Space is a big challenge → this approach saves space inside readout box
- Cost → to be done full assessment, but scenario with 312 links is not for free (and it entails, however 6-7 DAMs, 312 medium-size FPGA medium size, etc.) →back of the envelope computation is approx. +600 k$ (just fresh money but if you keep in mind salaries balance is different!)(*)
- PDU very modular
- Less power consumption inside readout box
- We add cables, materials inside readout box

FPGA	cost estimate (small qty) EU
XCAU10P-2FFVB676E	100-250
XCAU15P-2FFVB676E	300-350
MPF200T-FCVG484E	300-350
MPF200T-FCSG536I	400-485

This slide NOT for dRICH review

Preparing 2024 RDO plans (in second semester 2023)

During 2024 we need to build a prototype RDO card (”close to final”) where we demonstrate:

- We can fit within space
- We start talking with ePIC DAQ (“FELIX based”)
- We are able to serve 2023 electronics (old ALCOR32/old FEB with FireFly connectors)
- We operate test beam 2024 (October) with optical link readout and RDO

The exercise must aim:

- To fully define specs of RDO (possibly by December 2023)
- To select FPGA candidate (and it might include some radiation test)
- To define ancillary services on RDO, we will work out within dRICH electronics the divison of work (LV, watchdog, communication, … → conversations on-going)
- Several studies / collection of material in progress

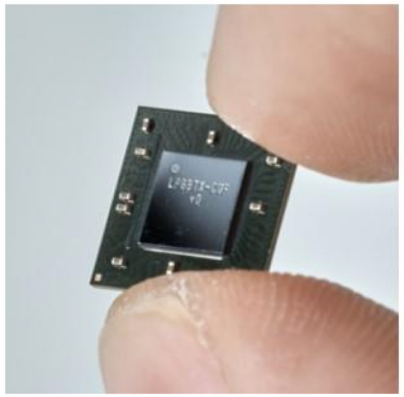
This slide NOT for dRICH review

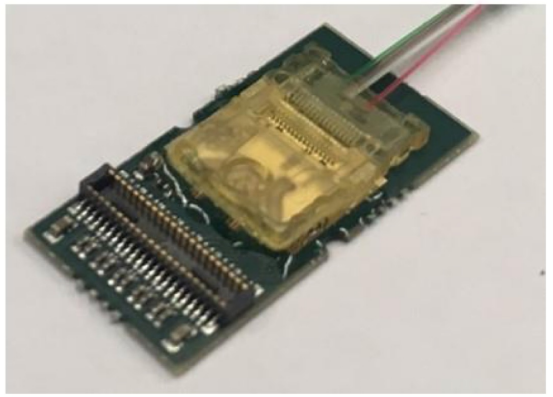
Additional information for dRICH meeting

None of the following for dRICH review

Optical transceiver: VTRX+

- **lpGBT and Versatile link +**
  - https://ep-ese.web.cern.ch/project/lpgbt-and-versatile-link
  - lpGBT
  - VTRX+
- **produced for LS3/Run4**
- **no iteration after that for mass production is planned (for now)**
  - performance assumed to be good for LS4/Run5
  - if this is not correct → we need to speak up now
  - future development effort goes to EP-RD WP6



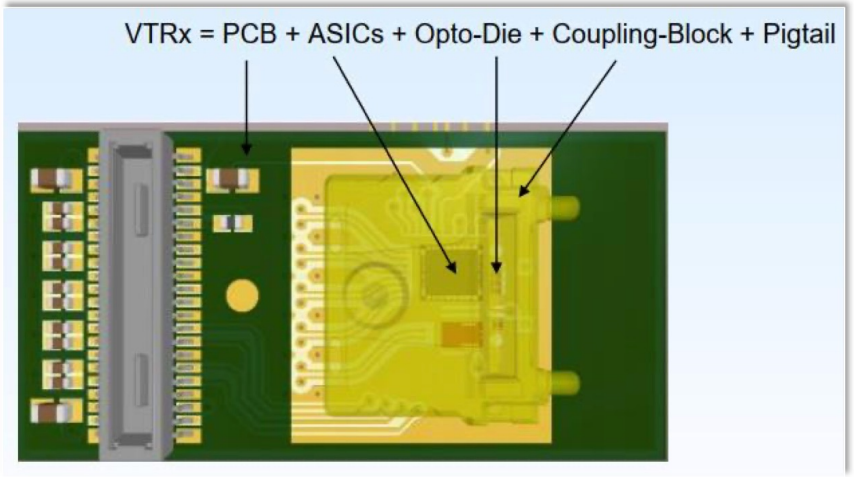


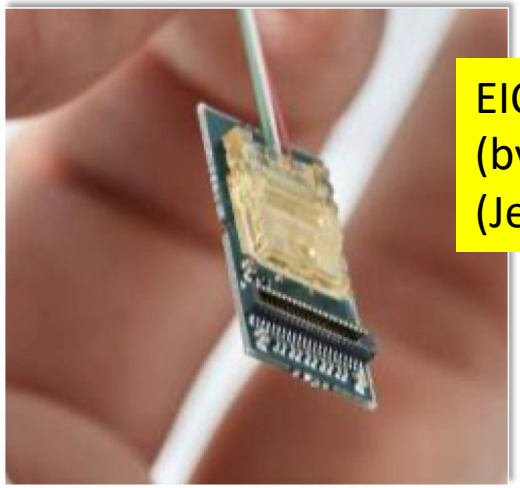
Slide from A. Kluge, ALICE Electronics coordinator

Note lpGBT not an option for EIC, but VTRX+ is a miniaturized opt. transceiver (rad hard) that might be interesting

VTRx+ Front-end Module

- **Versatile**
  - Up to 4 Tx + 1 Rx, configurable by masking channels
- **Miniaturised**
  - 20 x 10 x 2.5 mm
- **Pluggable**
  - Electrical connector
- **Data-rate**
  - Tx: up to 4×10 Gb/s, Rx: 2.5 Gb/s
- **Environment**
  - Temperature: -35 to + 60 °C
  - Total Dose: 100 Mrad
  - Total Fluence: $1x10^{15}$ n/cm² and $1x10^{15}$ hadrons/cm²
- **Status**
  - Pre-production ongoing
  - Solving problems with module assembly
  - Alignment of optical components
  - Ramping up to 2k modules/month in 2023



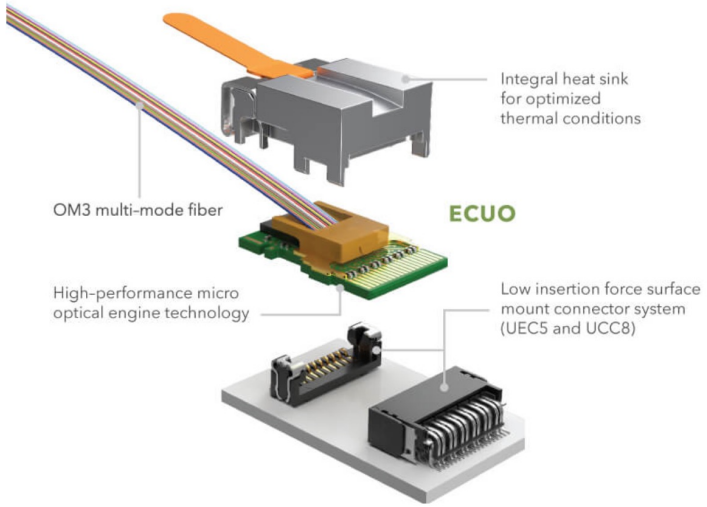


EIC project has been informed
(by us) that a decision is needed quickly
(Jeff reported the issue at last TIC)

Slide from A. Kluge, ALICE Electronics coordinator

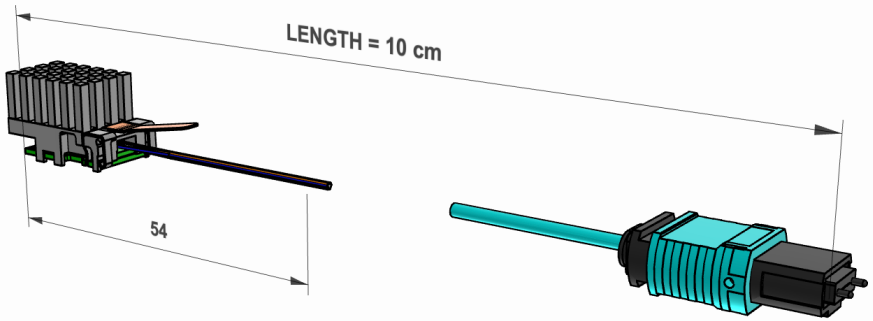
- **quantity and commitment to buy needs to be settled by end of 2023**
  - as components need to be purchased

Other optical transceivers for RDO?



Samtec FlyOver (used in many PCI cards) might be a possibility

- To be checked under radiation
- Dimensions should be similar to current Samtec FireFly (copper):
  2.5 x 1 cm not so different w.r.t. to VTRX+ but big heat-sink
- Cable to minipod connectors for patch panels… etc.
- All to be studied!



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Future-proof system with interchangeability of FireFly™ copper and optical using the same micro connector system for up to 28 Gbps per lane.

Features

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- Variety of integral heat sink and End 2 options
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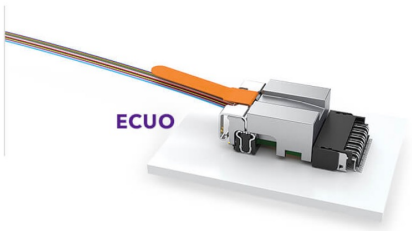
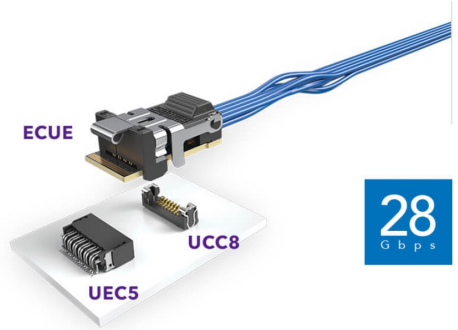




See other presentation (if time allowed)
Short summary:

- more precise data coming from background WG. Magic conservative numbers for dRICH:

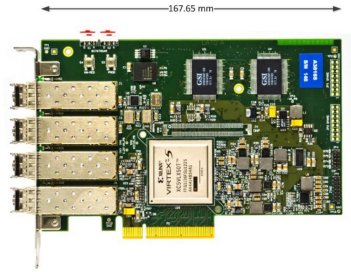
TID = 0.2 krad (10 years at max. lumi)
Φ (n 1-MeV n_{eq}) = 7 10^{10} (10 years at max lumi) / cm^2
ϕ (h>20 MeV) = 20 /cm^2 s^{-1} (at max lumi)

- trade-off between a Flash technology and RAM to be studied
- several key irradiation tests will be needed in 2024 (plus the study of literature, when available)

Building a plan

dRICH World

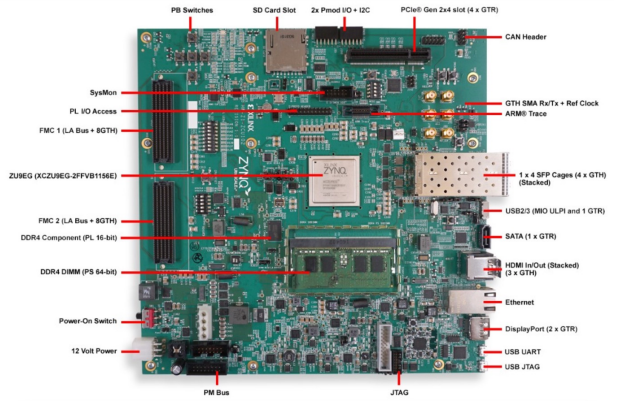
- define FEB-RDO specs!!! → by December 2023 at the latest worked out internally dRICH
- Production RDO + breakout-boards: first semester 2024
- @test-beam 2024: read 8 PDU using CONET IPCORE and 2 PCIe CARD A3818 from CAEN (all hardware + know-how available from ALICE
- Some radiation tests of key component @TIFPA to be planned for 2024 → eRD109



ePIC World

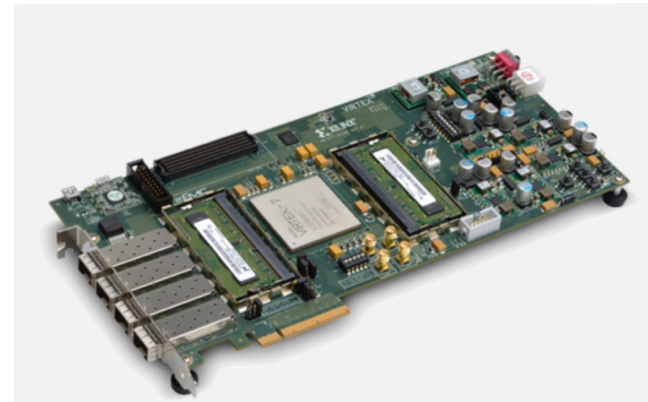
- Test/Development of ePIC DAQ link on a pair of Zynq ZCU102 (1 available, 1 from project)

  Davide/Pietro part of a small sub-DAQ WG to define specs of DAQ link
  These cards will be used to define specs. We might play already with RDO when existing (clock transmission etc). Since Fall 2023



- No FELIX available from ATLAS/BO: we will use VC709 as main “FELIX” development platform

  → ATLAS provides FW for VC709 operating it as a “mini-FELIX”



→ we need to collect more information about FELIX, the project expects to “release” FELIX in 2025, following shutdown of sPHENIX

Backup

First FPGA candidate: Xilinx Artix Ultrascale+ family

	AU7P	AU10P	AU15P	AU20P	AU25P
System Logic Cells	81,900	96,250	170,100	238,437	308,437
CLB Flip-Flops	74,880	88,000	155,520	218,000	282,000
CLB LUTs	37,440	44,000	77,760	109,000	141,000
Max. Distributed RAM (Mb)	1.1	1.0	2.5	3.2	4.7
Block RAM Blocks	108	100	144	200	300
Block RAM (Mb)	3.8	3.5	5.1	7.0	10.5
UltraRAM Blocks	–	–	–	–	–
UltraRAM (Mb)	–	–	–	–	–
CMTs (1 MMCM and 2 PLLs)	2	3	3	3	4
Max. HP I/O(1)	104	156	156	156	208
Max. HD I/O(2)	144	72	72	72	96
DSP Slices	216	400	576	900	1,200
System Monitor	1	1	1	1	1
GTH Transceiver(3)	4	12	12	–	–

Package (1)(2)(3)	Package Dimensions (mm)	AU7P	AU10P	AU15P	AU20P	AU25P
		HD I/O, HP I/O, GTH, GTY				
UBVA292	10.5x8.5	72, 58, 4, 0				
UBVA368	11.5x9.5		24, 104, 8, 0	24, 104, 8, 0		
SBVB484	19x19		48, 156, 12, 0	48, 156, 12, 0		
SBVC484	19x19	144, 104, 4, 0				
SFVB784	23x23				72, 156, 0, 12	96, 208, 0, 12
FFVB676	27x27		72, 156, 12, 0	72, 156, 12, 0	72, 156, 0, 12	72, 208, 0, 12

Xilinx Artix Ultrascale+ family

VCCINT = 0.850 V
VCCAUX = 1.800 V
VCCO = 1.140 – 3.400 V for HD I/O banks
VCCO = 0.500 – 1.900 V for HP I/O banks

HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.

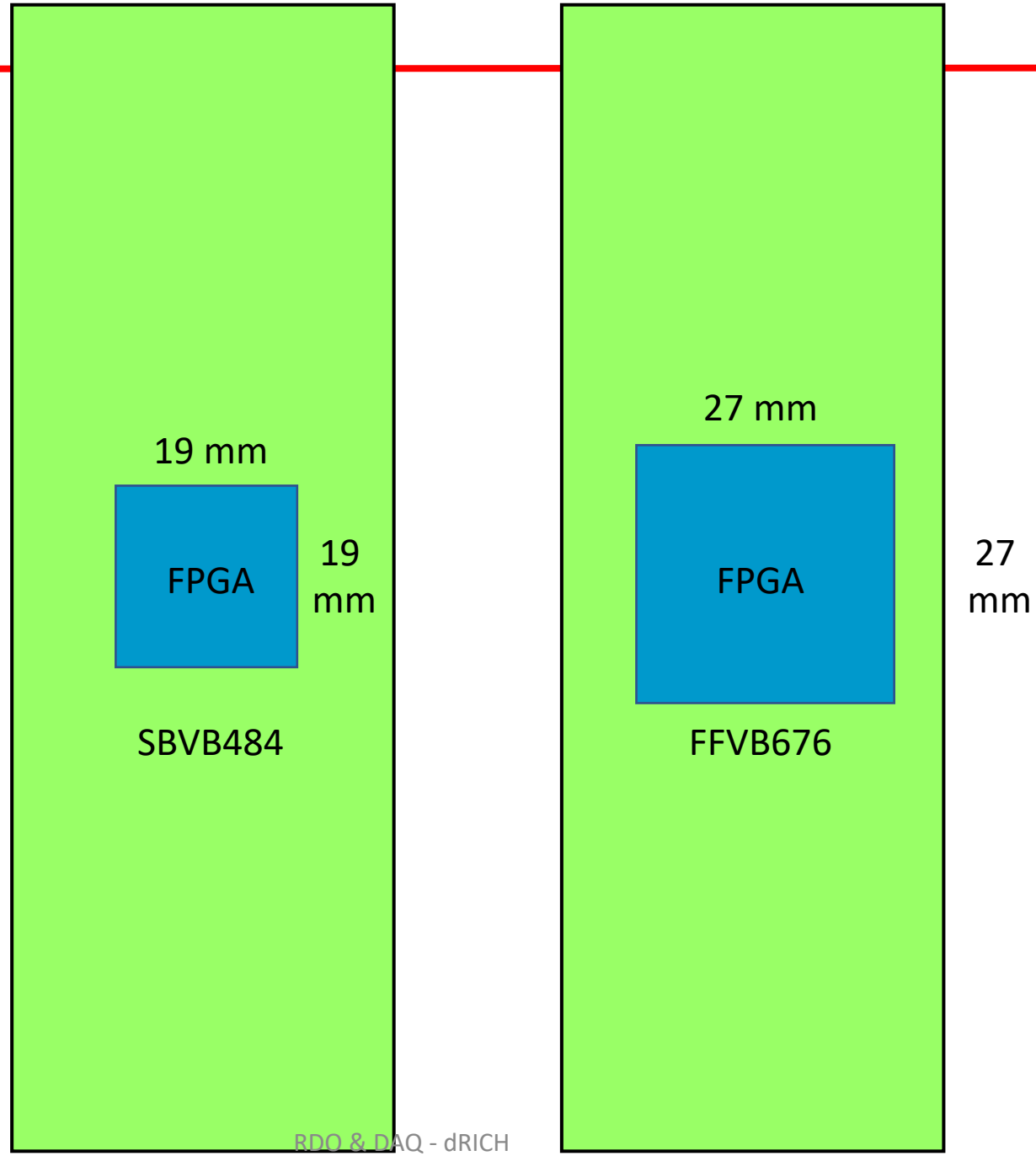
HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.

GTH and GTY transceiver line rates are package limited: SFVB784, SBVB484, UBVA368, and UBVA292 to 12.5Gb/s

LVDS DC specifications (**HP** I/O banks)

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO} [1]	Supply voltage		1.710	1.800	1.890	V
V_{ODIFF} [2]	Differential output voltage: $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	454	mV
V_{OCM} [2]	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF} [3]	Differential input voltage: $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High		100	350	600 [3]	mV
V_{ICM_DC} [4]	Input common-mode voltage (DC coupling)		0.300	1.200	1.425	V

On-scale drawings (scale factor = 1.5)



Choosing a Xilinx Artix Ultrascale+ requires both:

- a QSPI Flash
- a Microchip FPGA performing scrubbing

Second FPGA candidate: Microchip Polarfire family

	MPF050	MPF100	MPF200	MPF300	MPF500
Logic Elements (4LUT + DFF)	48K	109K	192K	300K	481K
Math Blocks (18 × 18 MACC)	150	336	588	924	1480
LSRAM Blocks (20 Kb)	160	352	616)	952	1520
uSRAM Blocks (64 × 12)	450	1008	1764	2772	4440
Total RAM (Mb)	3.6	7.6	13.3	20.6	33
uPROM (Kb)	216	297	297	459	513
User DLLs/PLLs	8	8 each	8 each	8 each	8 each
250 Mbps–12.7 Gbps Transceiver Lanes	4	8	16	16	24
PCIe® Gen 2 Endpoints/Root Ports	2	2	2	2	2
Total User I/O	176	296	364	512	584

Microchip Polarfire packages

VCCINT = 1.0 V

HSIO DC IO supply:
1.2V, 1.35V, 1.5V, 1.8V

GPIO DC IO supply: 1.2V, 1.5V, 1.8V, 2.5V, 3.3V

	MPF050	MPF100	MPF200	MPF300	MPF500
Type/Size/Pitch	Total User I/O (HSIO/GPIO) GPIO CDRs/XCVRs				
FCSG325 (11 × 11, 11 × 14.5 0.5 mm)	164 (84/80) 6/4	170 (84/86) 8/4	170 (84/86) 8/4		
FCSG536 (16 × 16, 0.5 mm)			300 (120/180) 15/4	300 (120/180) 15/4	
FCVG484 (19 × 19, 0.8 mm)	176 (96/92) 7/4	284 (120/164) 14/4	284 (120/164)14/4	284 (120/164) 14/4	
FCG484 (23 × 23, 1.0 mm)		244 (96/148) 13/8	244 (96/148) 13/8	244 (96/148) 13/8	
FCG784 (29 × 29, 1.0 mm)			364 (132/232) 20/16	388 (156/232) 20/16	388 (156/232) 20/16
FCG1152 (35 × 35, 1.0 mm)				512 (276/236) 24/16	584 (324/260) 24/24

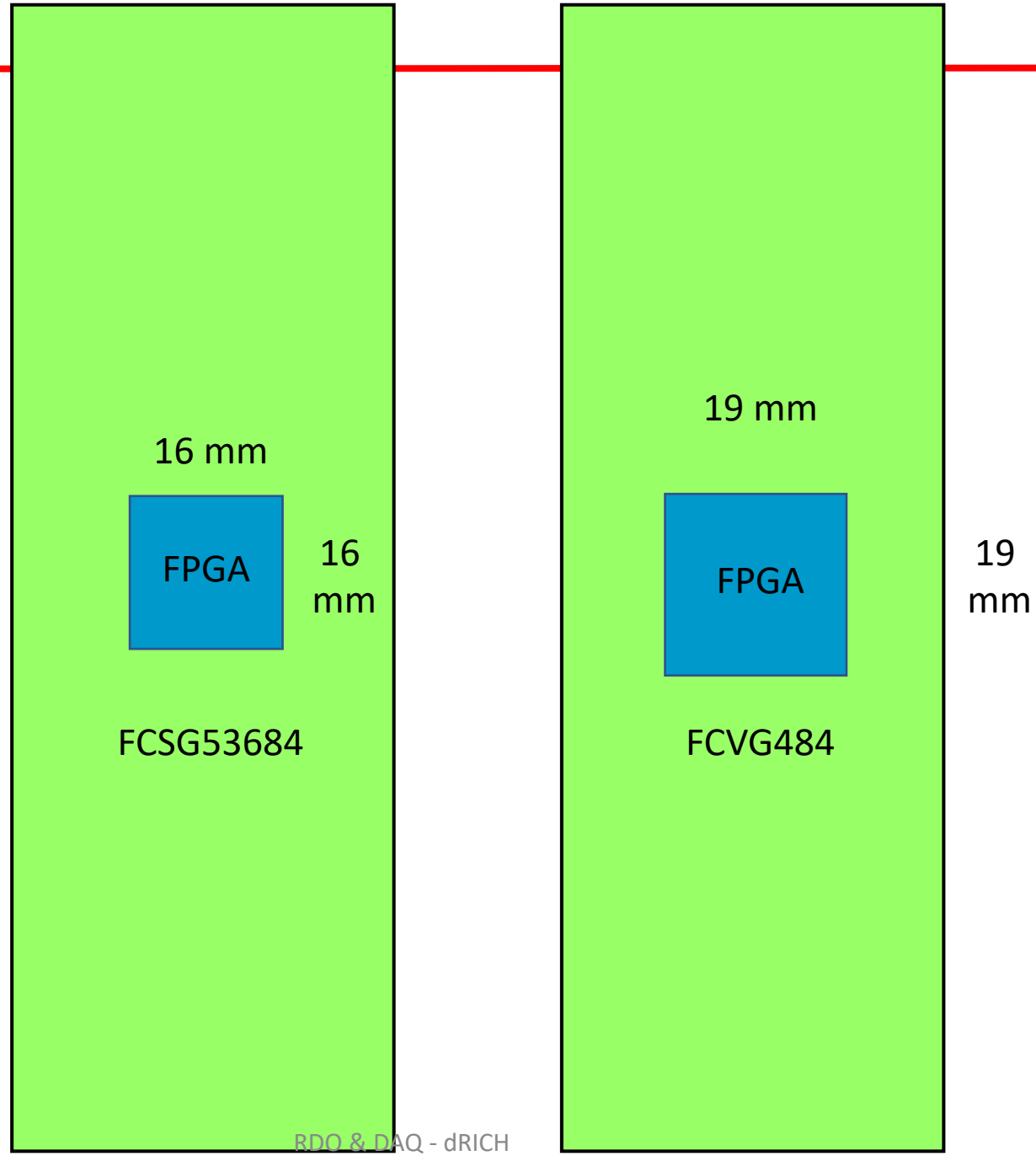
Differential DC input levels

I/O Standard	Bank Type	V_{ICM_RANGE} Libero Setting	V_{ICM} [1,3] Min (V)	V_{ICM} [1,3] Typ (V)	V_{ICM} [1,3] Max (V)	V_{ID} [2] Min (V)	V_{ID} Typ (V)	V_{ID} Max (V)
LVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS25 [7]	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18G[4]	GPIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18 [7]	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6

Differential DC output levels

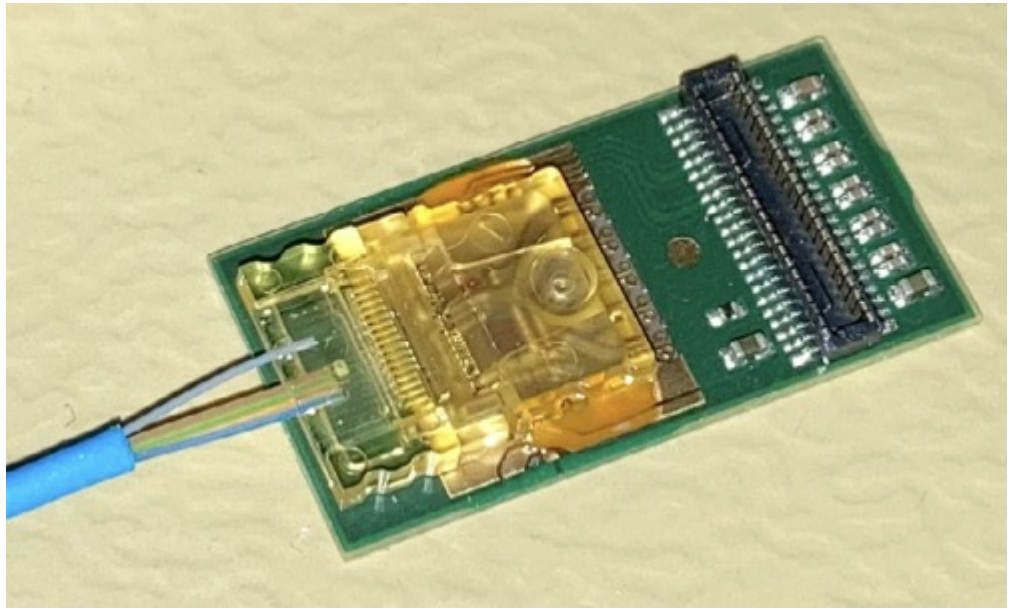
I/O Standard	Bank Type	V_{OCM} [1] Min (V)	V_{OCM} Typ (V)	V_{OCM} Max (V)	V_{OD} [2] Min (V)	V_{OD} [2] Typ (V)	V_{OD} [2] Max (V)
LVDS33	GPIO	1.125	1.2	1.375	0.25	0.35	0.45
LVDS25 [4]	GPIO	1.125	1.2	1.375	0.25	0.35	0.45
LVDS18G[4]	GPIO	1.125	1.2	1.375	0.25	0.35	0.45

On-scale drawings (scale factor = 1.5)



it would also allow to save on the QSPI Flash (not needed)

VTRX+



VTRX+: 20 x 10 x 2.5 mm^3