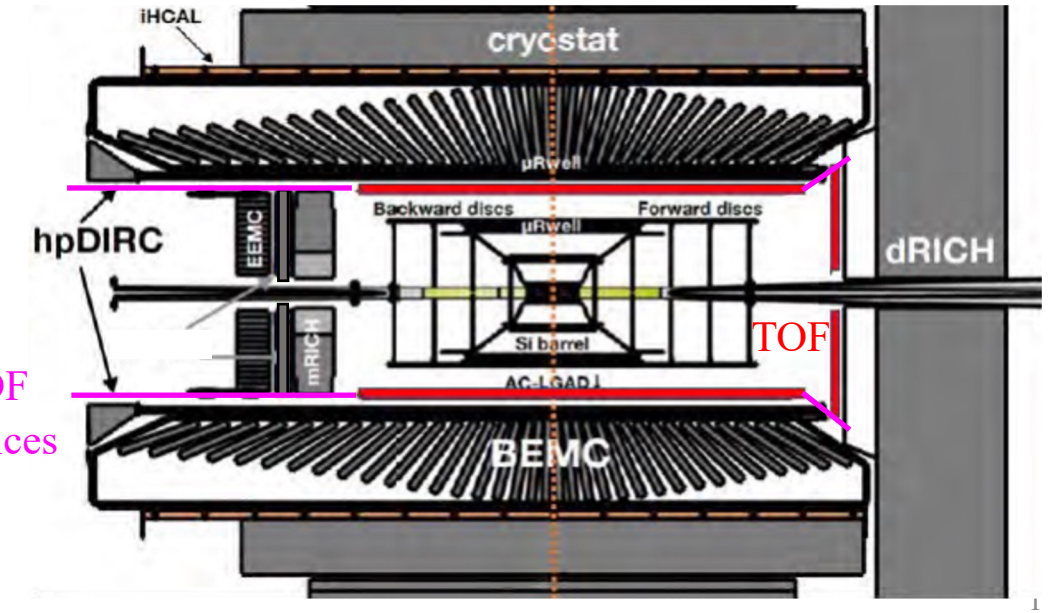
TOF Integration Status

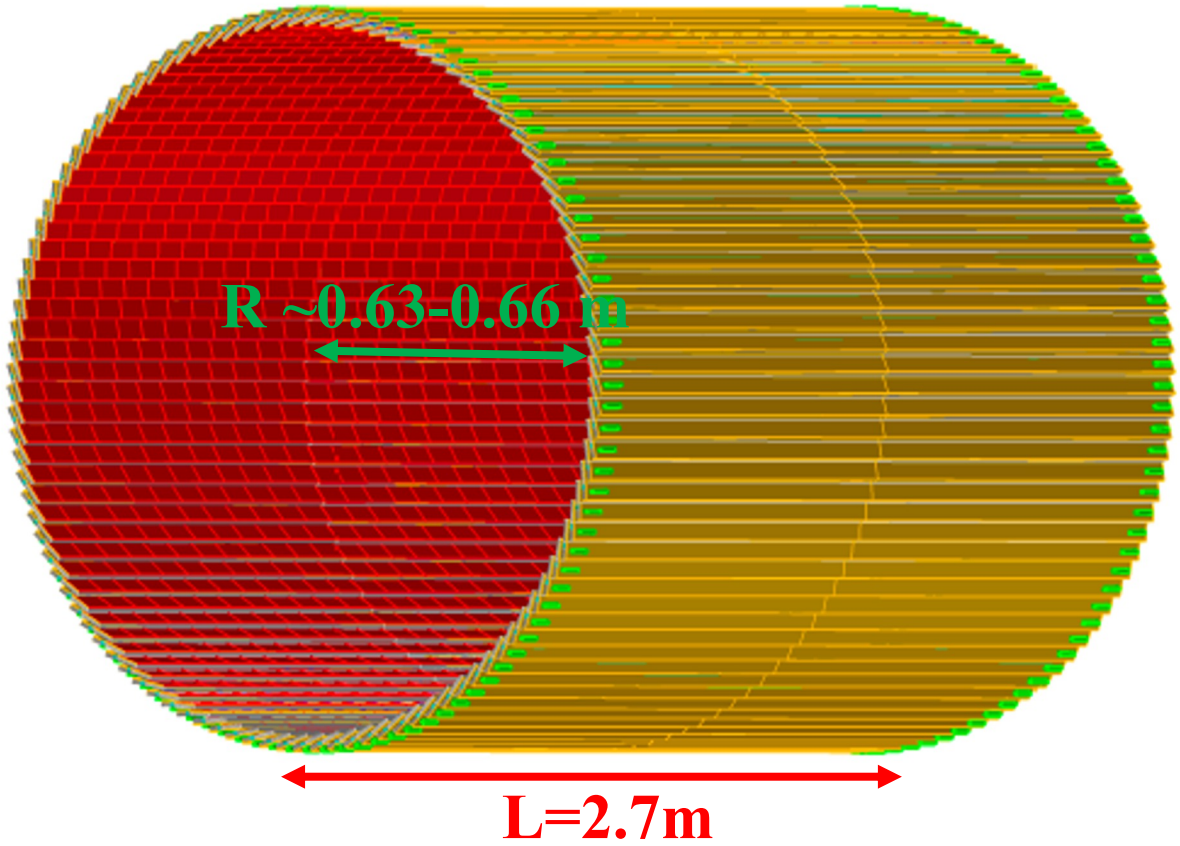
- How is your system integrated with the overall ePIC design, i.e., what is the envelope occupied, is there possibly overlap with other subsystems, and is the design consolidated, ...
  - BToF: R=[63, 66]cm, z=[-135, 135cm]
  - FToF: R=[8, 67]cm, z=[180, 195cm]
  - No overlap with other subsystems as far as we know as of now. But will need to check possible overlap of support structure and services when they are implemented.
- How are the services integrated, i.e., readout, cooling, support structure, etc?
  - Looking into this, had initial meeting with technical team last week (Rahul), follow-up meeting in ~2-3 weeks
- Does the present technical design and implementation fulfill the YR requirements, i.e., will it stand a technical design review, and if not what is the strategy to mitigate?
  - R&D
    - BNL-IO and HPK on sensor (eRD112)
    - EICROC/FCFD/SCIPP frontend ASIC (eRD109)
    - Low mass Kapton PCB (eRD109)
    - Low-density composite material for module (eRD112)
  - PED
    - light-weight support structure (in preparation)
    - clock distribution and readout board (DAQ WG)



Barrel TOF Layout

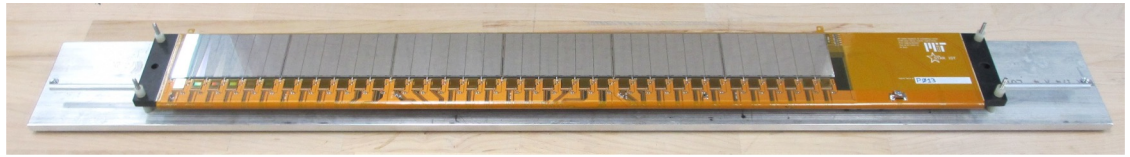
More details: https://indico.bnl.gov/event/16765/

ePIC Barrel TOF (~1% X_0)



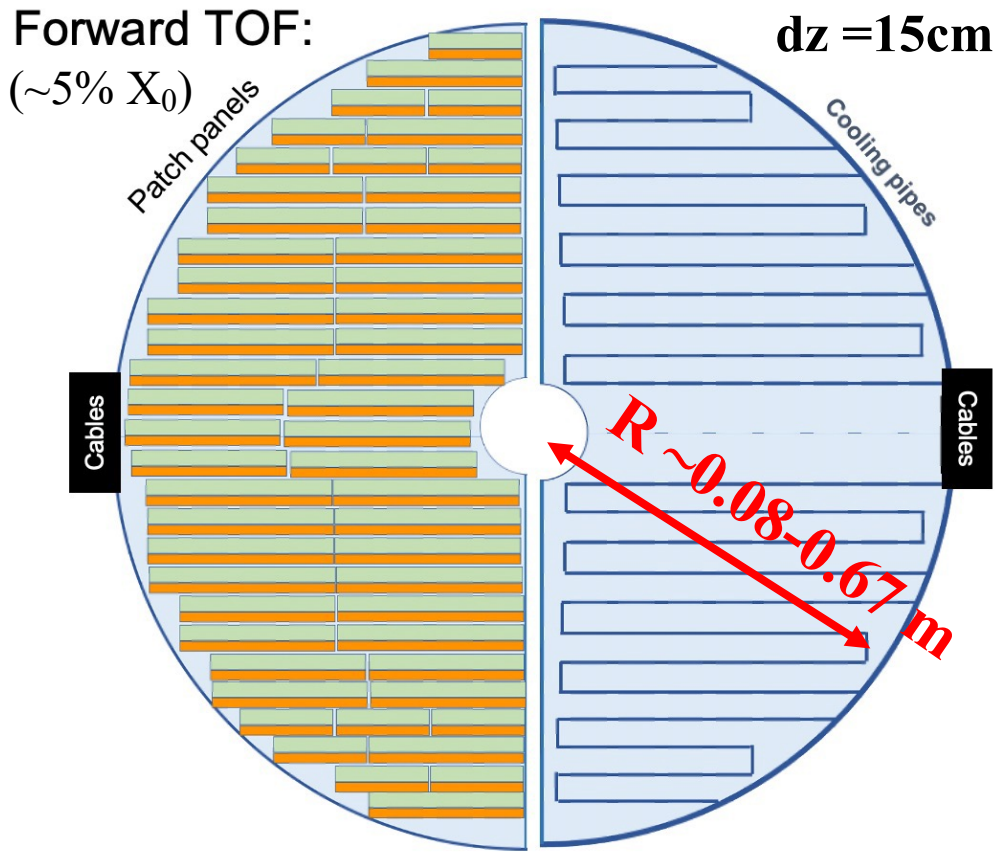
STAR Intermediate Silicon Tracker

- 288 staves, each with 32 strip sensors wire-bonded to 64 frontend ASICs on low mass Kapton flex and CF support
- Power consumption: ~4 kW for 500μm x 1cm strips (2.4 kW for ASIC, 1.0 kW for DC-DC, 0.6 kW for sensor+cable+RB)

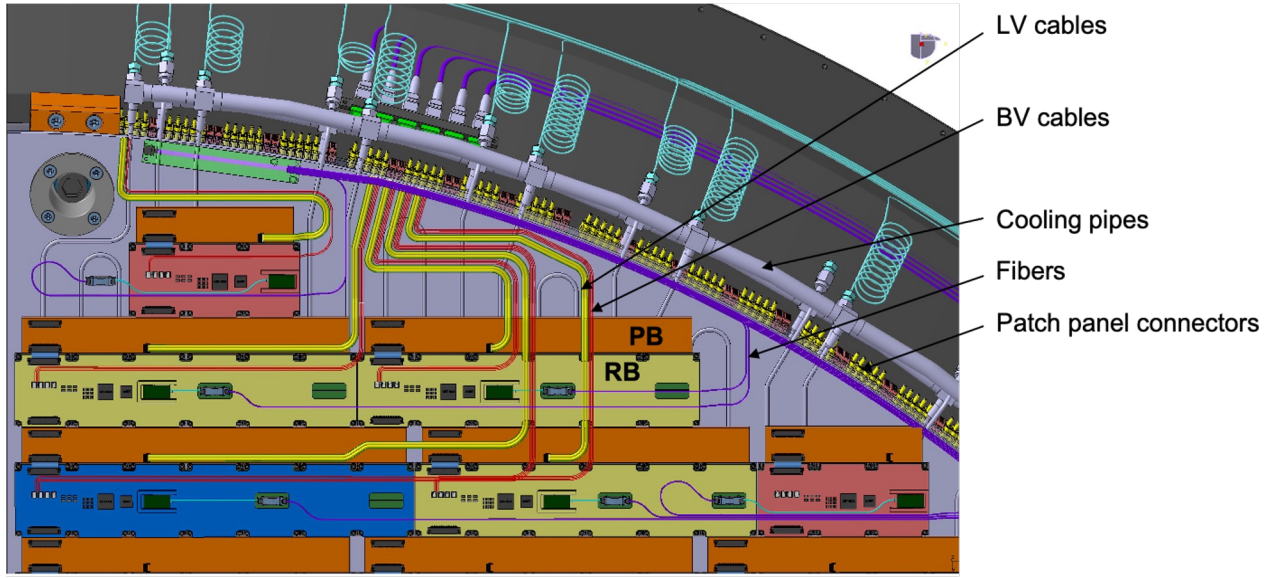


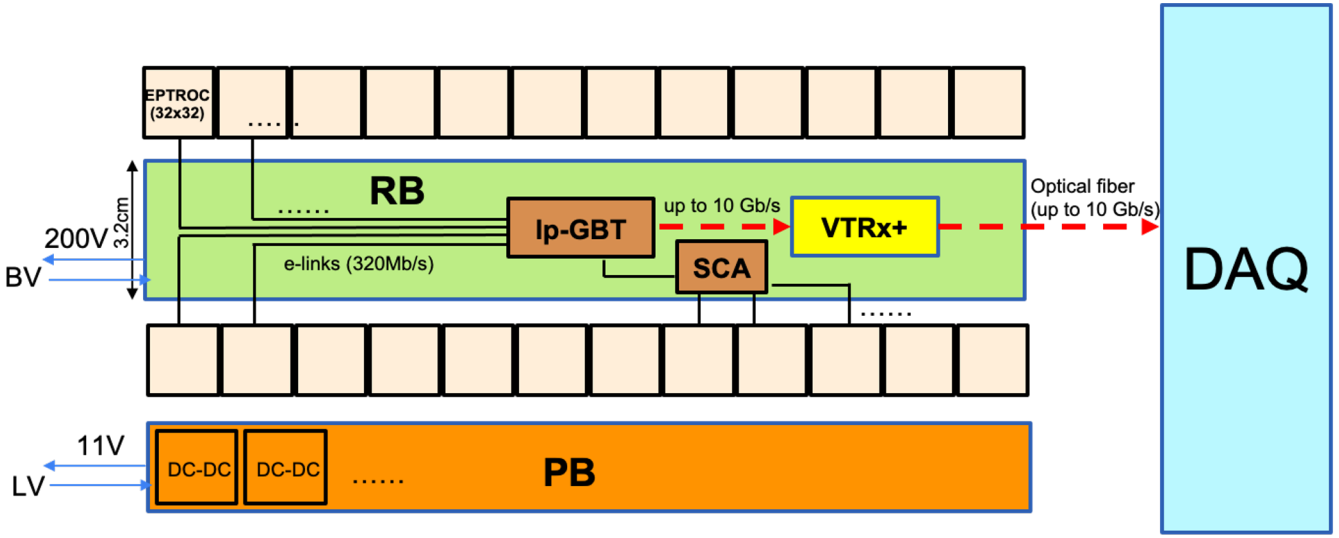
Forward TOF Layout

More details: https://indico.bnl.gov/event/17336/



CMS Endcap Timing Layer





- 212 modules, each with 24 to 96 bump-bonded pixel sensor + ASIC assemblies on Al disk
- Power consumption: 13 kW for 500x500 μm^2 pixels (6 kW for 800 x 800 μm^2)