HGCROC & EICROC Introduction

Jeff Landgraf

- There are TIC meetings planned to focus on HGCROC (July 10th) & EICROC (July 17th). Klaus asked DAQ for a short intro regarding these today, as an advertisement and introduction
- OMEGA and in2p3 have now committed considerable resources dedicated specifically to EIC ROC ASIC development. This is great news!
- eRD109 projects are also active developing and evaluating these ASICs
- Frederic Duluco (Ecole Polytechnique – CNRS) gave a recent talk regarding these chips to the DAQ WG presentation and recording available at: https://indico.bnl.gov/event/19653/
- Similar base ASICs with modifications…

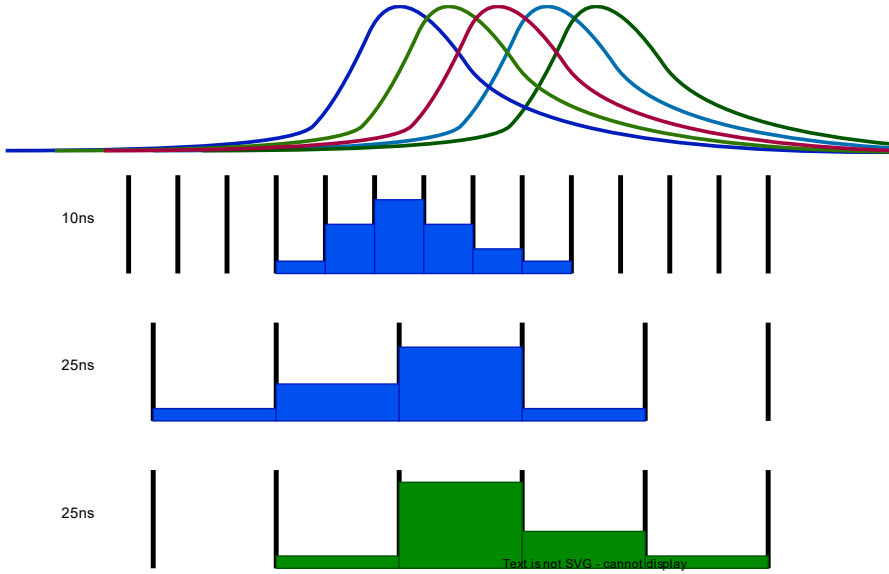
	Detector/Technology	Discrete/ASIC	Group	Awarded
A	Calorimeter	Discrete	IUCF	April 2023
B	Calorimeter	HGCROC	ORNL	April 2023
C	dRICH	ALCOR	INFN	April 2023
D	AC-LGAD	EICROC	Omega	
		FCFD	FNAL	
		Barrel L-M Serv. Hybrid	ORNL	April 2023
		3rd Party Evaluation	UCSC	
E	MPGD/µRWell	SALSA	CEA	
			USP	

HGCROC

- HGCROC is a waveform digitizing ASIC aimed for digitizing the SiPM readout of the Calorimeters.

- 72 Channels version. HKROC exists with auto-triggered design but half the channels

- The main challenges for EIC
  - Digitization Clock 40MHz rather than 100MHz
    - Corrections for phase relative to BX
    - Can hits be resolved to a BX? (Do they need to be?)
    - Clock could be increased to 200MHz, but at the expense of timebin reduction (7→3-4), power use, and possible deadtime
  - 10 Bit resolution, so dynamic range may be an issue
    - Potential non-linear (or range dependent) pre-amp
    - Potential TOT scheme
  - “Could be converted to auto-triggered design”

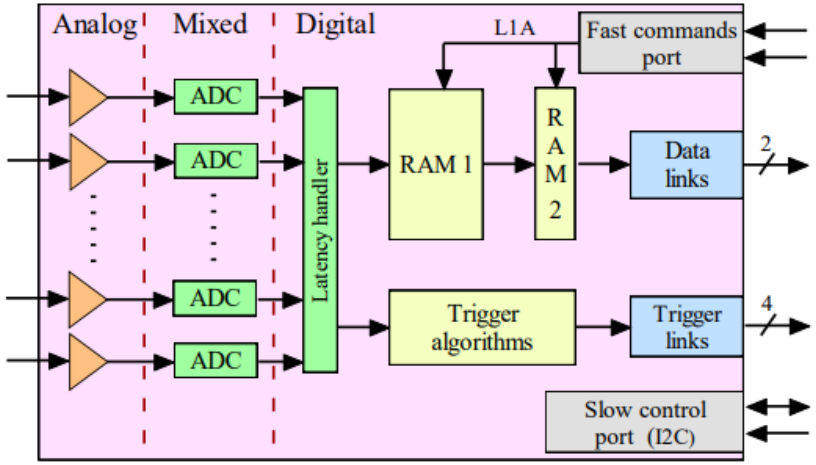


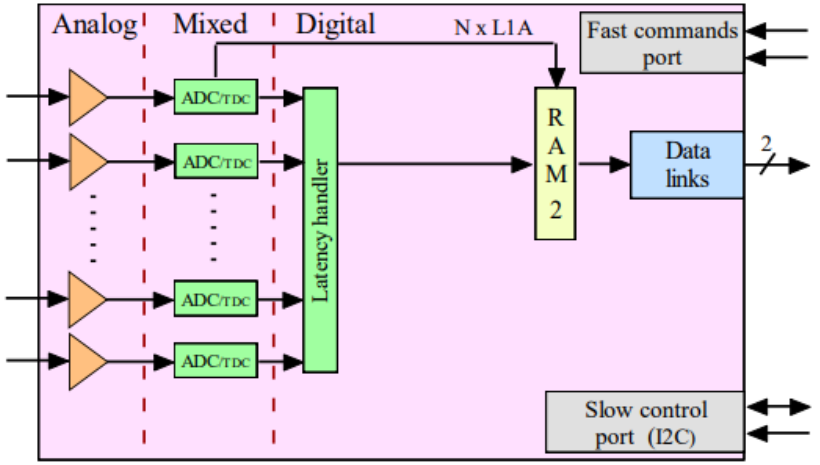
HGCROC → EGCROC-EIC

What HGCROC-EIC could look like

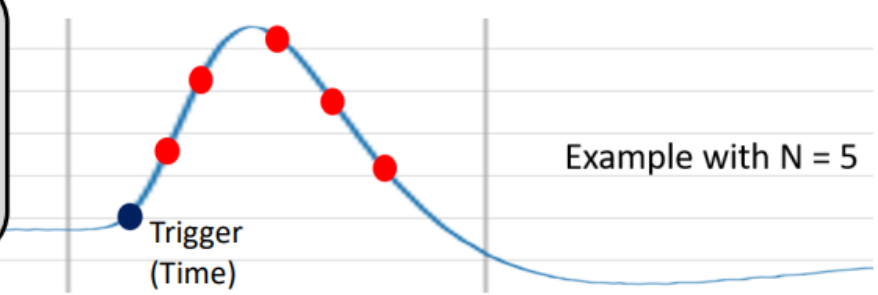
Omega

- HGCROC / H2GCROC (for SipM) with the integration of auto-triggering
  - Below is an calorimetry structure (not pixel like ALTIROC or EICROC but interfaces are similar)





- Each event passing the threshold is readout
- Check Hit rate
- Auto-trigger with N "samples" (1 to 7)
  (Same as HKROC)



EIC 2023

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(Frederic's talk)

EICROC

- EICROC is a TOA/TOT threshold based on the ALTIROC aimed for AC-LGAD readout (and possibly the HRPPDs). This could be used in the TOF, eTOF, RP, OffM, pfRICH, DIRC, B0,
- High Resolution, Pixelated readout: ~20ps timing resolution
- Is Clock 40MHz? If so, clock still must be synchronized to EIC BX clock, but digitization issues for HGCROC not as relevant because the only issue is the numerical translation between TOA values under different clock references

(Frederic's talk)

ATLAS HGTD: ALTIROC ASIC

- **ALTIROC** (Atlas Lgad Timing Integrated ReadOut Chip)
  - Design under OMEGA responsibilty - Collaboration CERN Geneva, LPCF Clermont-Ferrand, IFAE Barcelona, SLAC Stanford, SMU Dallas
  - 20 ps timing silicon timing detector for jet identification and pileup rejection
  - ⇒ Pixel ASIC for precise timing measurements
    - **Qmin/Cd ~ 500 µV** with **Cd ~4 pF** (1300 x 1300 µm2) and **Vth min= 2 fC** to be compared with other timing ASIC for which Qmin/C > 2 mV with Cd ~ 50 fF (50 x 50 µm²) and Vth min = 0.1 – 0.2 fC
  - ⇒ Mix of requirements specific to calorimetry and some of the requirements specific to pixel ASICs for trackers
  - ⇒ Mix of Analog on Top design for the floorplan and analog performance + Digital on Top design for digital part (70% of the ASIC)
  - ALTIROC2 : first 225 channels full matrix LGAD readout chip with **1 GHz** preamplifier **4 pF** detector capacitance = **new territory in HEP**
- See details in https://indico.cern.ch/event/1127562/contributions/4904499/attachments/2511666/4317317/ALTIROC2_ATLAS_HGTD.pdf