

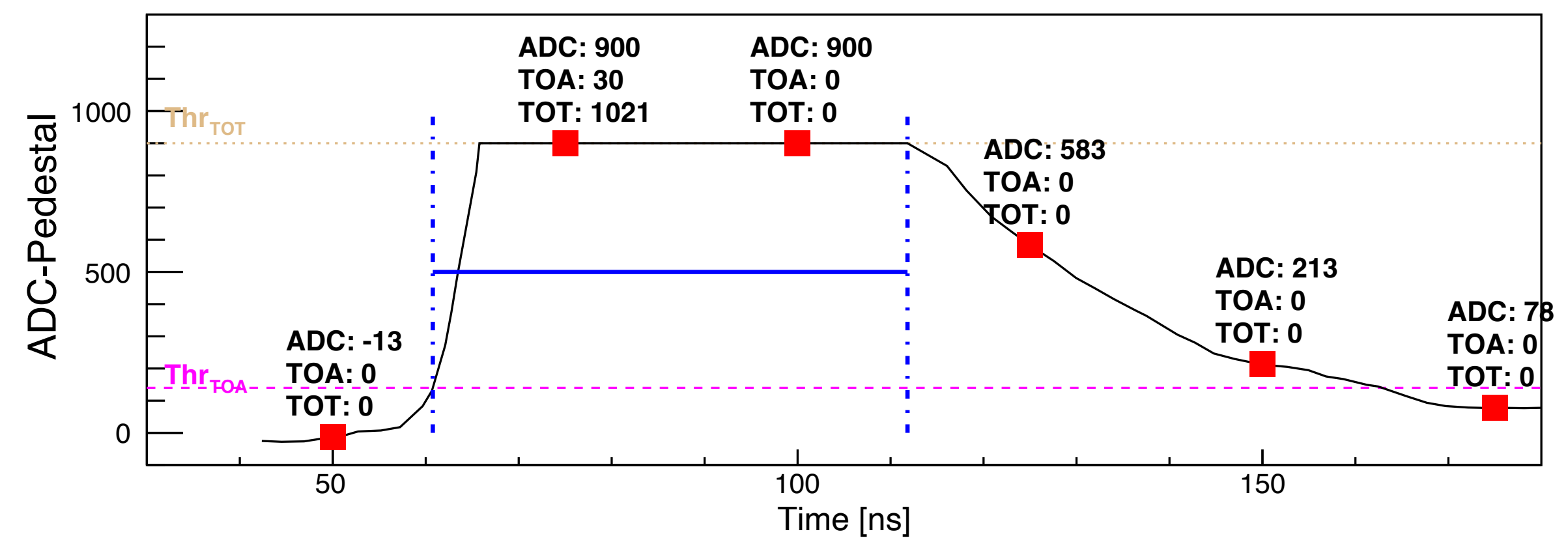
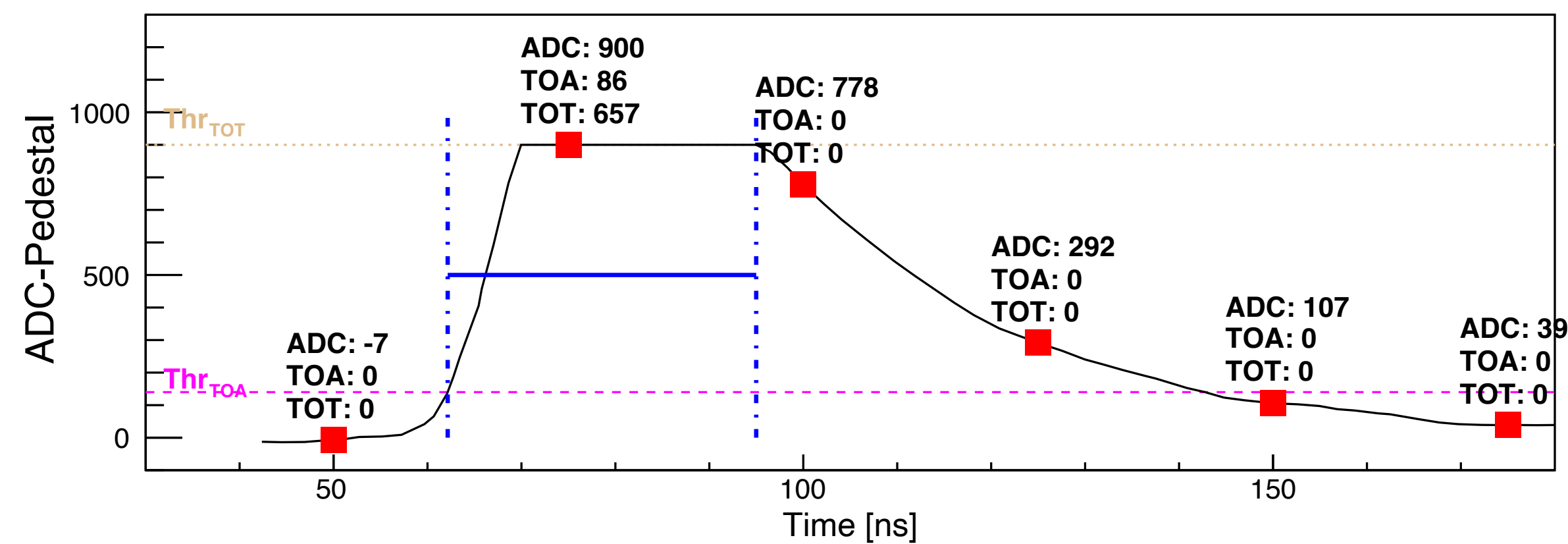
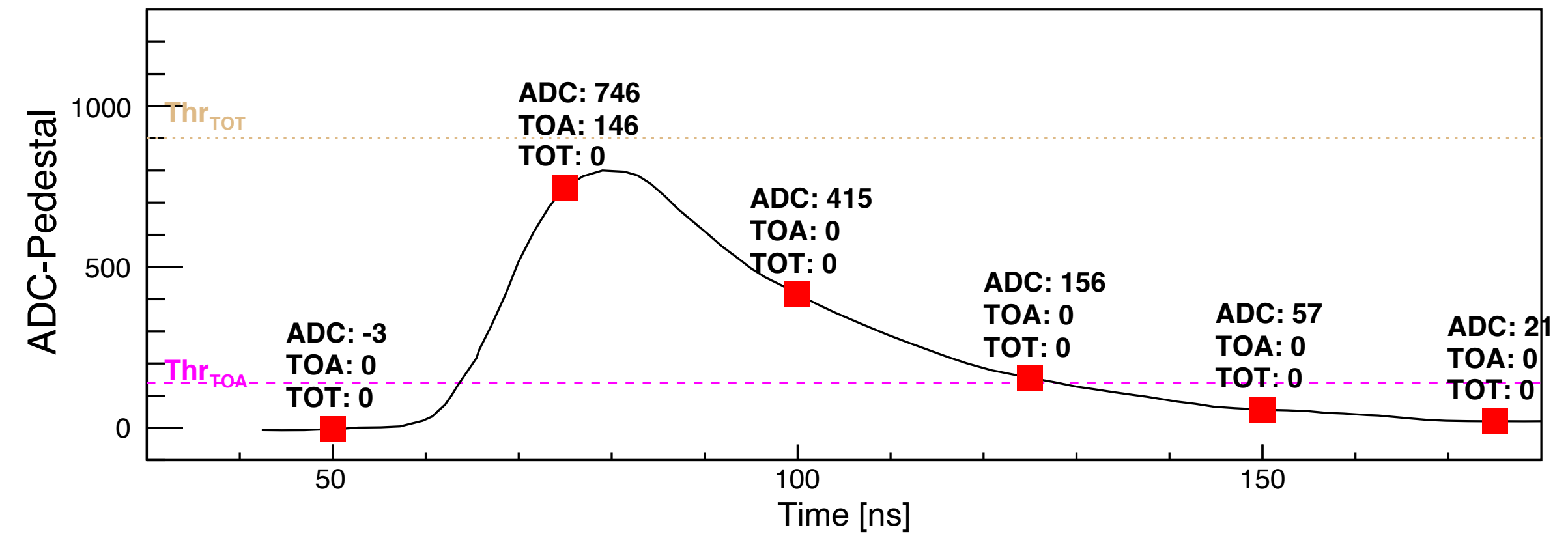
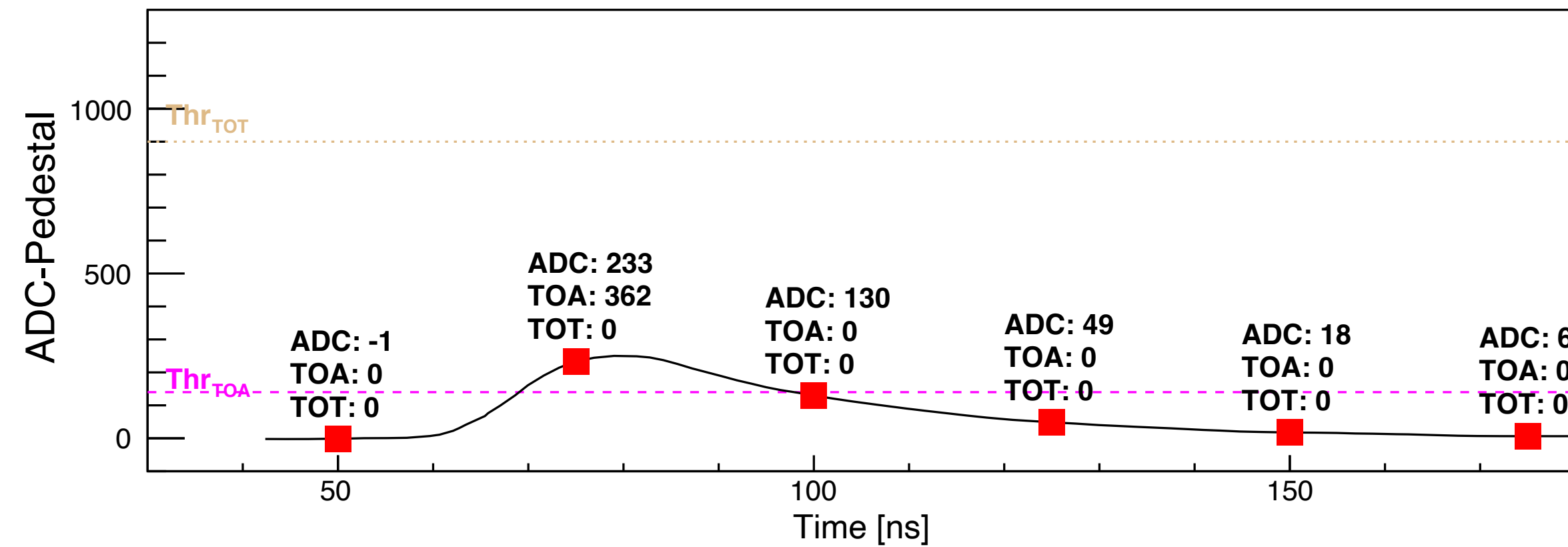
H2GCROC3 → ePIROC

Norbert Novitzky
(ORNL)

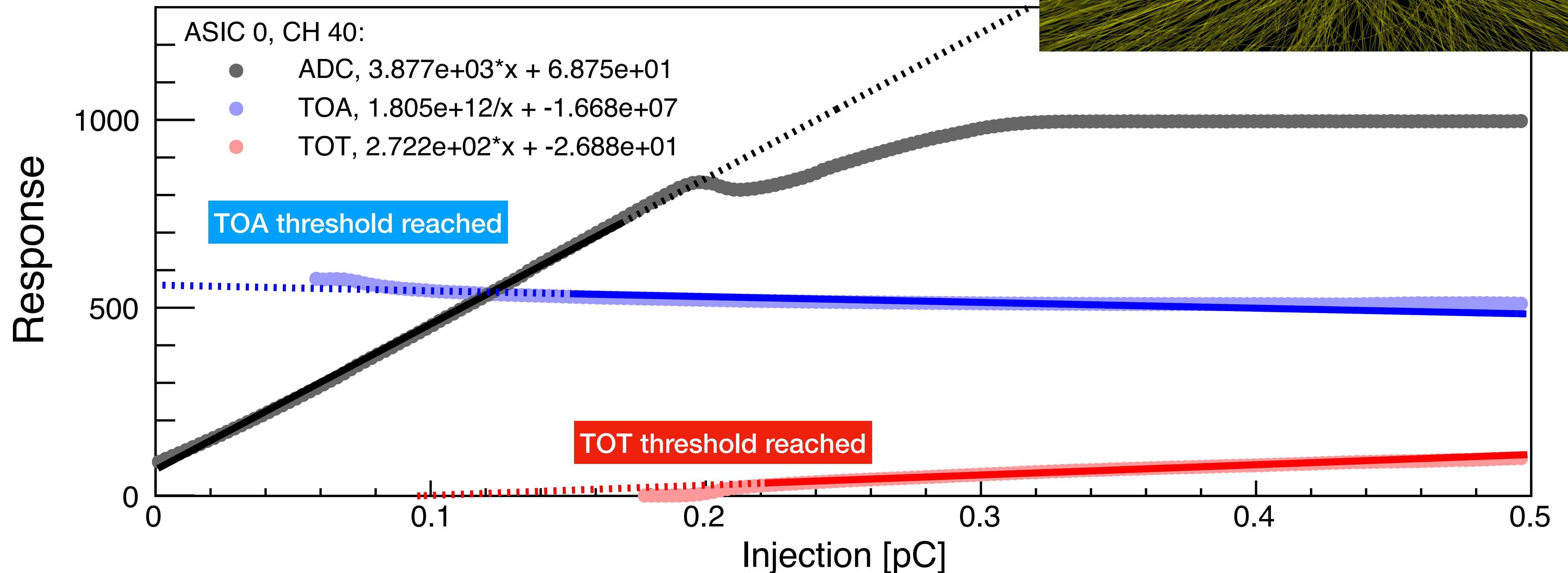
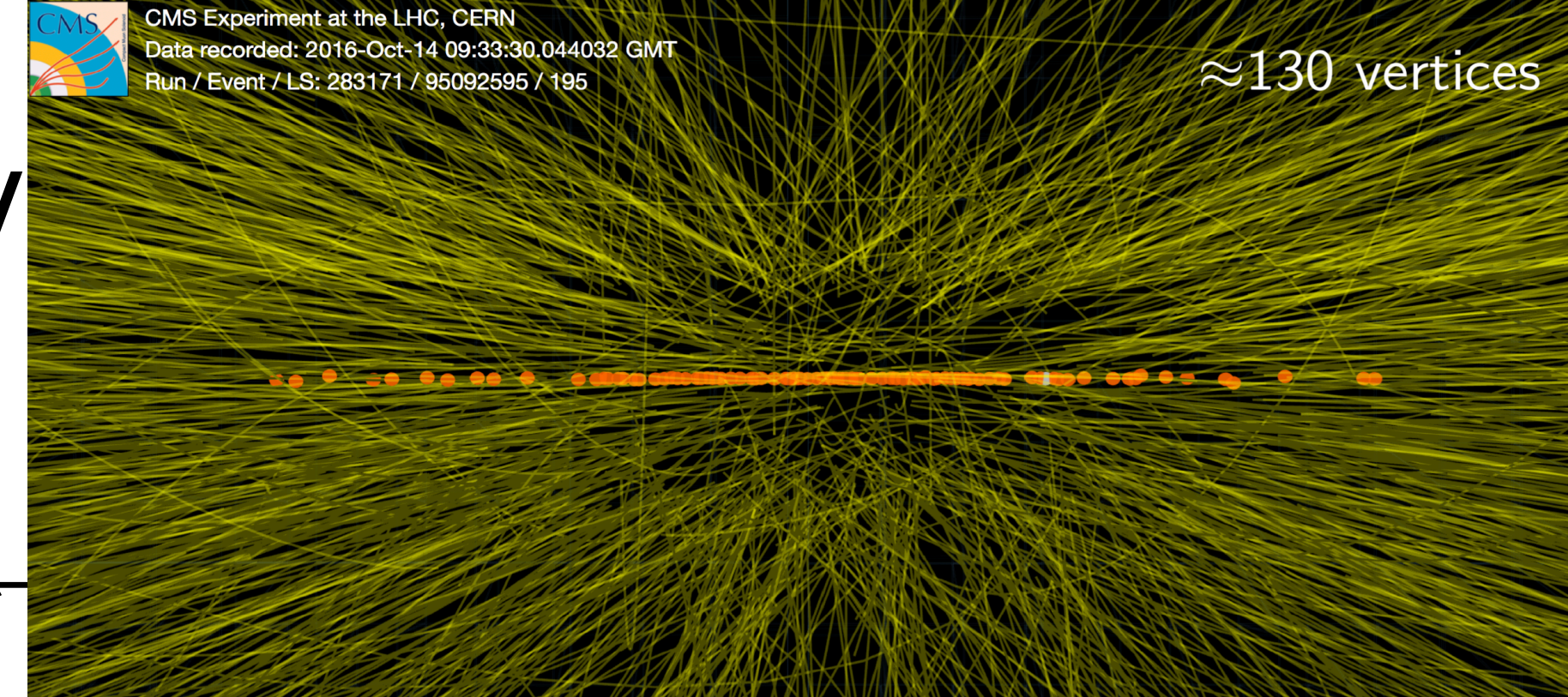
Explaining the ADC/TOT combination

HGCROC is not a waveform sampling chip:

- It sends a 32-bit word for each channel each Bunch Crossing (BX) 10-bit ADC, 10-bit TOA, 12-bit TOT:
 - Format explained in the next slide
- eRD109 is looking into the consecutive BX readouts and the shaper configurations



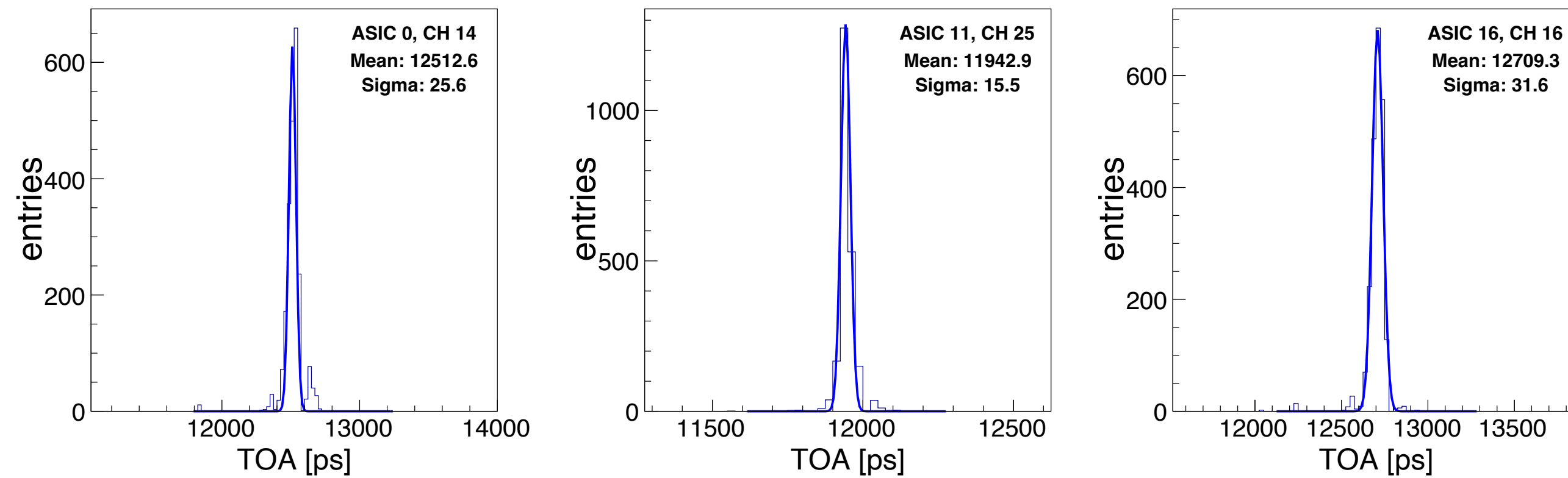
CMS/LHC strategy is looking into one BX only



At CMS they expect up to 200 events each bunch crossing (2800 BX in one ring):

- Important to distinguish clusters in the pile-up events (timing is 15-35 ps, TOA)
- They focus on 1 single BX readout

Real measurement of the timing distribution in HGCR0Cv2



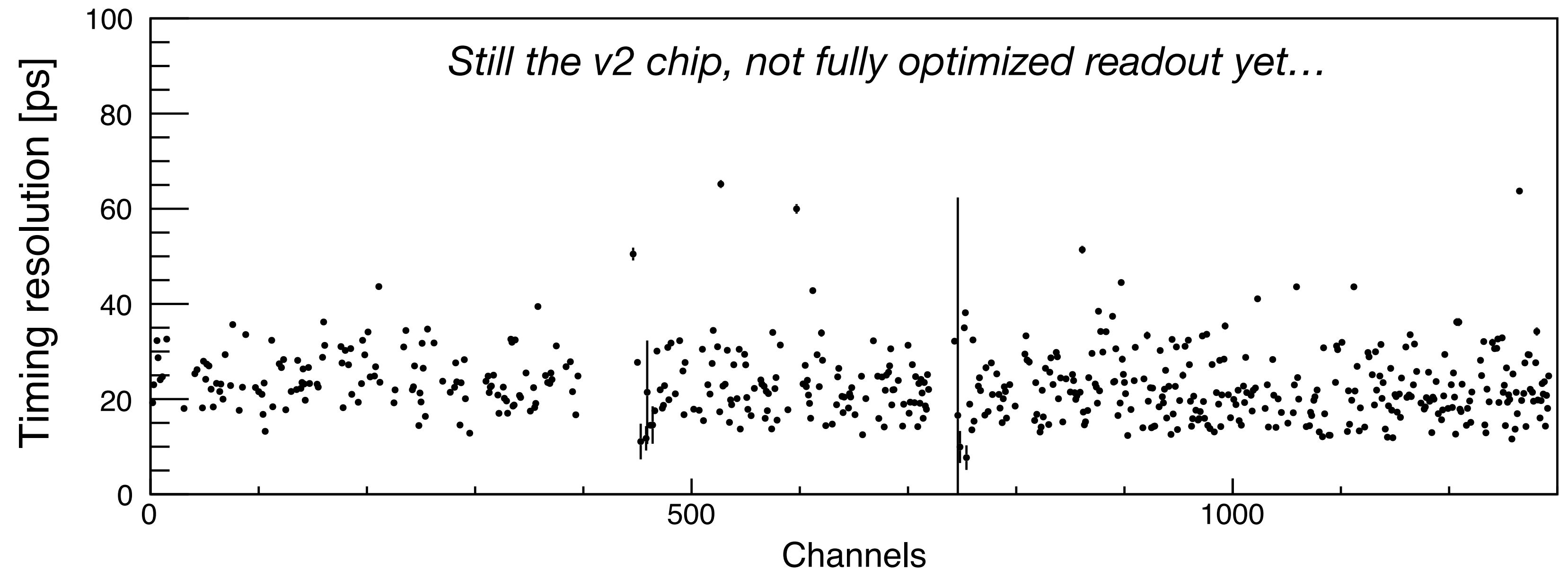
Some examples of the TOA timing distribution

Real data obtained with a prototype used in ALICE-FoCal:

- Older version of the chip
- Realistic resolutions with noise obtained from each channel

Resolution extracted from 18 ASICs in series:

- Run by a Xilinx Ultrascale FPGA
- 18 in series (from 30cm to 10cm distance from FPGA-ASIC)
- Extracted the timing resolution where I could: 15-35 ps in general



Readout formatting (as of now)

Address	Bytes (Rx)	ChipID	HalfID	FPGA counter	Header	CMN0	Ch0	Ch5
110928.655	Bytes (Rx)	A5 14 00 00		27 30 2B C7	5A AB E7 05	00 00 98 0C	08 F2 40 00	0A A2 A8 00
110928.656	Bytes (Rx)	A5 14 00 01		27 30 2B C7	0B 62 D8 00	0A B2 B4 00	0B 52 D4 00	09 82 5C 00
110928.656	Bytes (Rx)	A5 14 00 02		27 30 2B C7	0B D2 F4 00	0C A3 24 00	0C 33 04 00	0B 72 D8 00
110928.656	Bytes (Rx)	A5 14 00 03		27 30 2B C7	0B A2 DC 00	0B F2 FC 00	0A 52 94 00	0B E2 FC 00
110928.656	Bytes (Rx)	A5 14 00 04		27 30 2B C7	0B 92 E4 00	0C 43 18 00	0A C2 BC 00	0B 52 BC 00
110928.657	Bytes (Rx)	A5 15 00 00		27 30 2B C7	5A AB E7 05	00 00 04 17	09 22 48 00	08 F2 40 00
110928.657	Bytes (Rx)	A5 15 00 01		27 30 2B C7	09 C2 70 00	0C 93 24 00	0A 62 A0 00	08 D2 38 00
110928.657	Bytes (Rx)	A5 15 00 02		27 30 2B C7	09 72 5C 00	08 82 24 00	09 F2 78 00	0A B2 AC 00
110928.657	Bytes (Rx)	A5 15 00 03		27 30 2B C7	0A 72 9C 00	08 E2 38 00	0A 32 84 00	09 92 68 00
110928.657	Bytes (Rx)	A5 15 00 04		27 30 2B C7	08 D2 34 00	07 B1 E8 00	09 D2 74 00	D4 18 A0 2D

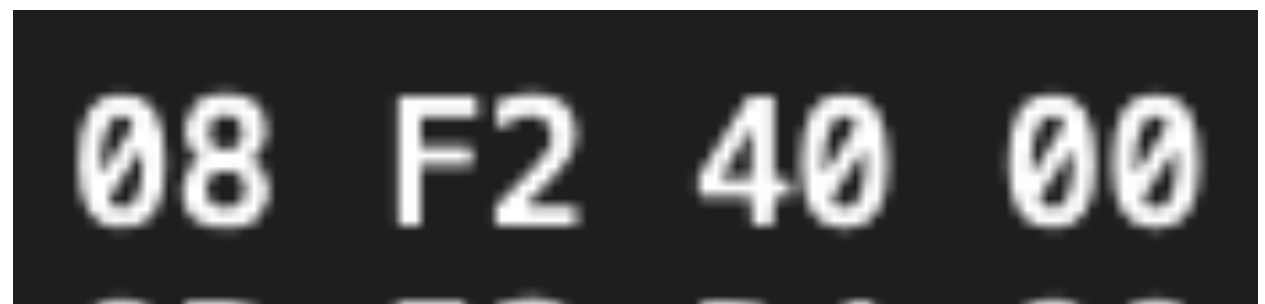
Software counter

HalfID

Ch71

CRC32

Ch0

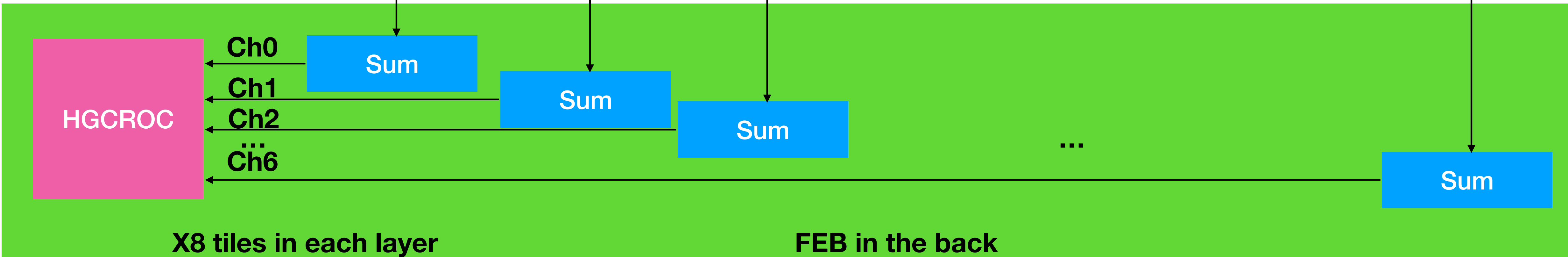
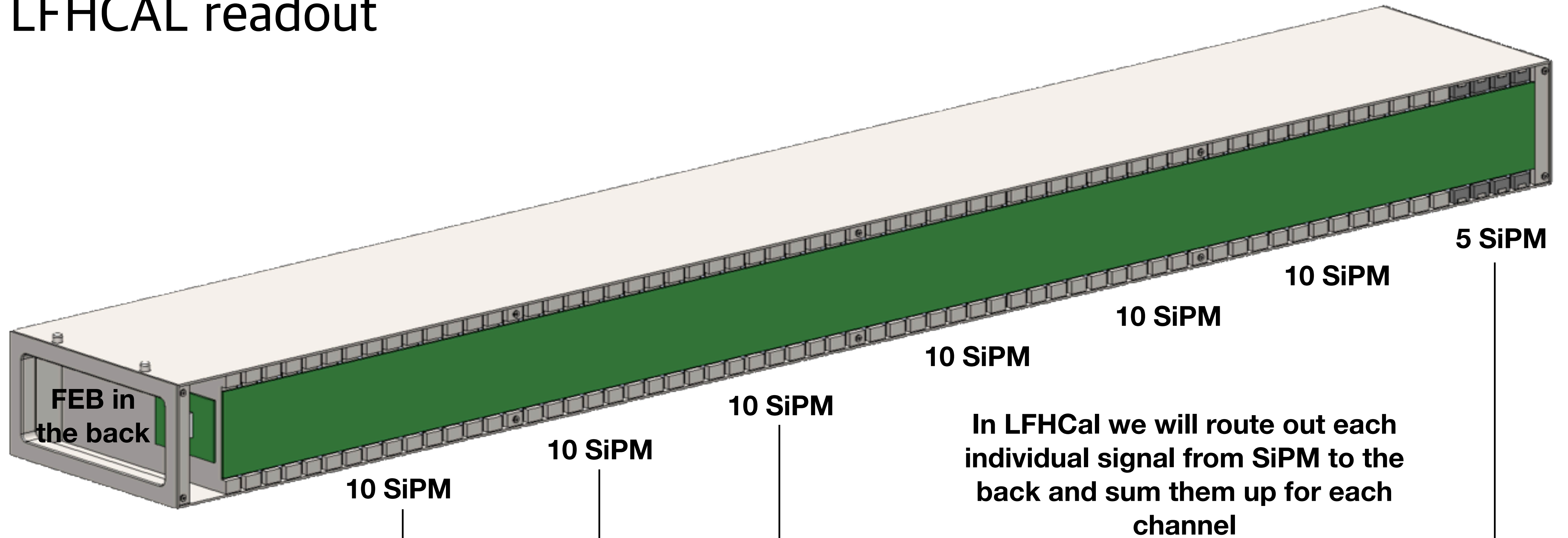


0 0 0010001111 0010010000 0000000000
 Tc Tp ADC(BX-1) ADC(BX) TOA(BX)

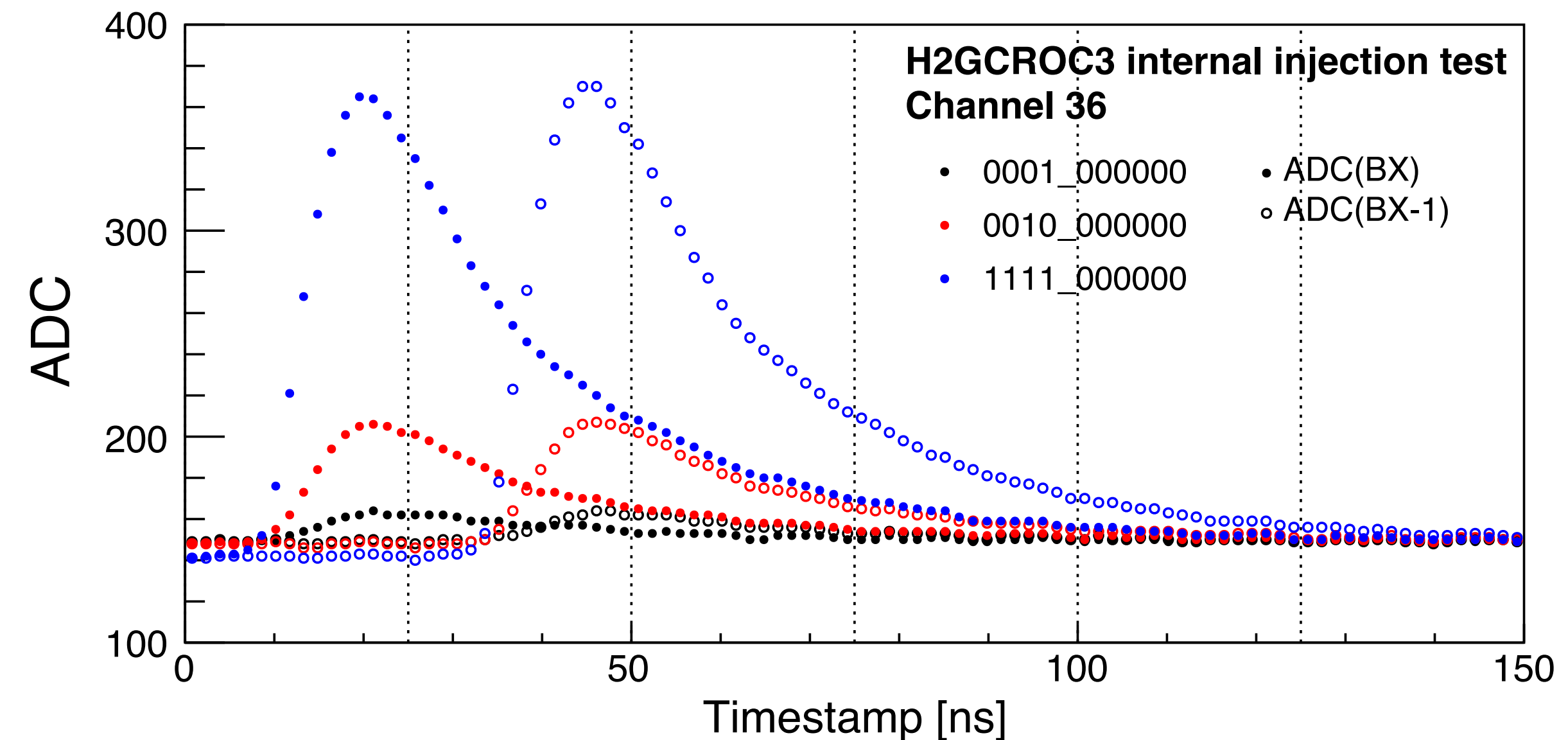
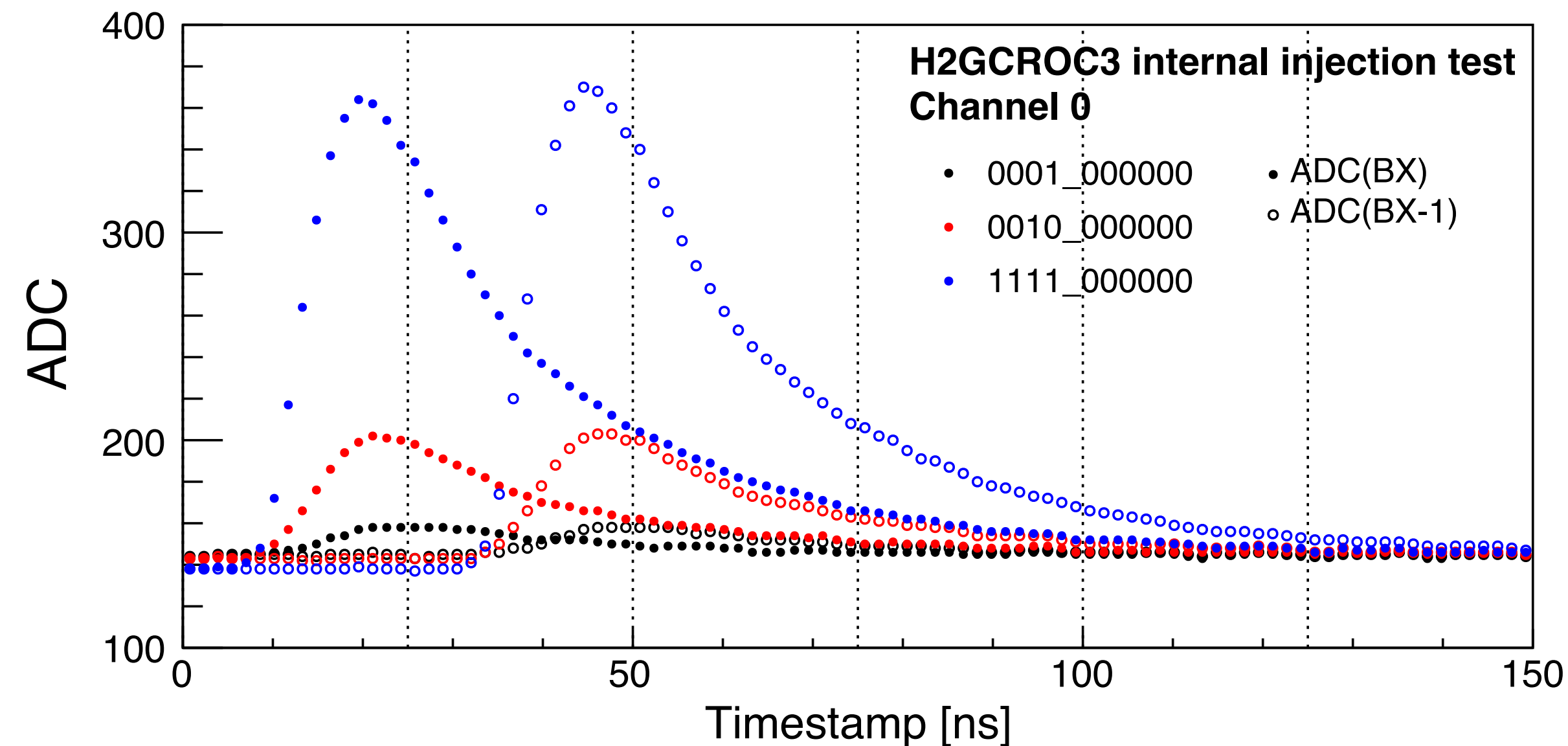
Decoding from the documentation

	ADC (BX-1)	ADC (BX)	TOT (BX)	TOA (BX)	Charge collection	Data type
1	x	x		x (=0)	Q < TOA_thr AN	Normal
2	x	x		x	Q < TOT_thr AN	Normal
3	x		x	x	Q > TOT_thr AN	Normal
4		x	x	x		"Characterization"

LFHCAL readout



First results in ORNL



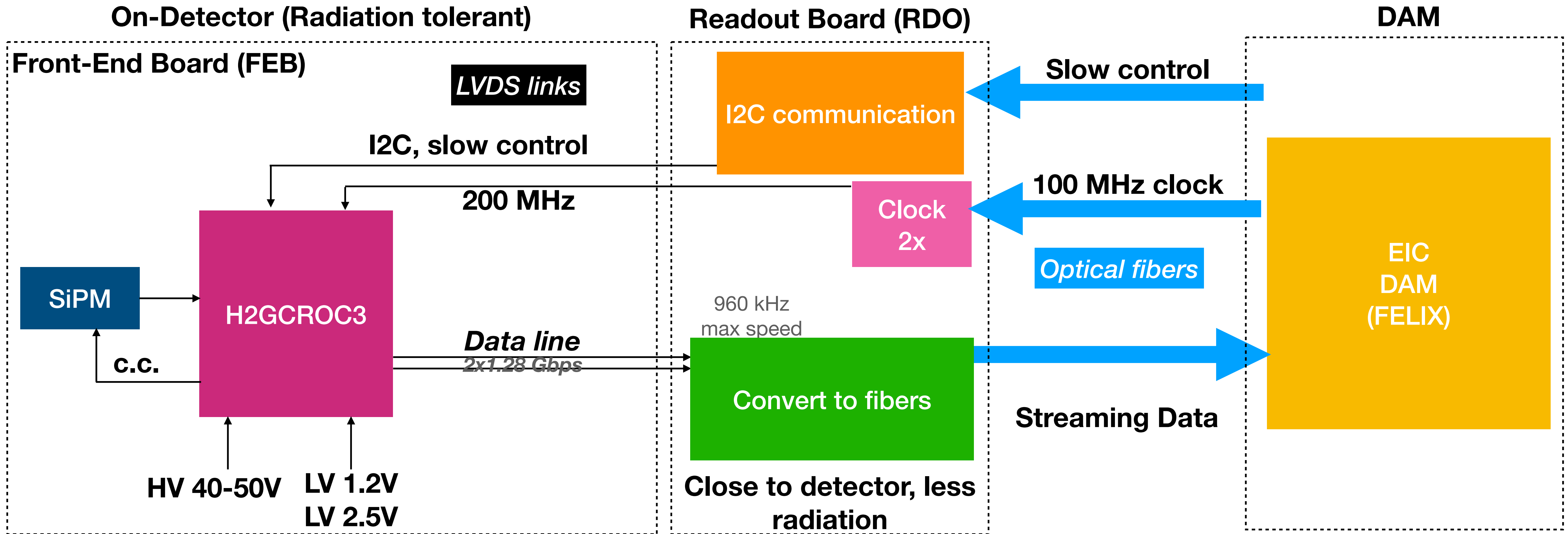
Very first results on the internal injections on 2 channels in H2GCROC3:

- Still need the full scan of different gains
- High/Low range injection, plus 2.5V injection (low injection was done only)
- Working on the algorithms for full calibration of the chip
- Collecting a bunch of questions/feedback to Omega

In parallel:

- By end of July (hopefully) first PCB layout of the 2xH2GCROC3 prototype will be submitted
 - Input will be compatible with CAEN A5253 board

LFHCaI readout hierarchy (after the upgrade)



Data propagation from the detector to the EPIC DAQ system:

- The H2GCROC3 requires the L1 trigger for readout, with the maximum speed of 960 kHz
- The expected hit rate in **one channel of LFHCaI** is up to 50 kHz:
 - With possible 4 sample readout we would reach a maximum of 200 kHz
 - Streaming readout towards the EPIC DAQ system

Plans and thoughts

PARIS-Omega:

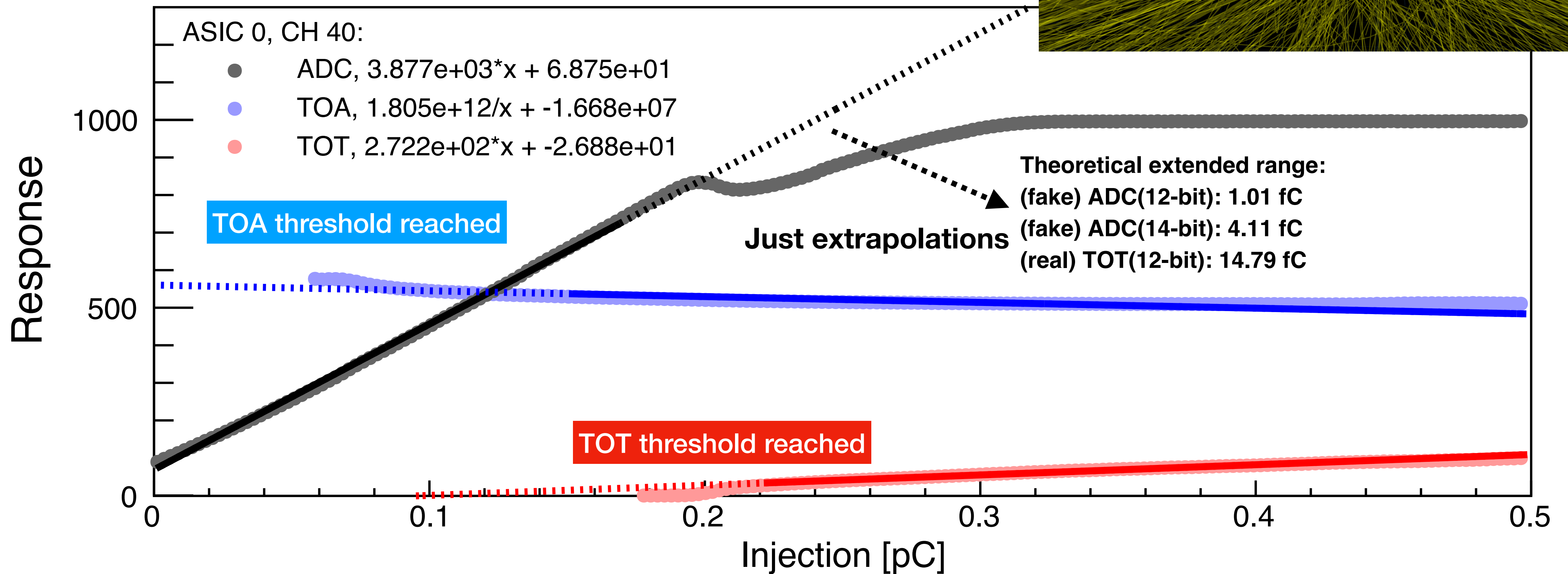
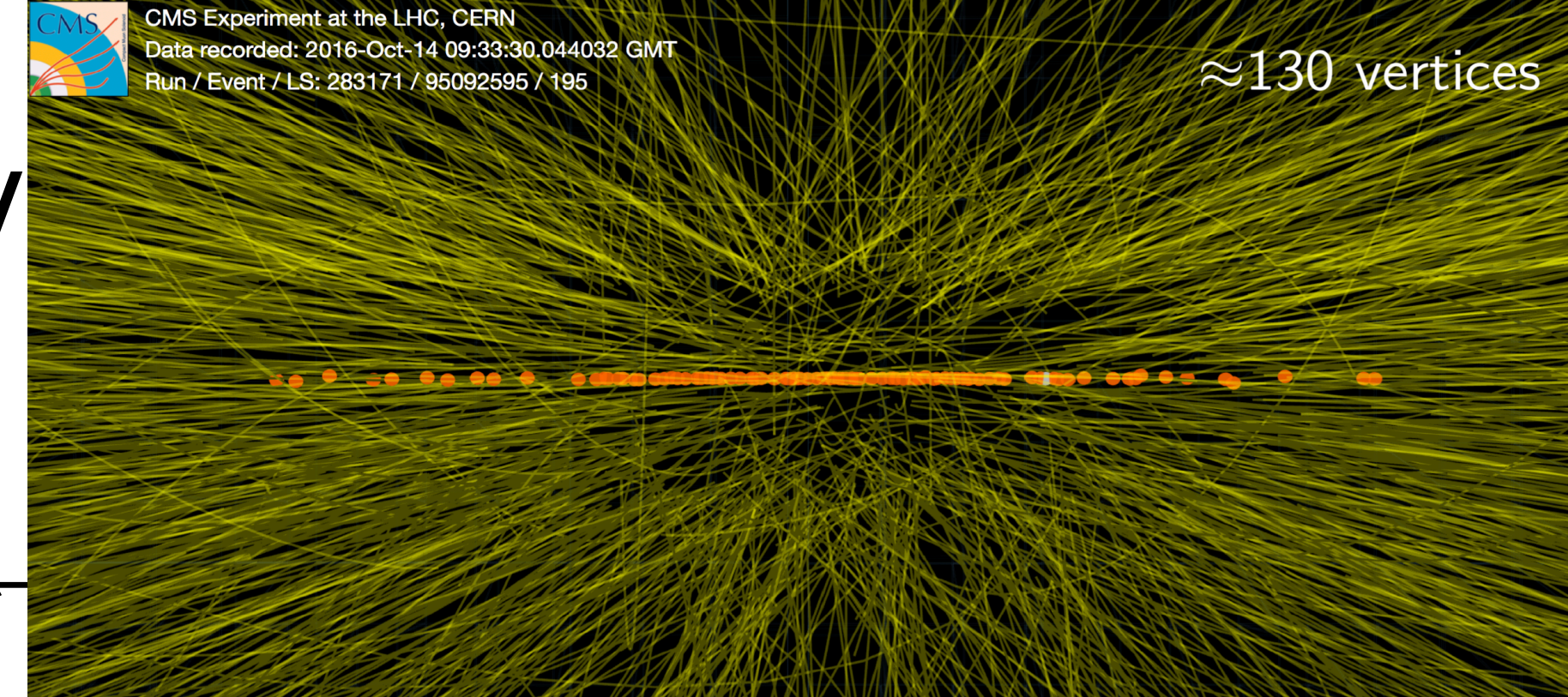
- 200 MHz clock input (or better 98.5x2) for EIC and it would convert it inside to 1/5th
- Self-triggering like HKROC
- TOT nonlinearity fix at threshold
- I2C fixes:
 - We had some troubles with the stability of the I2C module
- Number of data lines:
 - if there is a lot of hit multiplicity and we would need faster readout (deeper RAM2)

https://indico.bnl.gov/event/19653/sessions/6335/attachments/47872/81221/FD_230606_ROC4EIC_introduction.pdf

ORNL:

- Initial (first) prototype to be available in September this year:
 - Input will be compatible with the A5253 from CAEN (then we can always hook up a CAEN commonly used by different groups now)
 - 2 HGCROCs (144 channels in total)
 - KCU105 for readout electronics (firmware is ready from the testboard)
- Test the Samtec cables for data transmission, while using it also for LV/bias, 200 MHz clock and I2C communication
- Sum-up module for the FEB to sum up multiple SiPM outputs:
 - This depends on each calorimeter (some use up to 16 SiPM in one channel)
 - Different capacitance of the inputs has to be checked (or passive component to fix it)
- Implement the readout for each calorimeters.
 - LFHCal as baseline for Sept/Oct testbeam already
 - Implement readout to barrel HCal (from sPHENIX prototype) and backward HCal prototypes.
 - Backward HCal prototype?
 - BarrelECal: existing prototype from GlueX
 - Backward and Forward ECals can be tested also

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