Towards HGCROC for EIC

(focused on ASIC changes)

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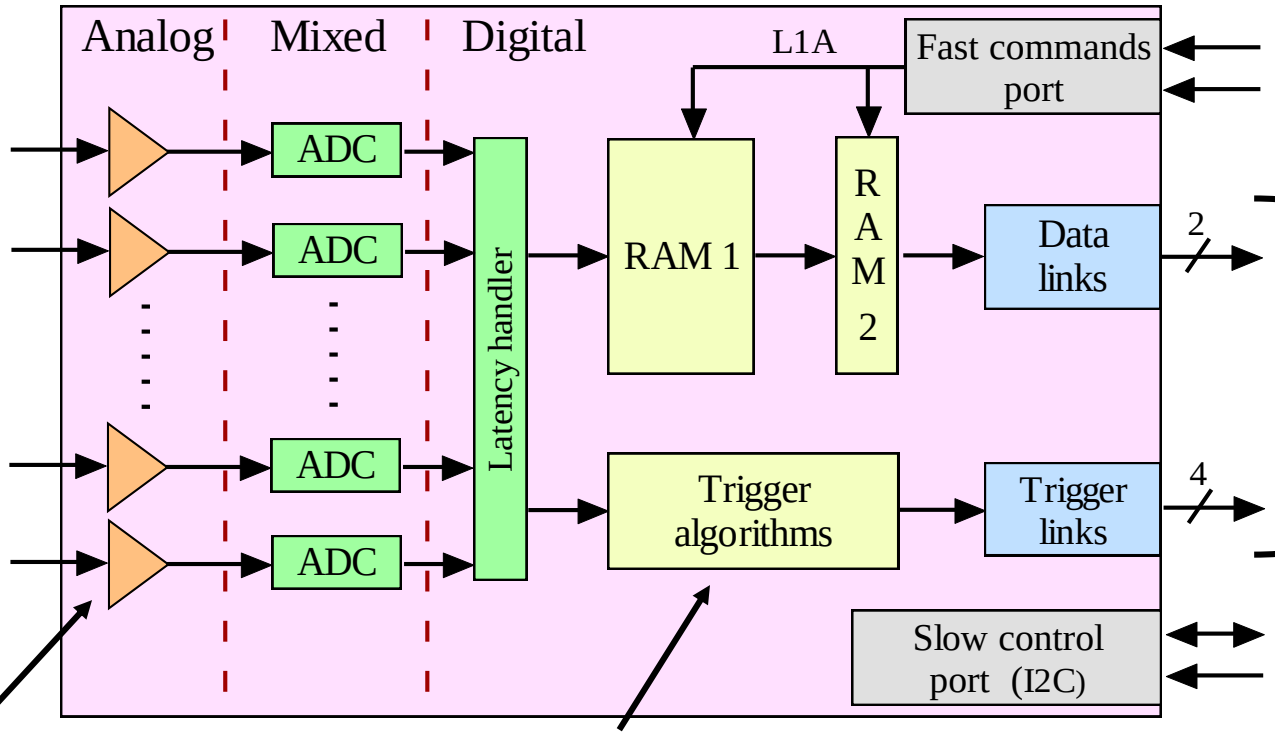
ROC chips main structure

- HGCROC / H2GCROC (for SiPM) and ALTIROC are LHC colored ASICs (external L1 trigger)
  - Below is an calorimetry structure (not pixel like ALTIROC or EICROC but interfaces are similar)



Dedicated fast command interface : calibration pulses, external L1 trigger.

Data and trigger serial links with CLPS signaling (LpGBT @ 1,28 Gbps)

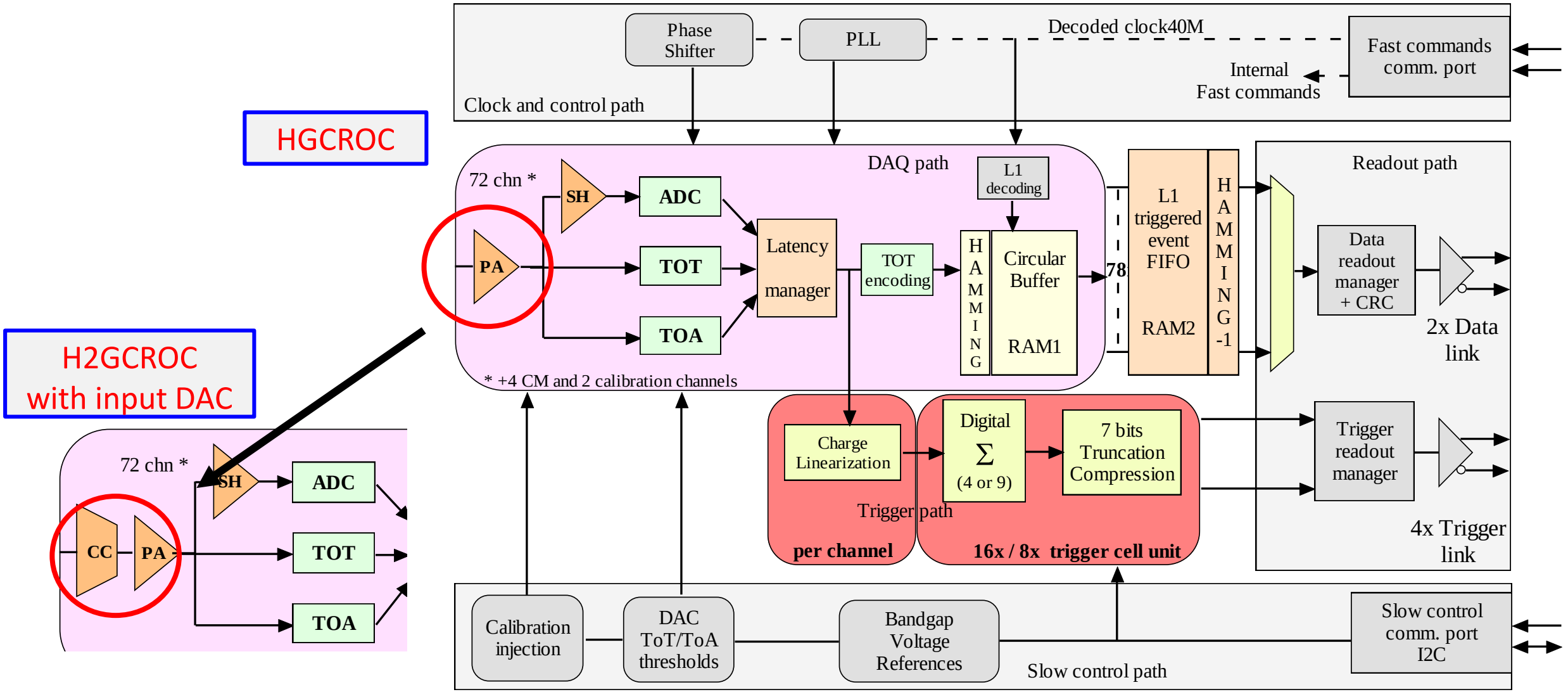
Analog front-end specific to sensor

LHC-like structure :
Ram1 for data storage
Ram2 for L1 accepted events

I2C interface to load the ASIC parameters (slow control interface)

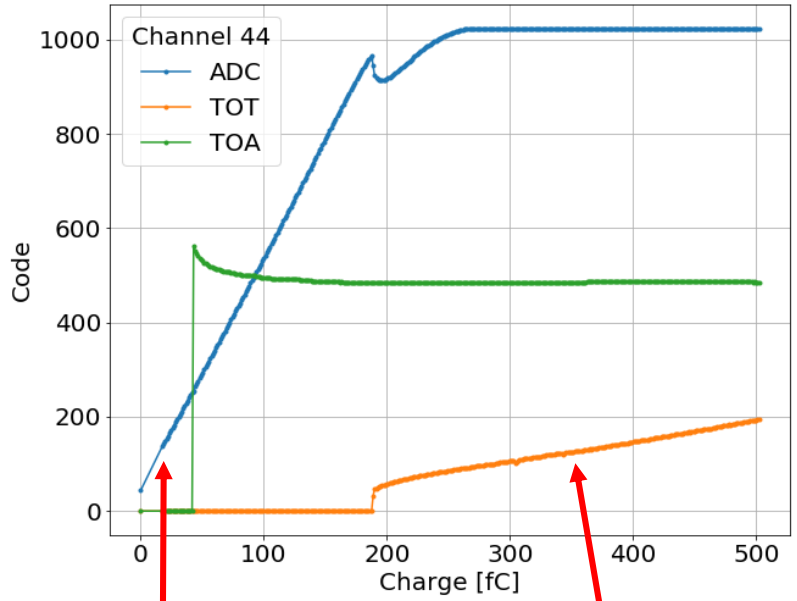
HGCROC (Si) versus H2GCROC (SiPM)

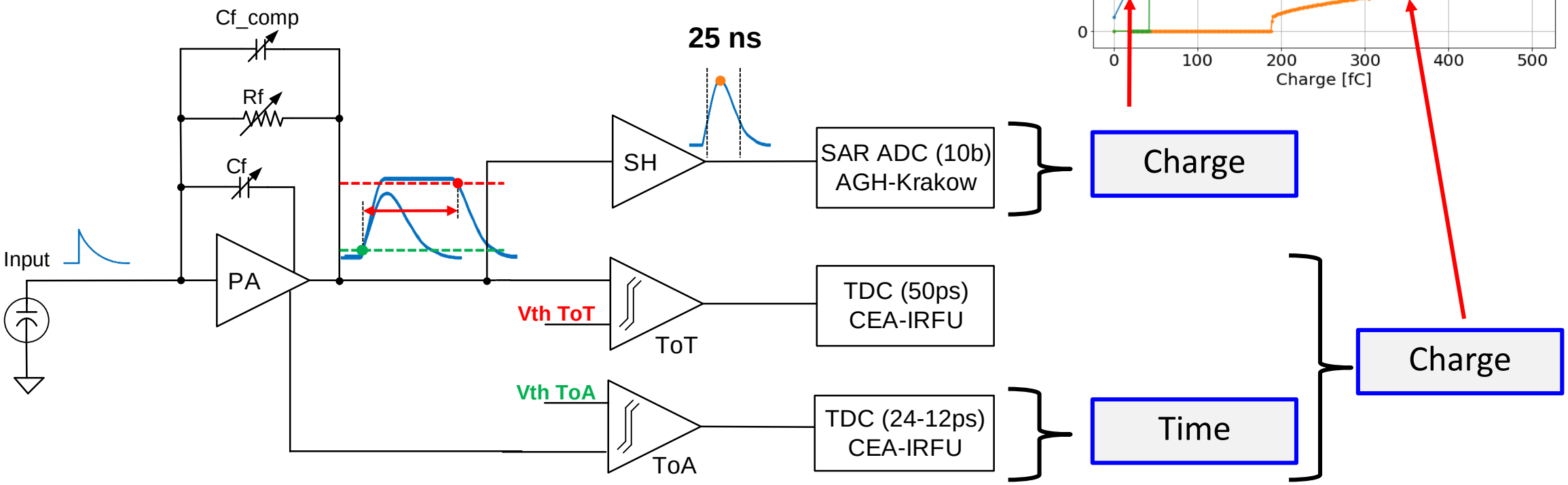
- Same back-end (ASIC digital processing) – Specific analog very front-end



Analog channel overview

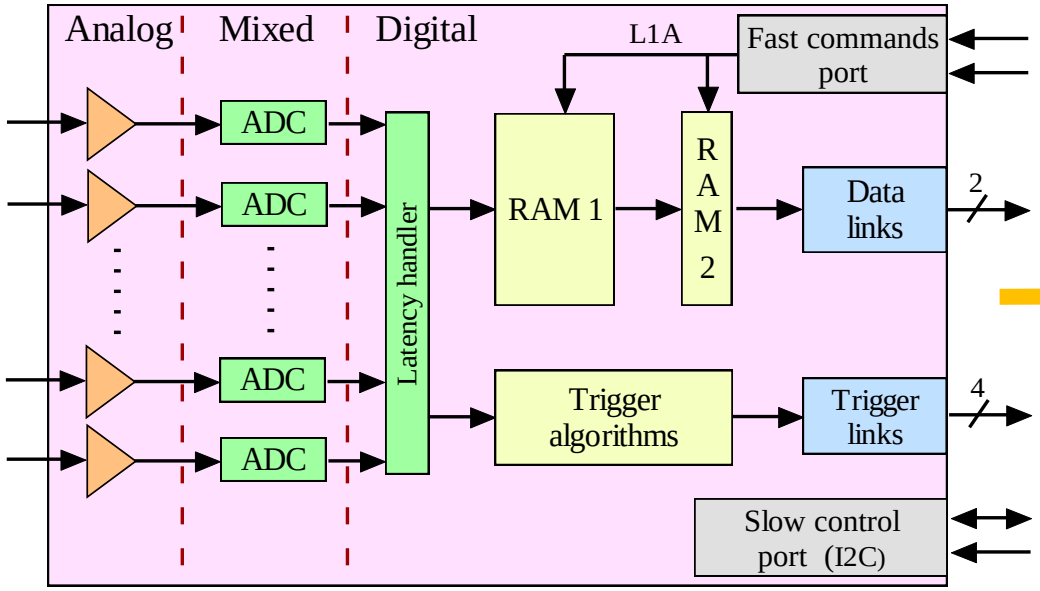
- The charge measurement is done with ADC + TOT (measured by 2 TDC)
  - Non-linear zone between ADC and TOT switching
- The time measurement is made by 1 TDC (also used for the charge)

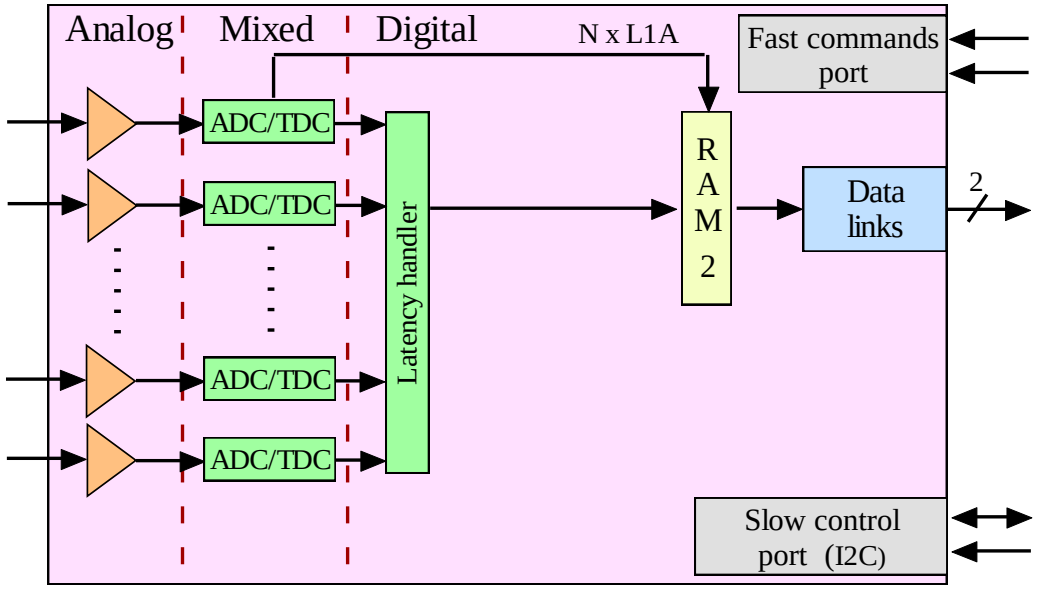




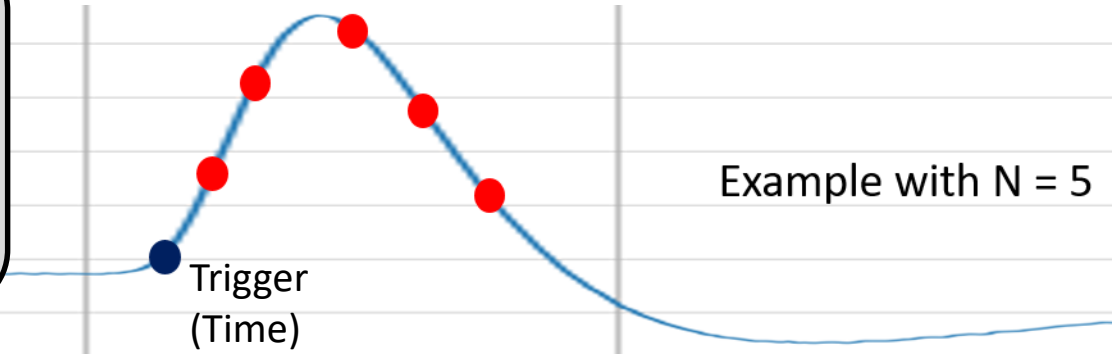
EIC: Moving to a waveform digitizer with auto-trigger

- Possible if "**low rate**" ➔ suppress all the LHC trigger lines (ease system integration)



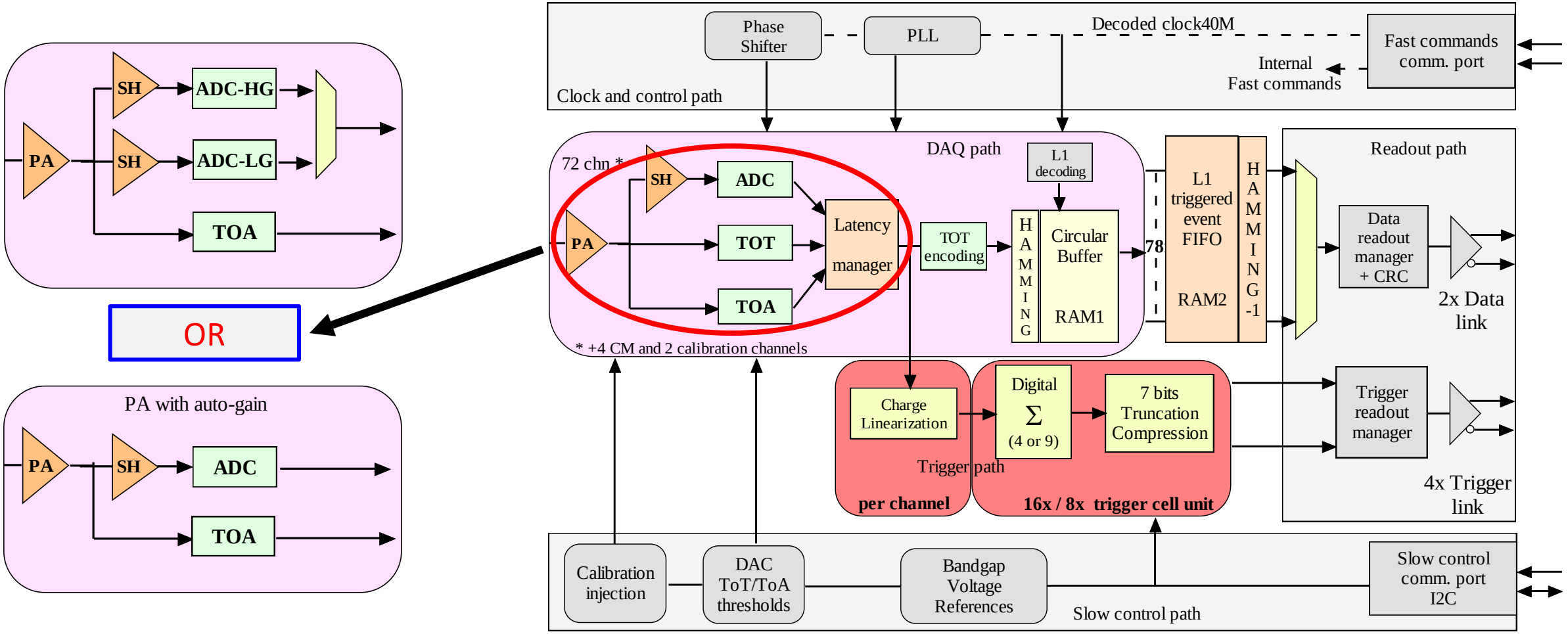


- Each event passing the threshold is readout
- Auto-trigger with N "samples" (1 to 7)
- Can be exercised with present HGCROC (multiple L1A-triggers)



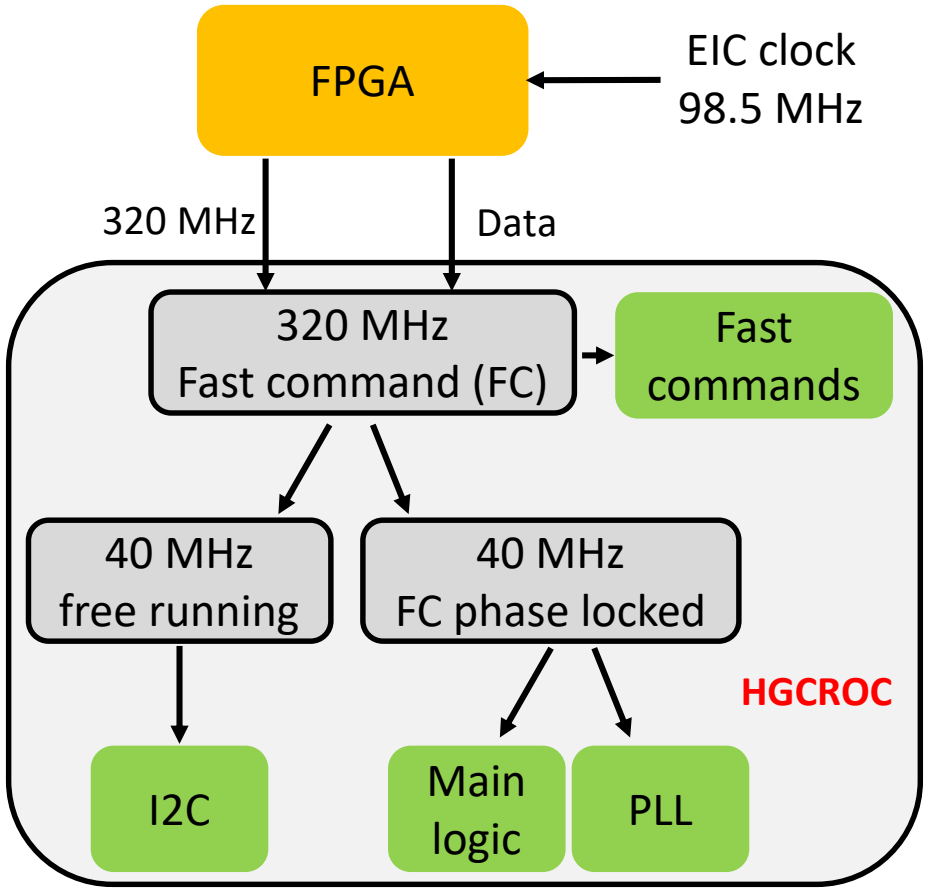
EIC: analog very front-end simplification

- Smooth transition between both ranges – TOT is a quite complicated (as the preamp is saturating)

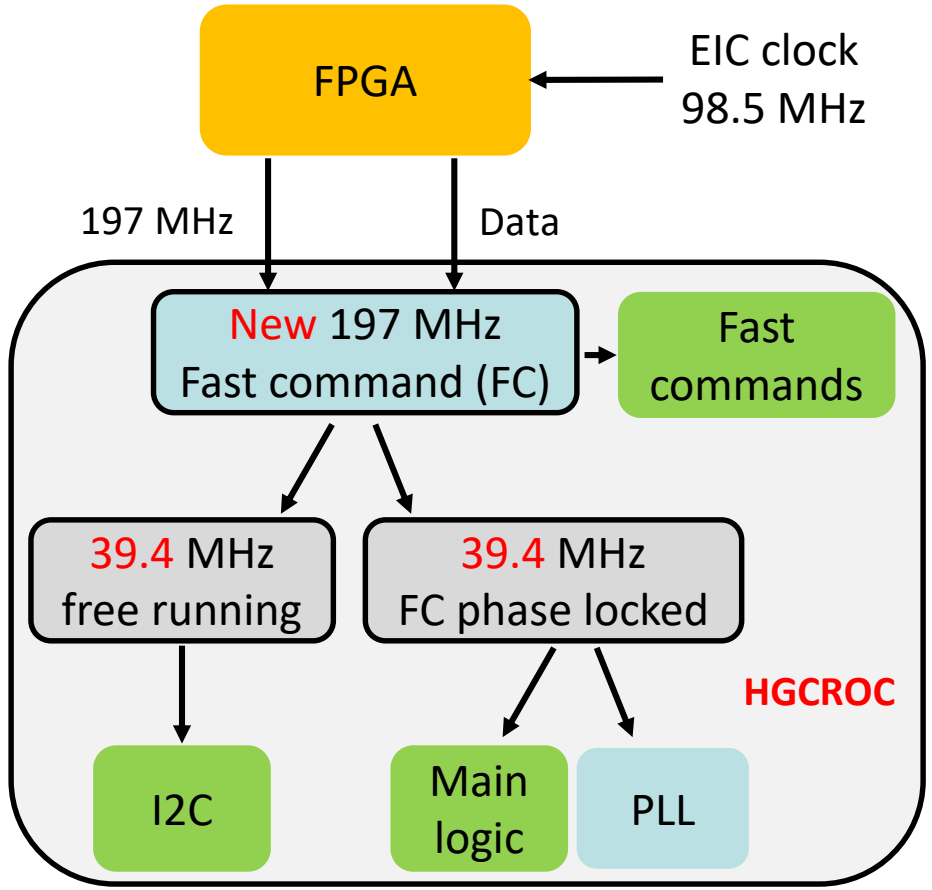


EIC: clocking scheme (LHC vs EIC)

- Adapt LHC-like 40 MHz to EIC clock ➔ done within the FPGA with 2 possible solutions
  - 40 MHz / 1280 Mbps or 39.4 MHz / 1260.8 Mbps



Baseline (no change)



This could be tested with actual HGCROC (PLL)
With 315.2 MHz instead of 320 MHz

EIC: HGCROC rates

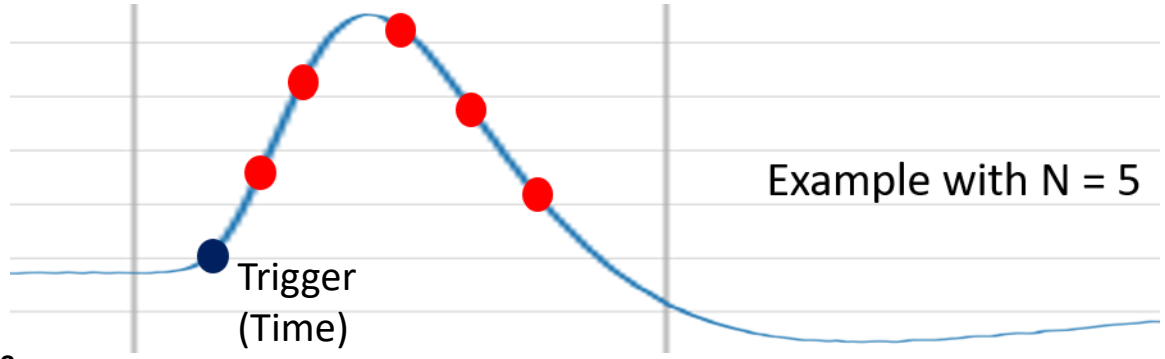
- Present HGCROC rate calculation: 1 serial link for 36 (+2) channels (HGCROC is arranged by 36 channels)

Version	Number of points (N)	Rate	Remarks
Present HGCROC-36ch	1	976 khz / ASIC	LHC is 1 snapshot
Per channel	3-4	6-9 kHZ / chn	Divide by N and by 36 (could be exercised)
Without TOT (ADC or bi-gain instead)	3-4	8-11 kHZ / chn	Shown slide 6
1 serial link per 18 ch	3-4	29-39 kHZ / chn	~ x4 rate / twice serial links (2 to 4)

Present HGCROC

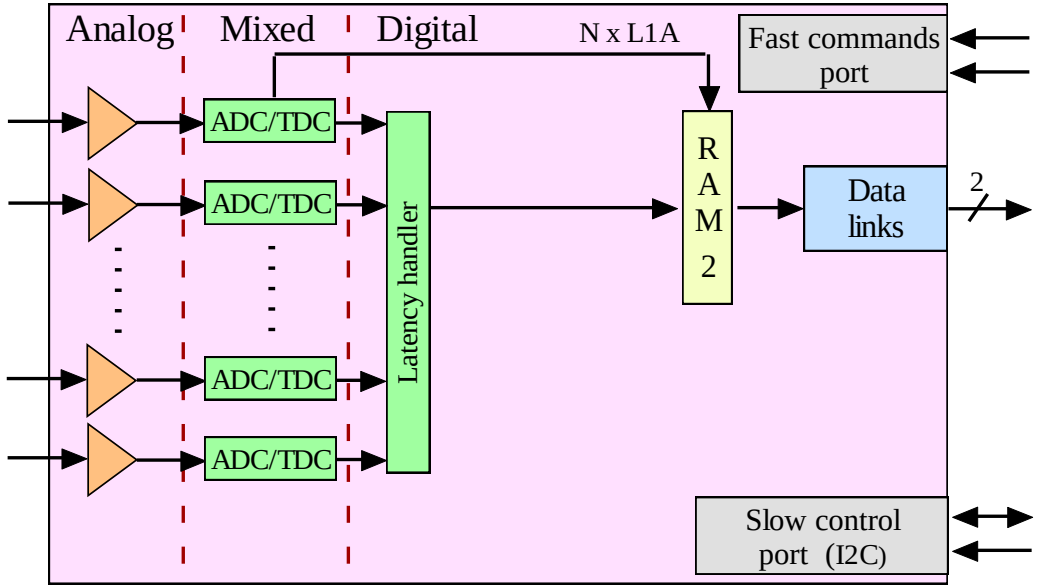
All events arriving at a different time (Worst case)

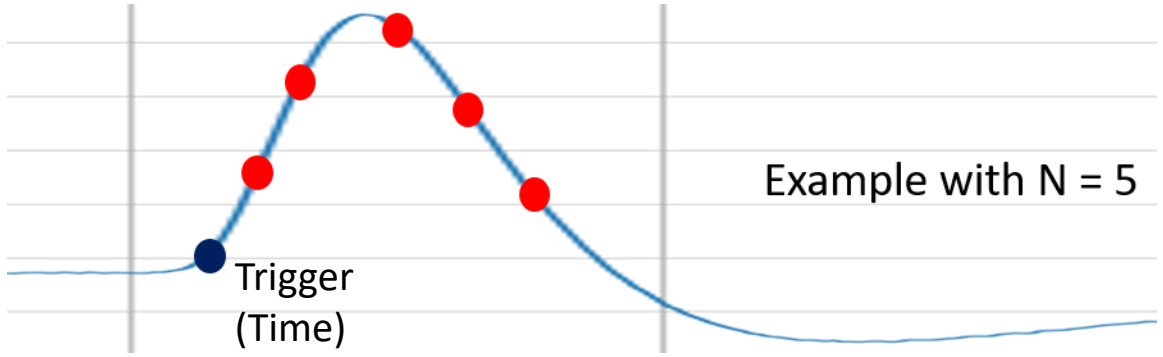
- Which rate to consider ?
- How many event overlap per 18 or 36 channels ?



Conclusion

- Present HGCROC could be
  - exercised as a waveform digitizer (with consecutive triggers)
  - Used to validate new clock scheme (possible change from 40 to 39.4 MHz for I2C – ADC – TDC – serial links…)
- Hit rate has an impact on the overall architecture
  - Digital architecture and also pile-up
- EIC clock should not be a problem (2 alternatives)
- Which level or radiation should be considered for ASICs ?
  - Parameters will be triplicated (LHC-like)
  - Same for digital logic ? (LHC: 200 Mrad, 1.10^{16} neq / cm²)
- Required analog performances versus detectors
  - Dynamic range, noise and shaping time
  - Detector capacitor, time resolution





Backup