EICROC update

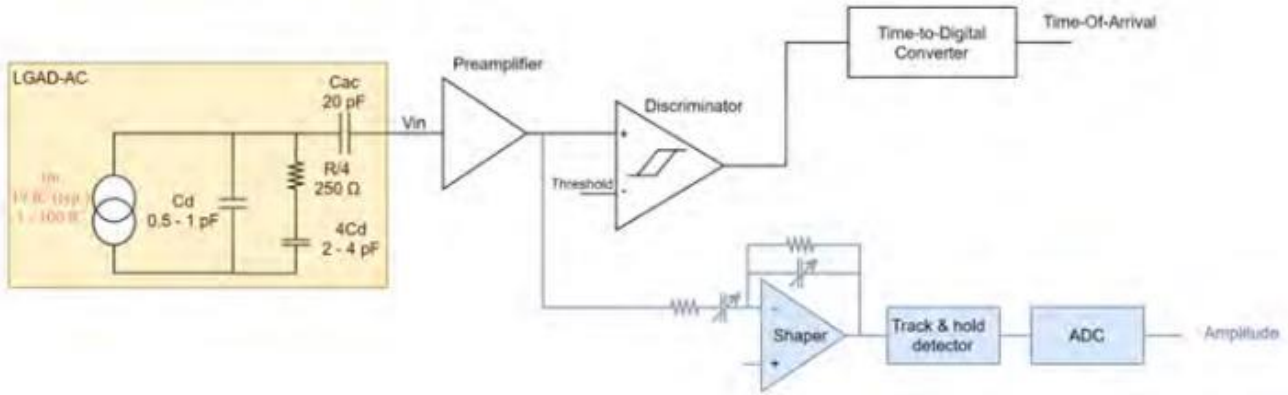
PIC meeting 17 july 2023

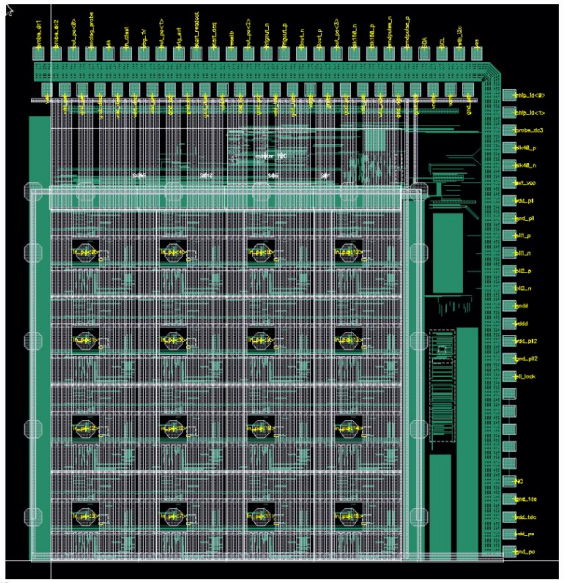
Ch. de La Taille

Organization for Micro-Electronics desiGn and Applications

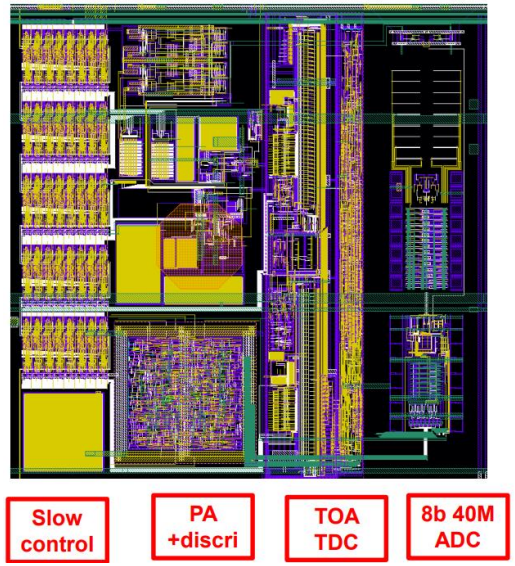
EICROC0 overview

- EICROC0 : 4x4 test chip for AC-LGADpixels of Roman pots





4x4 500 um pixels



One pixel

One pixel – EICROC0

- Preamp, discriminator – ATLAS ALTIROC.
- I2C slow controls – CMS HGCROC.
- TOA TDC – CEA-Irfu.
- ADC (8b) – AGH Krakow and IJCLab (EICROC1, EICROC2).
- Readout FIFO depth 8 (200 ns).
- Jitter: 15-20 ps.
- Power: 1-2 mW/Ch.

AGH Irfu OMEGA Microelectronics

status

Presented by D. Marchand 6 jul 23

Good analog performance

Digital noise observed => min threshold ~10 fC

Much larger than in Altiroc

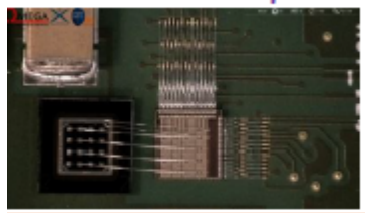
Status of EICROC0 Test Bench at IJCLab

RC2 | RC3

Preliminary studies [board w/ EICROC0, no AC-LGAD]

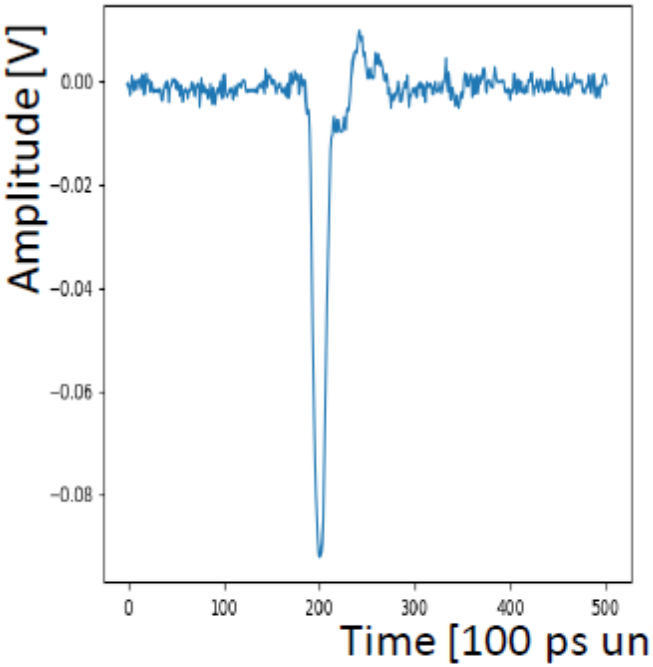
- TZ Pre Amplifier output signals
  - SNR > 70 for 12.5 fC input ; SNR > 6 for 1 fC input)
  - Jitter evaluation: < 20 ps (≥ 6 fC) ; 8 ps (25 fC)
- TDC performance (alone):
  - quantification step (~25 ps) in fair agreement with design
  - observation of a large noise coupled to 160 MHz clock
  - Time of Arrival resolution estimated to 14 ps (25 fC)
- ADC performance (alone) functional, 8-fold noise structure observed
- Evaluation of cross-talk between channels underway
- Further nvestigation of noise / clock couplings (**TDC and ADC**)

Short term plan: to evaluate performances of the existing board w/ **EICROC0 + AC-LGAD** (4 x 4)



Wire-bonding by Brookhaven National Laboratory

Typical **PA output signal** (12.5 fC input)



|Max. Amplitude| 95.5 mV

RMS 0.6 ns

Rise (Fall) Time **0.7 ns**
computed between
10% and 90% of |Max. Ampl.|

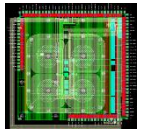
Evolution of EICROC

- EICROC0 is a testbeam prototype => sensor characterization
  - Triggered readout
  - all data shipped out : 16 ch * 8 samples ADC + TDC
  - Present power ~2 mW/ch + 4*20 mW « analog probe preamp »
  - ADC power + shaper/driver to be reduced from ~1 mW to 100 µW/ch => EICROC0A

- EICROC1 will address larger dimensions 4x16 or 8x16 and EIC readout
  - Address floor planning and power distribution
  - Selective readout : hit + 9 neighbouring channels

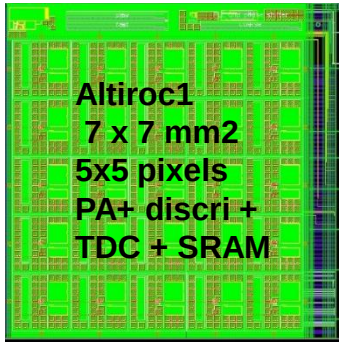
ATLAS LGAD readout : evolution of ALTIROC

2016

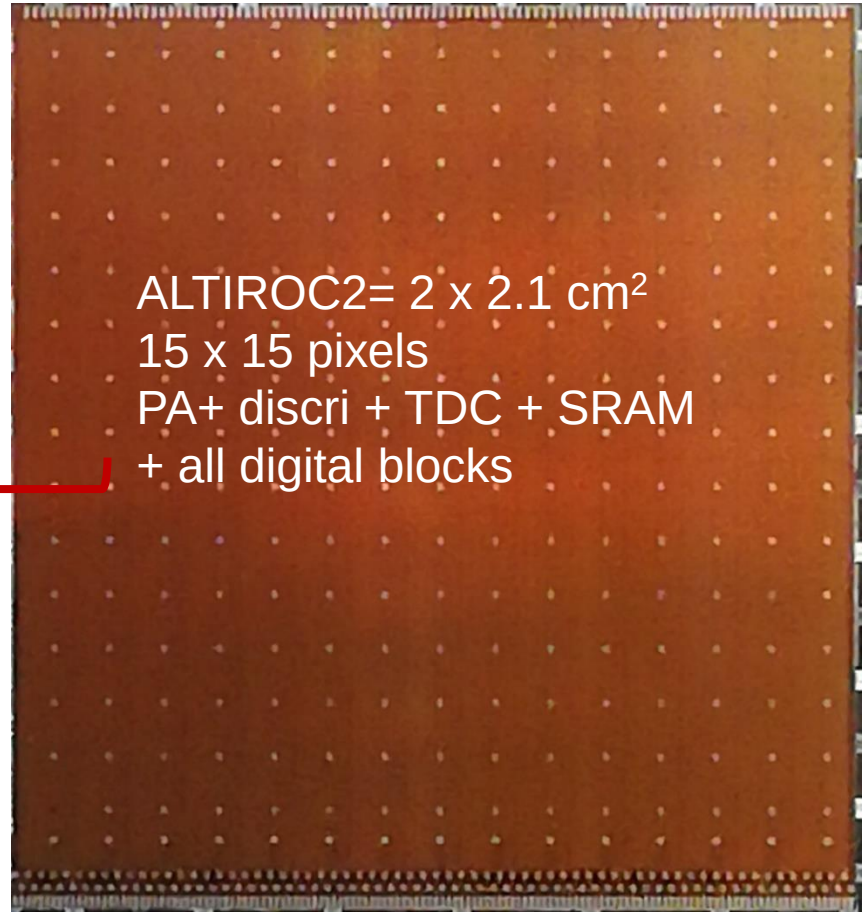


Altiroc0
2 x 2 mm2
2 x 2 pixels
PA + discri

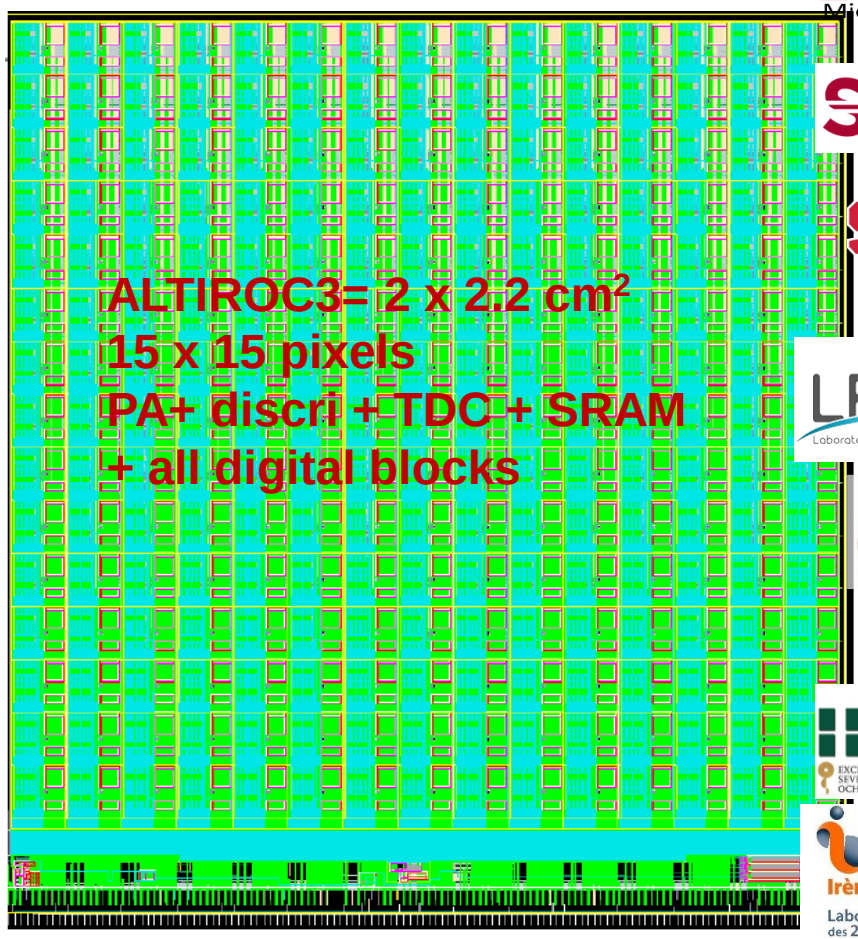
2018



2019



2021



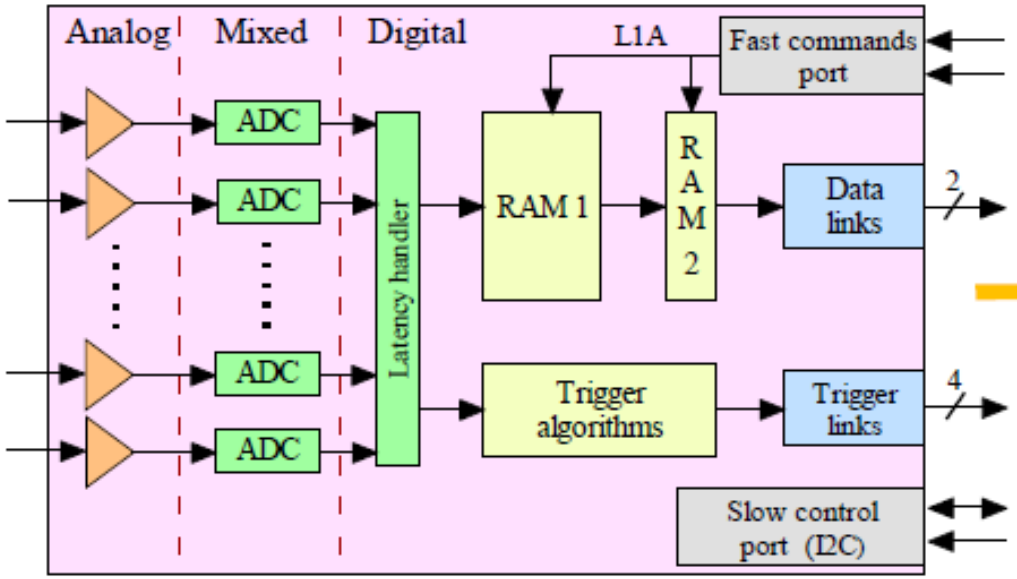
Altiroc0 and 1:
No digital,
To validate the FE part at system level (= ASIC bump-bonded onto a sensor)

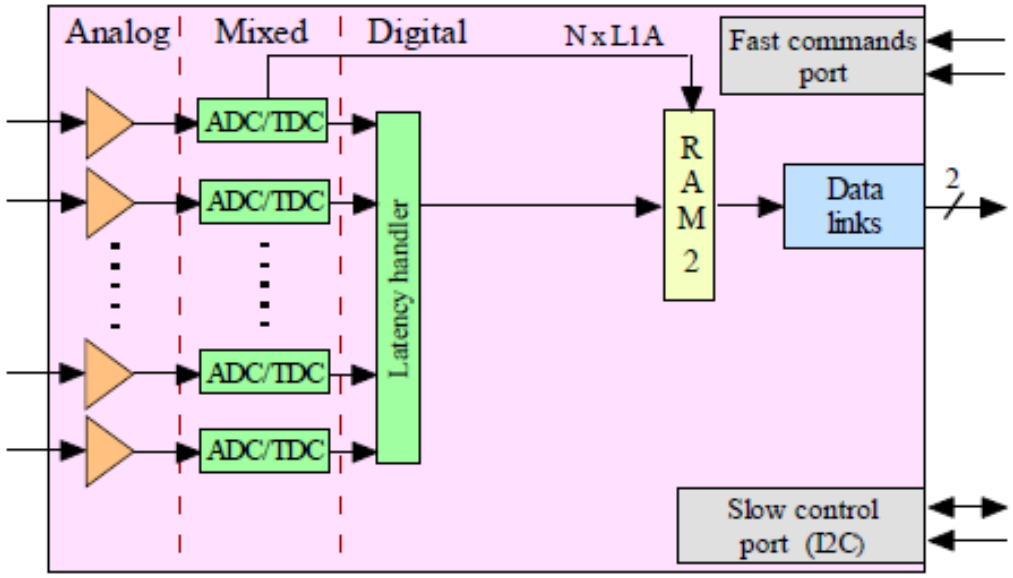
ALTIROC2:
First full size chip with 15 x 15 channels – 2 x 2 cm2
To demonstrate the functionality/performance of the ASIC (time resolution + luminosity counting) alone and bump-bonded onto a sensor
But NOT to be fully radiation hard (against SEE)

ALTIROC3:
Last full chip prototype before pre-production
Same as Altiroc2 but fully triplicated

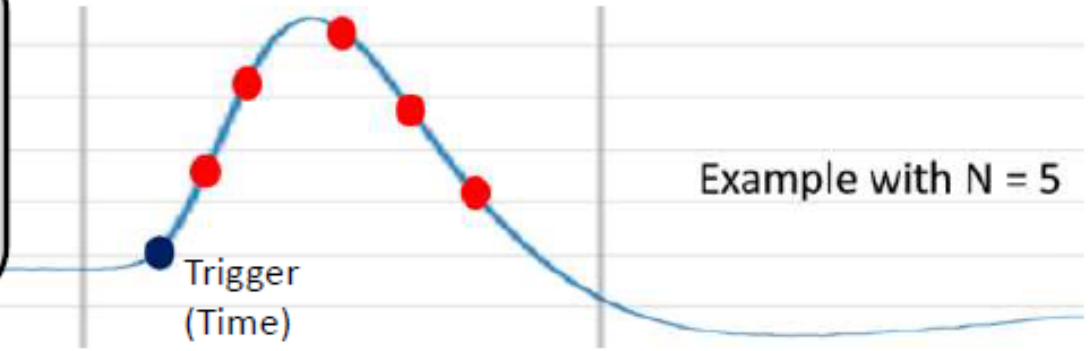
Evolution for EIC readout [F. Dulucq]

- Data streaming : auto-trigger and zero-suppress





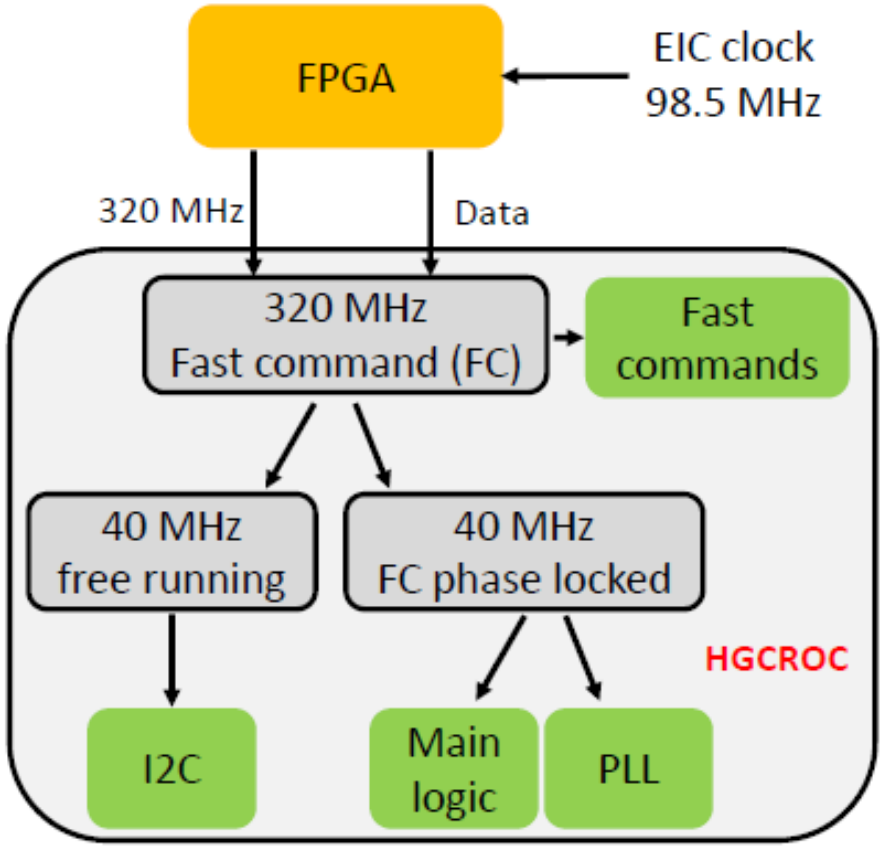
- Each event passing the threshold is readout
- Auto-trigger with N "samples" (1 to 7)
- Can be exercised with present HGCROC (multiple L1A-triggers)



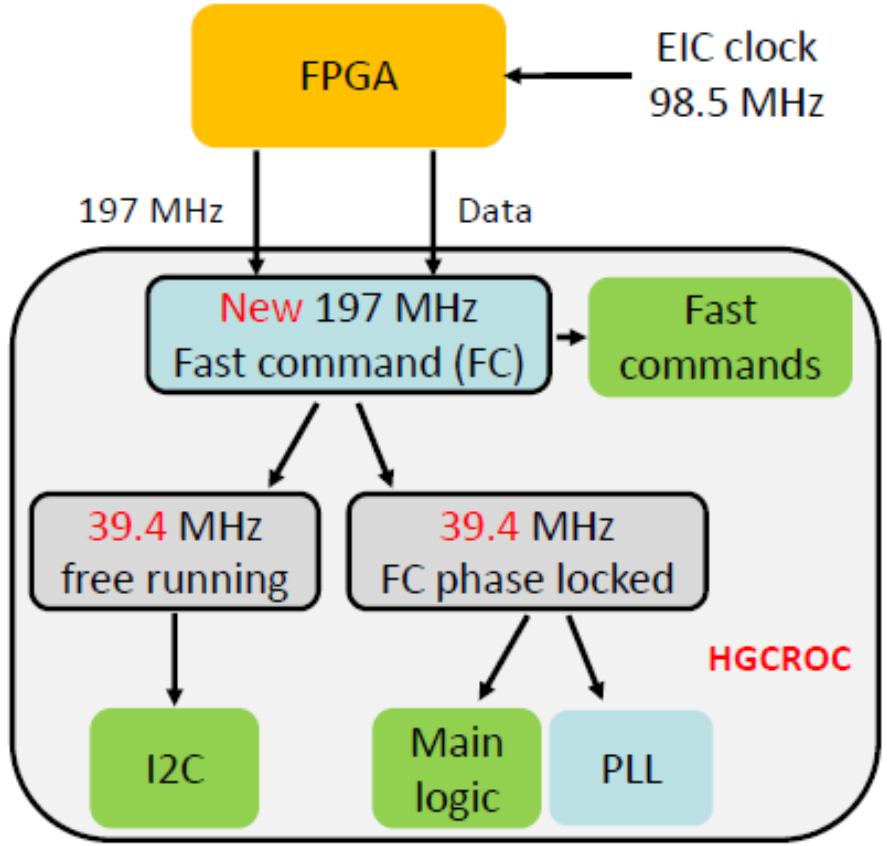
Evolution for EIC readout [F. Dulucq]

- Clocking scheme : 40 MHz -> 98.5 MHz

❑ Adapt LHC-like 40 MHz to EIC clock ➔ done within the FPGA with 2 possible solutions
  ❑ 40 MHz / 1280 Mbps or 39.4 MHz / 1260.8 Mbps



Baseline (no change)



This could be tested with actual HGCROC (PLL)
With 315.2 MHz instead of 320 MHz

Comparison EICROC / HGCROC

EICROC

- « 2D chip » 16 -> 1024 channels
- Input capacitance : Cd = 1-5 pF
- Dynamic range : 1 – 50 fC
- Target power : 1 mW/ch

HGCROC

- « 1D chip » 72 (64) channels
- Input capacitance : Cd = 5-50 pF
- Dynamic range : 1 – 10 pC
- power : 10-15 mW/ch

conclusion

- EICROC0 available for sensor tests
  - Good analog performance : tr = 700 ps, ENC = 0.16 fC
  - Large 40 MHz noise observed, origin not understood yet (chip, PCB, grounding ?)
  - Will also need a variant to reduce ADC power << 1 mW

- EICROC1 will address larger dimensions and EIC backend
  - Probably 4x16 to study floorplanning and power distribution
  - EIC clock and auto-trigger scheme, selective readout (hit and neighbours)
  - Should be ready fall 2024

- EICROC2 will have final dimensions (32x32) and functionnalities

backup

HGCROC3 performance