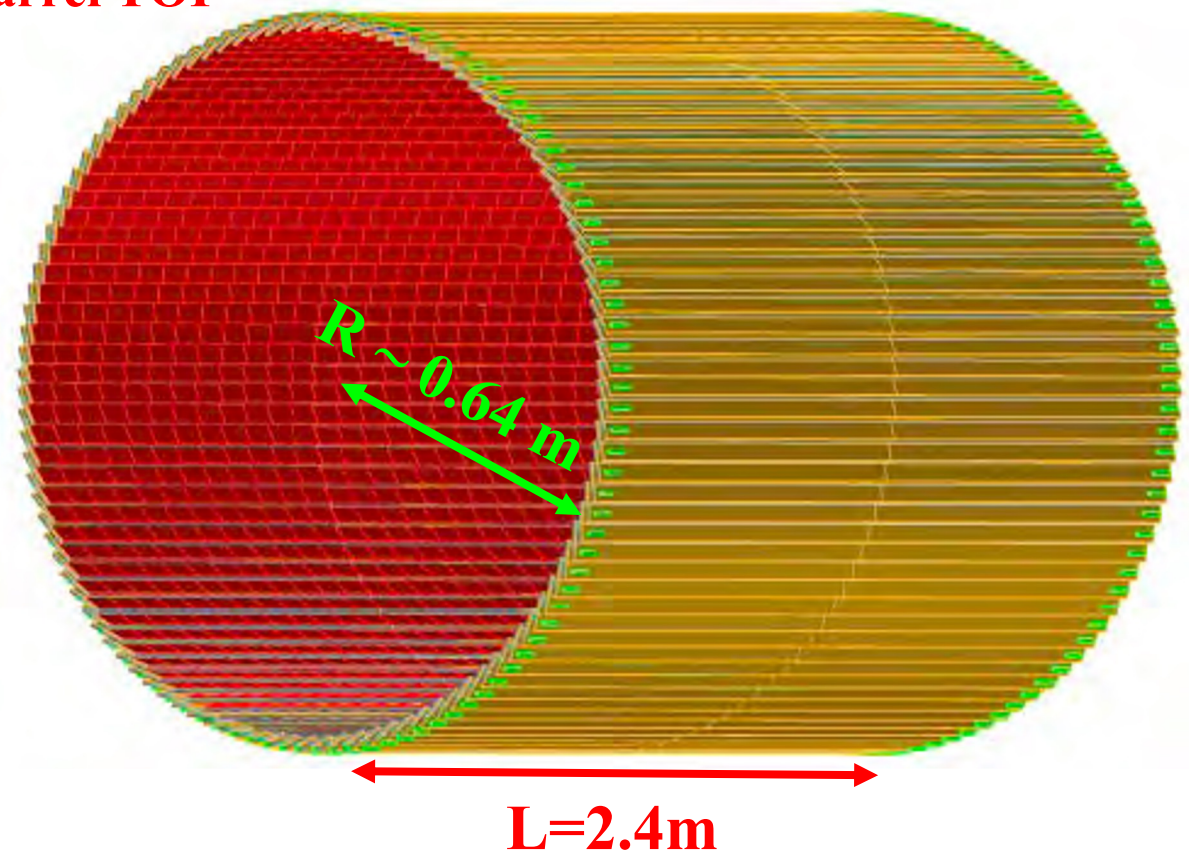
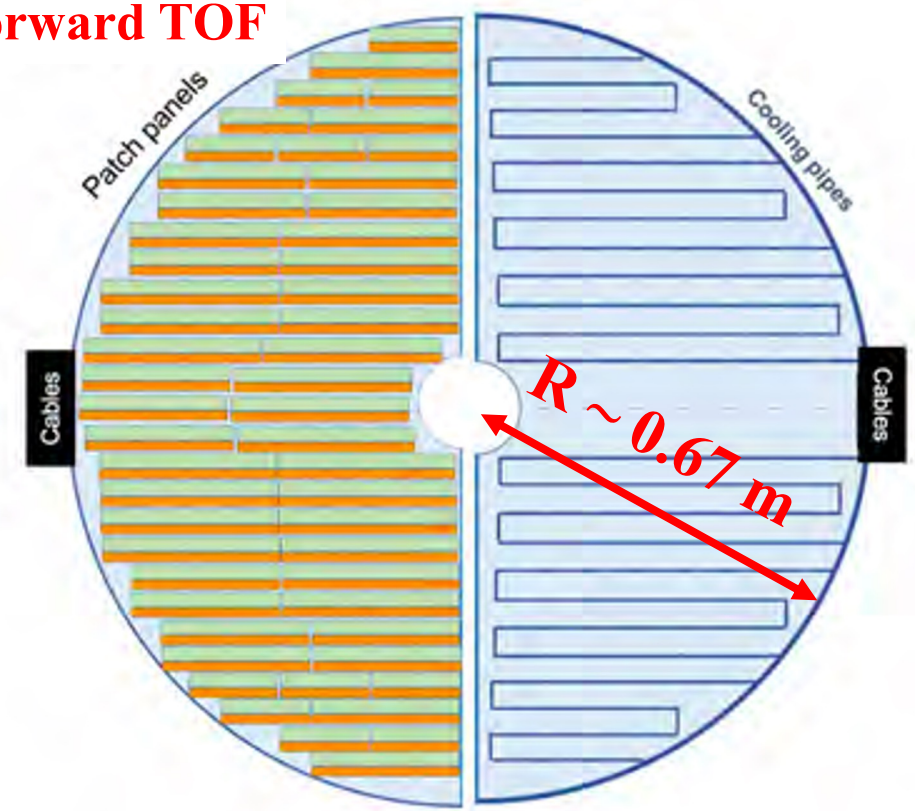
AC-LGAD TOF Detector Requirements

Barrel TOF



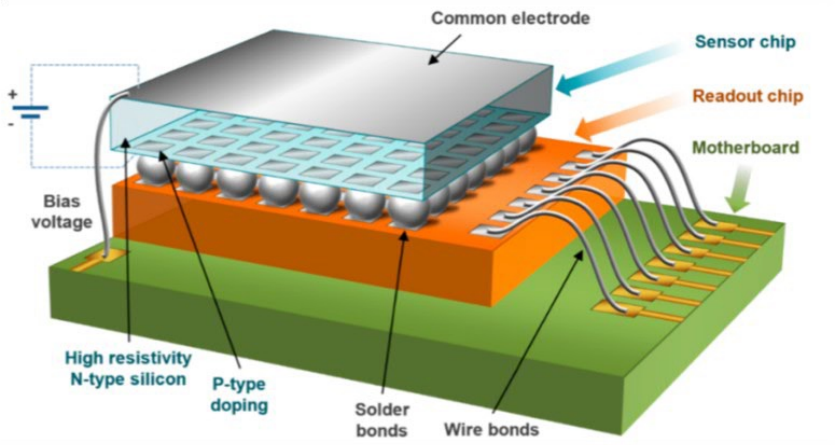
Forward TOF



Detector	Area	Channel size	Channel number	Time resolution	Spatial resolution	Material budget
Barrel TOF	~10 m^2	0.5mm x 10mm	~2.2 M	35 ps	30 μm in r·φ	0.01 X0
Forward TOF	~1.4 m^2	0.5mm x 0.5mm	~5.6 M	25 ps	30 μm in x and y	0.05 X0

TOF Requirements on Frontend ASIC

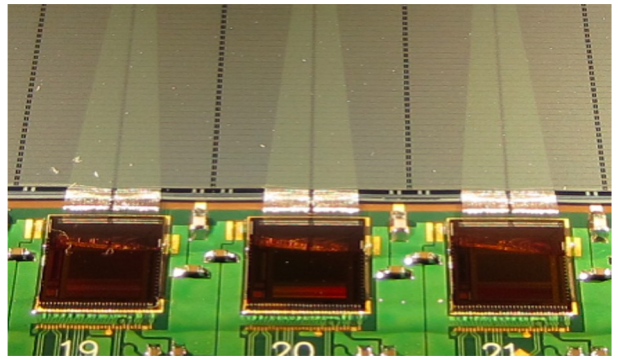
- **FTOF Requirements**
  - sensor bonding: **bump-bonding**
  - pixel size **0.5 x 0.5 mm^2 (larger pixels being studied)**
  - pixel array **32 x 32 (TBD)**
  - low power consumption **≤1 mW/channel**
  - low jitter **≤15 ps for MIP@12 fC**
  - sensitivity to low charge **(1-2 fC)**
  - time resolution (sensor+ASIC+clock) **≤25 ps**
  - spatial resolution **≤30 microns**



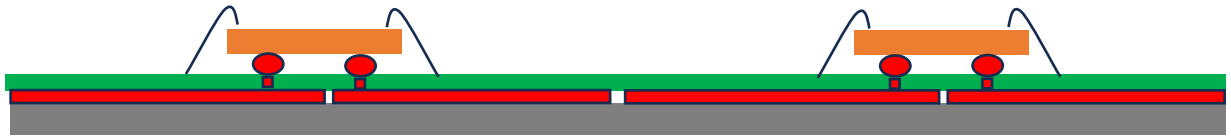
- **BTOF Requirements**
  - sensor bonding: **wire-bonding or bump-bonding (TBD)**
  - strip size **0.5 x 10 mm^2**
  - strip array **64 x 2 (TBD)**
  - low power consumption **≤1 mW/channel**
  - low jitter **≤ 15 ps for MIP@12 fC**
  - sensitivity to low charge **(1-2 fC)**
  - time resolution (sensor+ASIC +clock) **≤35 ps**
  - spatial resolution **≤30 microns**

Sensor

ROC

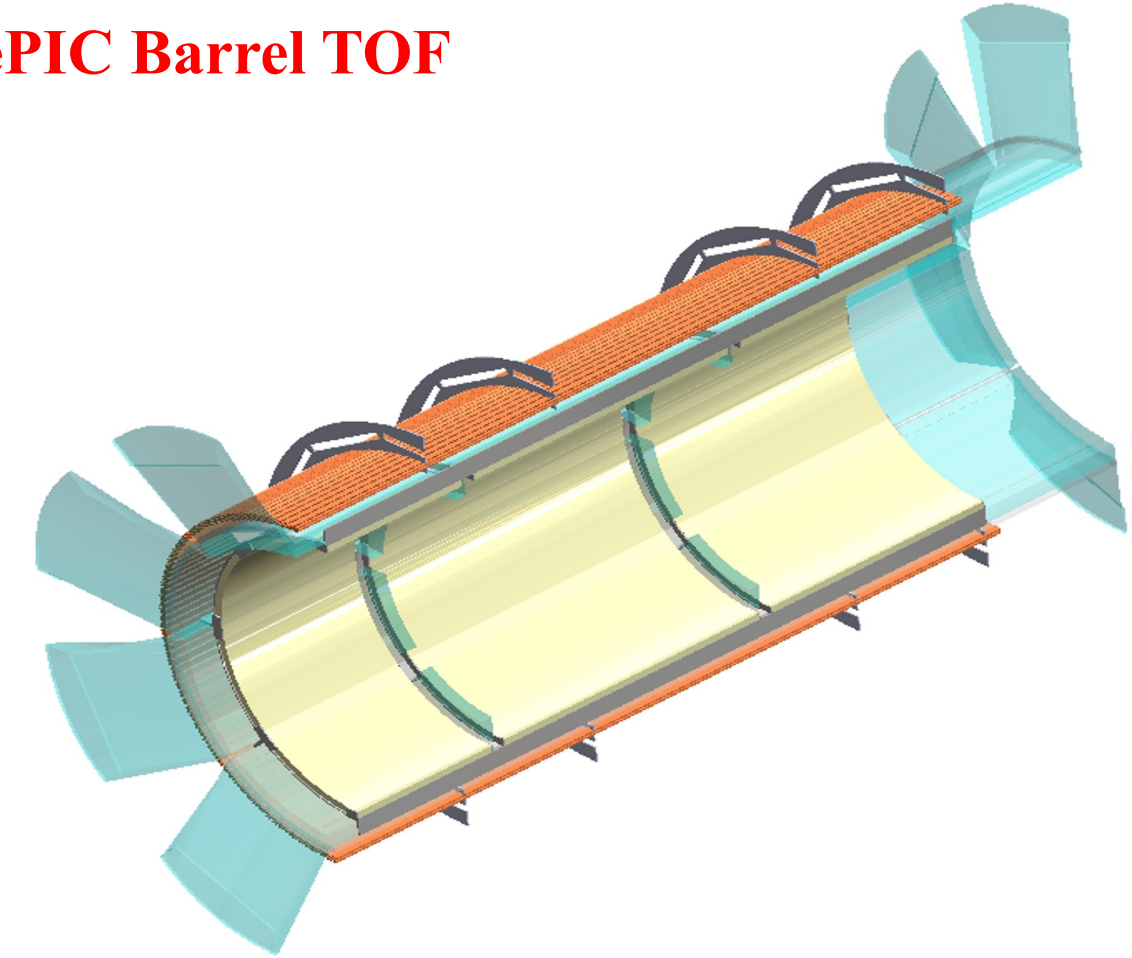


ROC
Interposer
Sensor

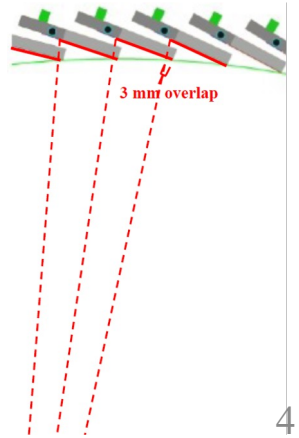


BTOF Detector Layout

ePIC Barrel TOF



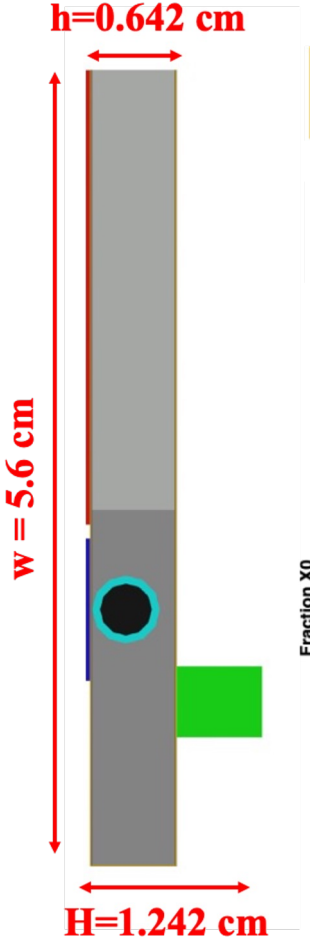
STAR Intermediate Silicon Tracker

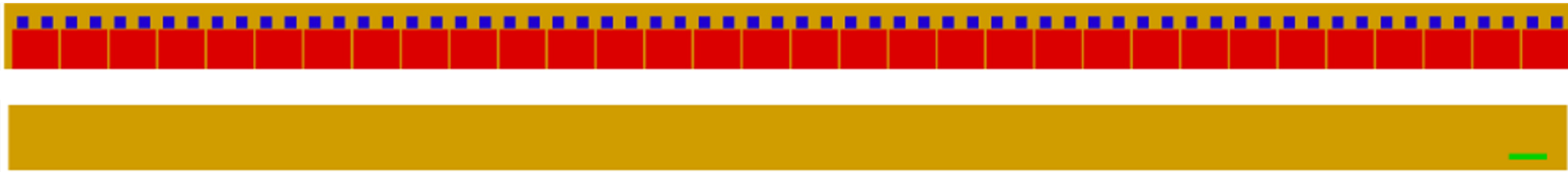


ePIC BTOF follows cylindrical silicon tracker design (e.g. STAR IST)

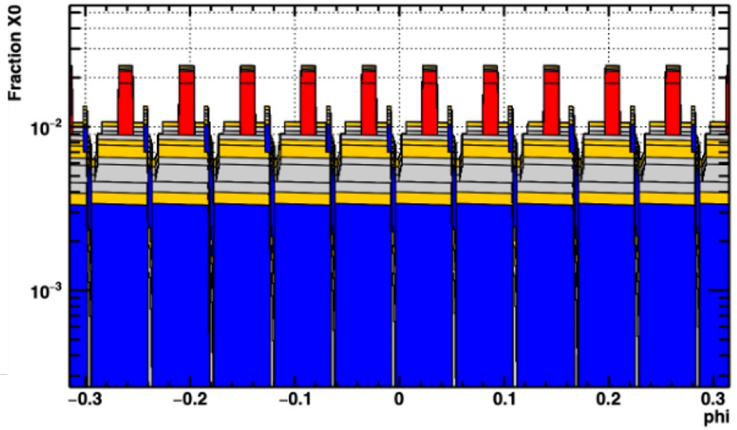
- Tilted stave modules overlap in phi to fully cover the azimuthal 2π angle
- Readout boards connected to the end of staves are outside of the BTOF acceptance (see next talk)
- Cooling tubes with liquid coolant at room temperature to take the heat generated by frontend ASIC

BTOF Detector Module Conceptual Design





- **64 AC-LGAD strip sensors**, each 3.2*4 cm^2 read out by **2 ASICs**
- **Low mass flexible Kapton PCB** distributes power and I/O signals from connector
- **Liquid coolant** in **Al tube** embedded in CF light-weight structure for heat removal

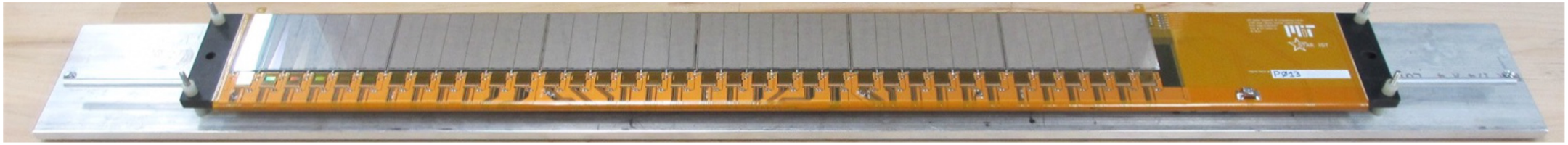


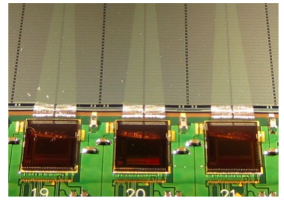
144 modules, each with 2 readout boards with 2 LV+HV cables, 2 DAQ fiber, and 1 cooling line

Power consumption: ~4 kW (2.4kW for ASIC, 1 kW for DC-DC, 0.6kW for sensors+cable)

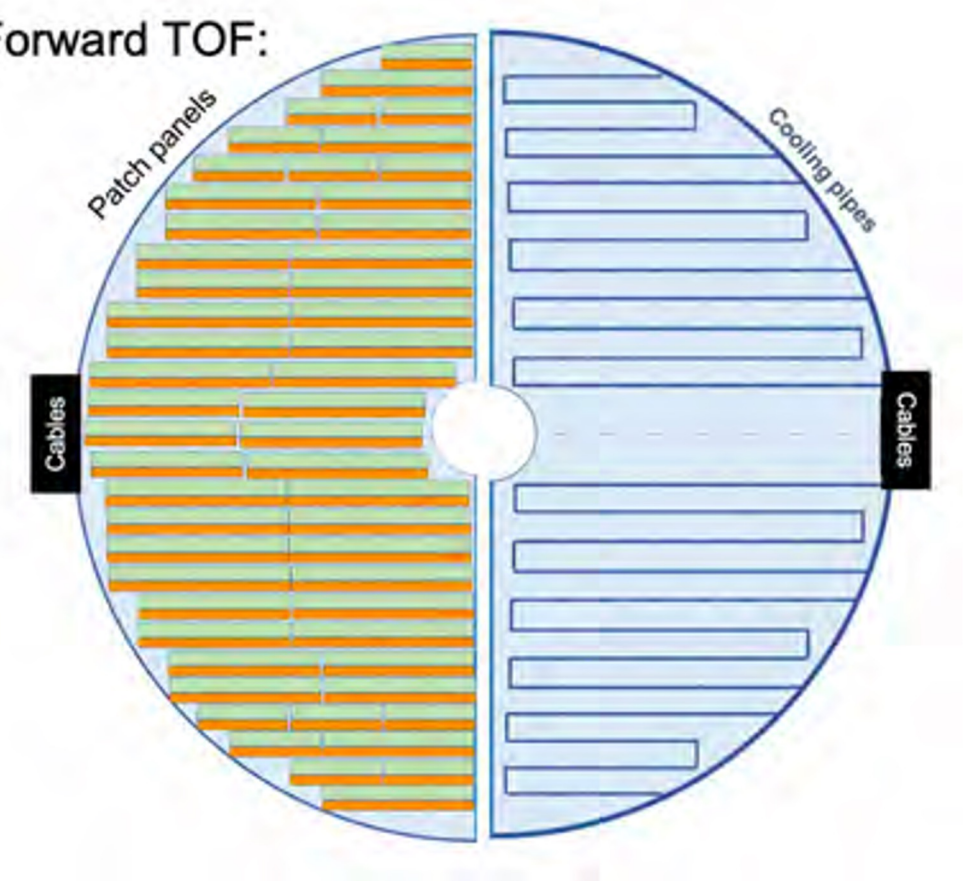
Total weight: ~70 kG

STAR IST

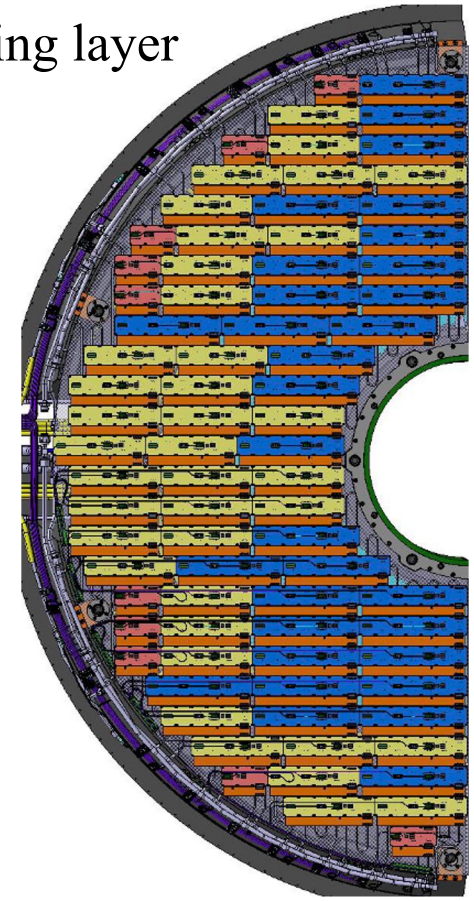




FTOF Detector Layout



CMS endcap timing layer

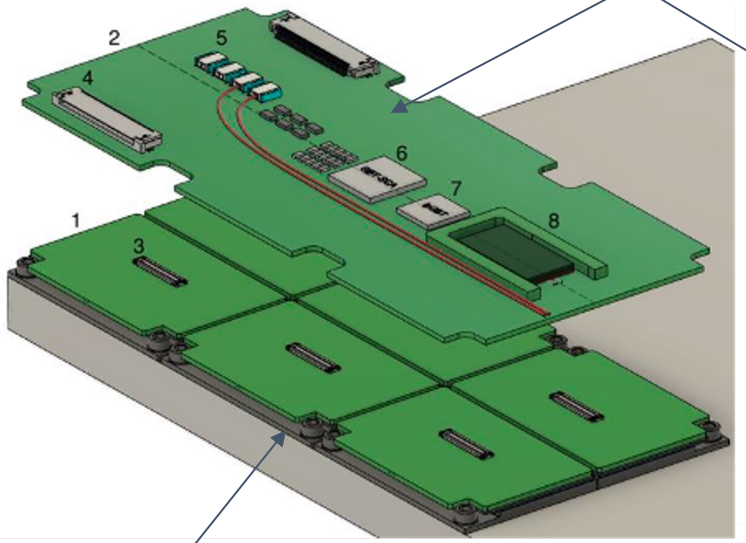


Forward TOF layout, based on the CMS ETL design:

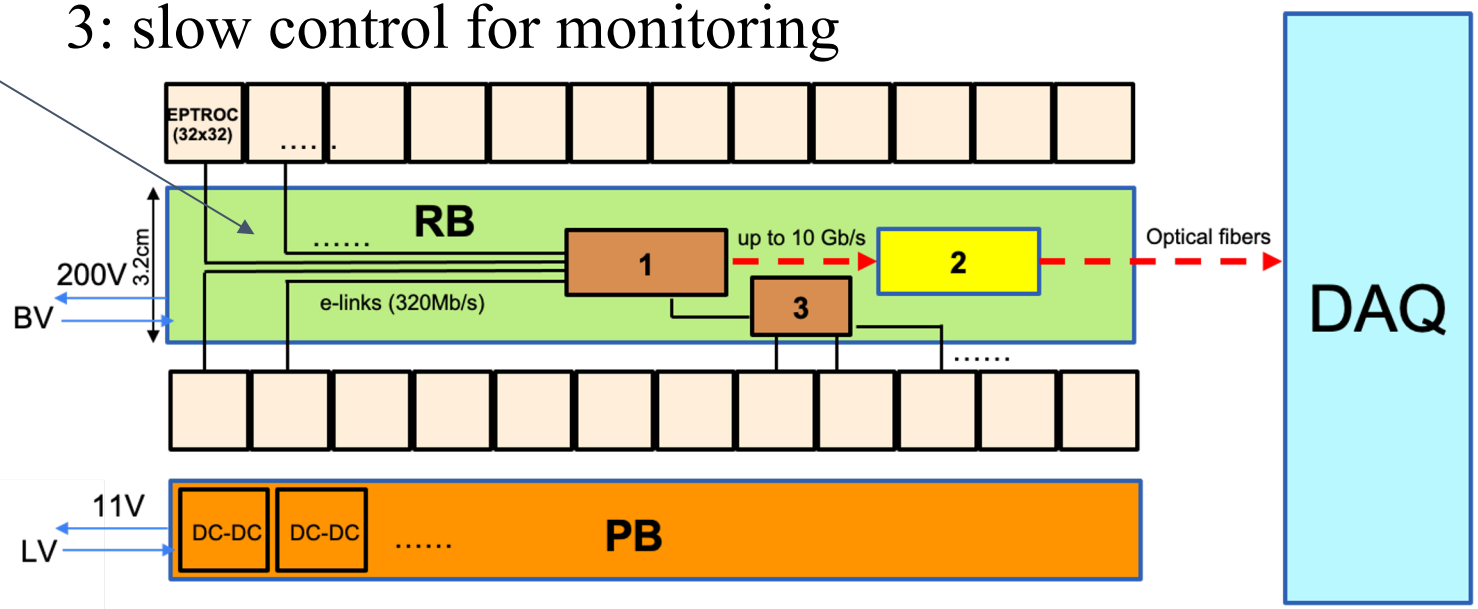
- Two halves DEEs made of light-weight (carbon fiber) support structure, tiled by rectangular modules of three types with different lengths
- Cooling tubes with coolant at room temperature to take the heat generated by frontend ASICs and other electronic elements

FTOF Detector Module Conceptual Design

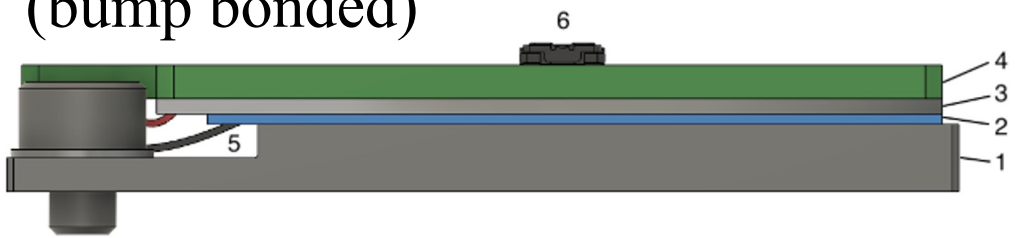
Readout Board



1: data transceiver FPGA chip
2: optical link module (e.g., CERN VTRx+)
3: slow control for monitoring



LGADs+EICROC
(bump bonded)



212 readout boards, each has: 1 fiber to DAQ, 2 LV cables (1 supply, 1 return) and 2 BV cables (1 supply, 1 return)

Power consumption: ~13 kW (8.5kW for ASIC, 3.5 kW for DC-DC, 1kW for sensors+cable)

- Considering 0.7x0.7 mm^2 sensor design, which reduces the power budget by ~50%