Calorimeter ASIC discussion

Norbert Novitzky
ORNL

Overview of Calorimeters – SiPM

	Insert Calorimeter	Forward HCal	Forward ECal	Barrel HCal	Barrel ECal	Backward ECal	Backward HCal (TBD)
SiPM Size	1.3x1.3 mm Or 3x3 mm	1.3x1.3 mm And 3x3 mm	6x6 mm2	3x3 mm	3x3 mm	6x6 mm2	1.3x1.3 mm Or 3x3 mm
Voltage	38-45 V	50-53 V	33-47 V	38 V	38-42 V	40-46 V	38-45 V
Array of SiPM (summing)	-	5 or 10	2x2 Parallel	-	4x4 (Assembled)	2x2	-
Capacitance/channel	320pF or 1280 pF	1.6-3.2 nF And 6.4-12.8 nF	10 nF	320 pF	500pF	2.5 nF	320pF or 1280 pF
Pixel/channel	7.3k Or 38k	13k-26k And 72k-144k	638k	40k	50k	160-360k	7.3k Or 38k
simulation Dynamic range	0.2 pC - 300 pC (TBD)	0.2 - 100 pC And 0.5 - 500 pC (TBD)	0.29pC-5.8 nC	1-52 pC	0.27pC - 400 pC	10-10,000pC (TBD)	0.1pC-320 pC (TBD)

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SiPM stability

	Insert Calorimeter	Forward HCal	Forward ECal	Barrel HCal	Barrel ECal	Backward ECal	Backward HCal
Overvoltage	+2 V	+3-4 V	+2 V	+2 V	+2.7V	+5 V	+3-4 V
Stability required [mV]	10mV	100mV	10 mV	100mV	TBD	TBD	100mV
Bias voltage accuracy	TBD	< 1% gain	0.05%	0.04%		TBD	TBD
Radiation simulation **Bias voltage current**	1mA (TBD)	100nA (TBD)	1 mA (TBD)	TBD	(TBD)	TBD	100nA (TBD)
Temperature compensation	TBD	Yes	Yes, temperature compensated bias	TBD	SiPM Cooled	Bias voltage temperature compensation would be preferred	TBD

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Pre-amp requirements

	Insert Calorimeter	Forward HCal	Forward ECal	Barrel HCal	Barrel ECal	Backward ECal	Backward HCal
Linearity	< 1 %	< 1 %	1-2 %	< 1 %	< 1 %	< 0.5 %	< 1 %
Gain stability	< 1 %	< 1 %	< 0.5 %	< 1 %	< 1 %	< 0.5 %	< 1 %
Full simulation **Peak time**	10 ns (TBD)	10 ns (TBD)	< 200 ns (TBD)	10 ns (TBD)	(TBD)	20 ns (TBD)	10 ns (TBD)
Charge resolution	TBD	15-16 bit (TBD)	14 bit (TBD)	15-16 bit (TBD)	13 bit (TBD)	14-bit (TBD)	10 bit (TBD)
Time-hit resolution	100 ps (TBD)	100 ps (TBD)	1 ns (TBD)	100 ps (TBD)	100 ps (TBD)	5 ns (TBD)	100 ps (TBD)
Double pulse resolving	**TBD**	TBD	**Few hundred ns (TBD)**	**50-100 ns (TBD)**	(TBD)	**10 ns(?) (TBD)**	TBD

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FEB, RDO questions for integration

	Insert Calorimeter	Forward HCal	Forward ECal	Barrel HCal	Barrel ECal	Backward ECal	Backward HCal
SiPM bias monitoring	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Temperature monitoring	Yes	Yes	Yes	Yes	Yes	Yes	Yes
FEB on detector	Yes	Yes	Yes	Yes	Yes	Yes	Yes
FEB accessibility	Between runs	Anytime	Between runs	Anytime	Between runs	Between runs	Anytime?
FEB-RDO distance	5m	5m	6-25m	5m	5m	3-5m	5m
RDO on detector	No	No	No	No	No	No	No
RDO location	Same as FHCal	On the side of the detector	Racks	5 m away	Same as Barrel HCal? 5 m	TBD	Side of detector

List of improvements in the HGCROC

1. **Self triggering:**
   - Trigger level should be set in slow control
   - How many samples should be also set in slow control
   - How many channels should be connected (need still some simulation work)
2. **EIC clock as input:**
   - Easiest to provide 2xEIC clock, 198.5MHz
   - Internally it will run on 1/5th of the clock
3. **May require to change the shaper for longer**
   - Now it is within 100ns and probably looks good
4. **Length of internal memory:**
   - Simulation required, now it is 32-depth
5. **Number of data lines:**
   - Currently we have 2x1.28Gbps, we can check if we need more
6. **Input capacitance check:**
   - This can be optional also to accept different input capacitances in EIC range
7. **Summing of multiple analog signals:**
   - Again optional, but might be implemented in the input

**These are the crucial ones, already in the list**

May require a lot of simulation work of the hit frequency, etc.

These can be also with an inexpensive analog circuit

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Timeline – initial

	2023						2024											
	Jul	Aug	Sept	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sept	Oct	Nov	Dec
SiPM requirements	■																	
Readout requirement		■																
First prototype readout card			■															
Feedback to Omega group			■	■	■	■												
Testing first detector prototypes							■	■	■	■	■	■	■	■	■	■	■	■
Omega Modification to design										■	■	■	■	■	■	■	■	■

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Integration questions
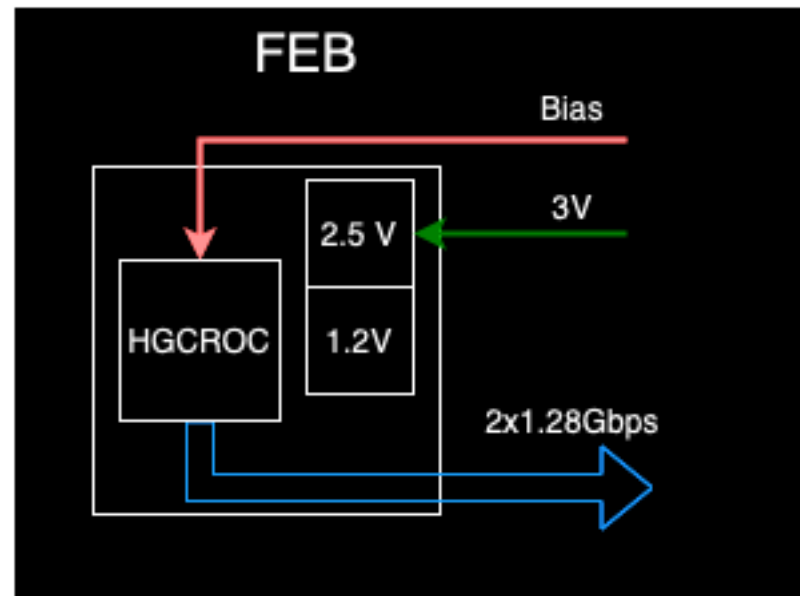
FEB:
- 1 HGCROC for readout (72 channel)
- 3 V input, 2 LDO's on board to provide 2.5V (analog), 1.2 V (digital)
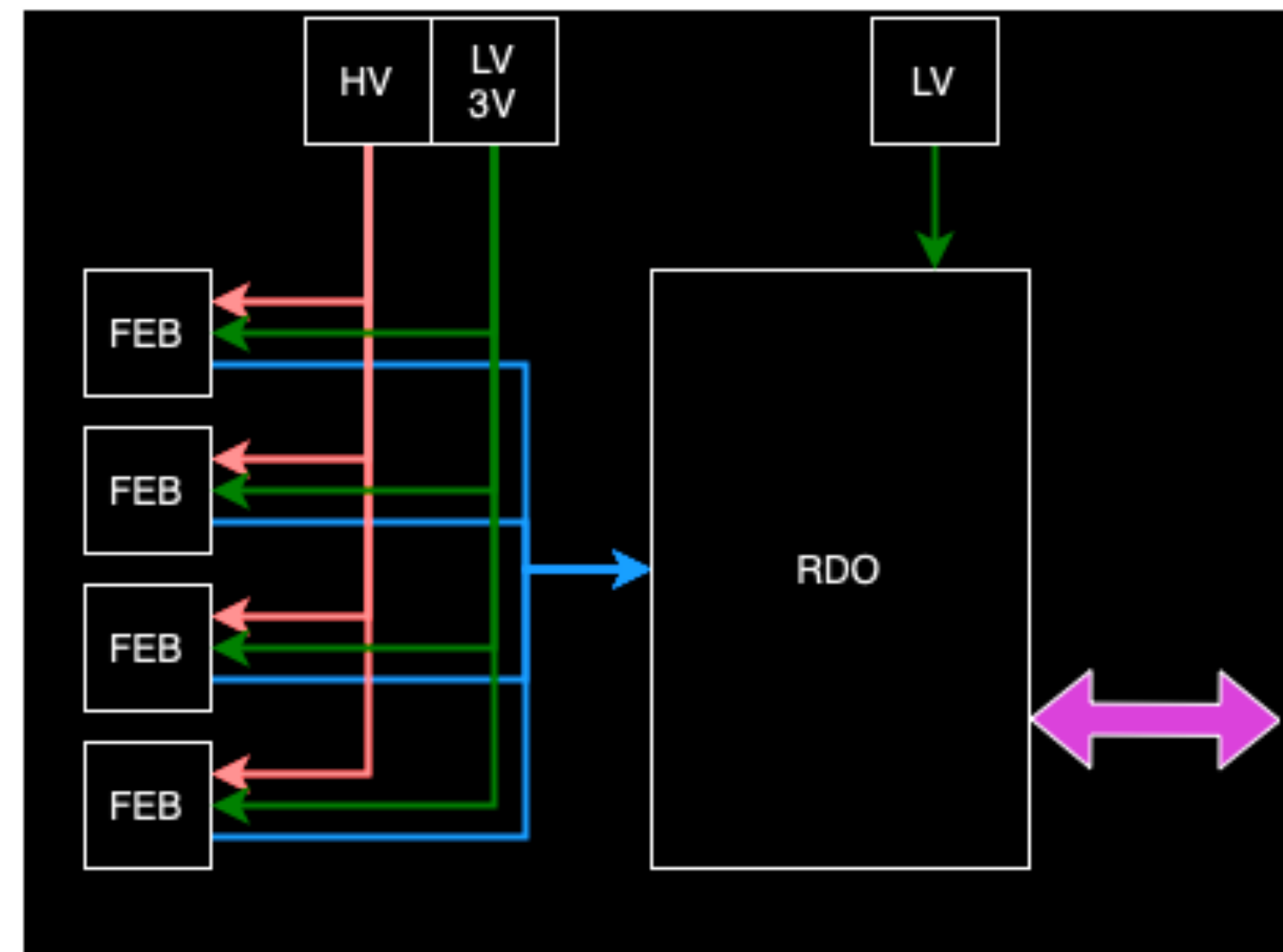- HV distributed to SiPM
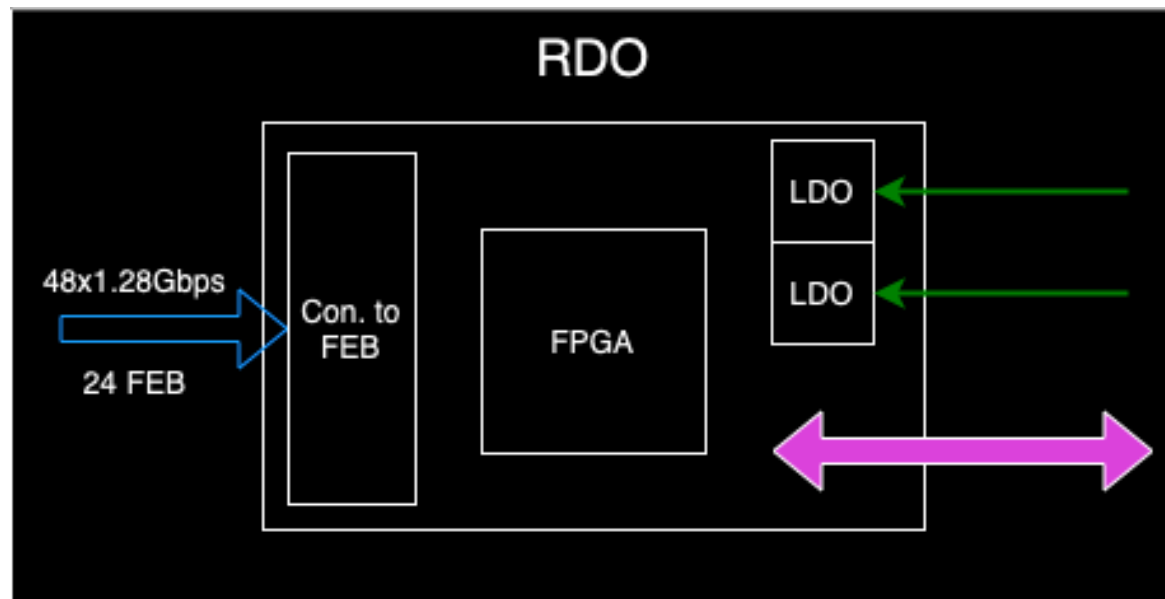
RDO:
- Handles 24 FEBs (have to be tested)
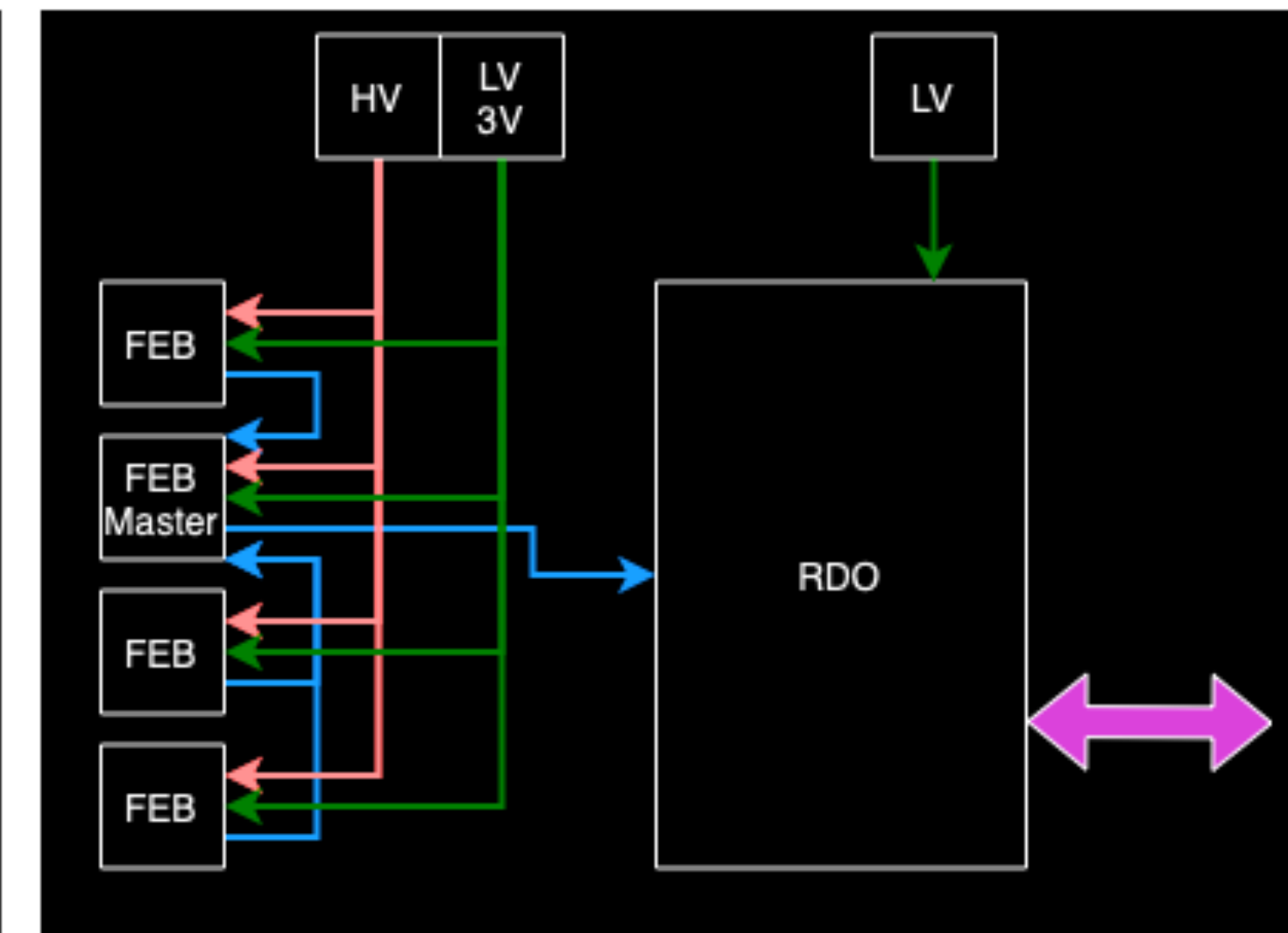- Input voltage for the FPGA
- Fiber for clock and readout

Readout scheme:
- FEB will receive LV, HV independently
- Option A - independent data connection between RDO/FEB
- Option B - Master/Slave cabling. This only if it helps with integration

Option A

Option B

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Feedback to ASICs

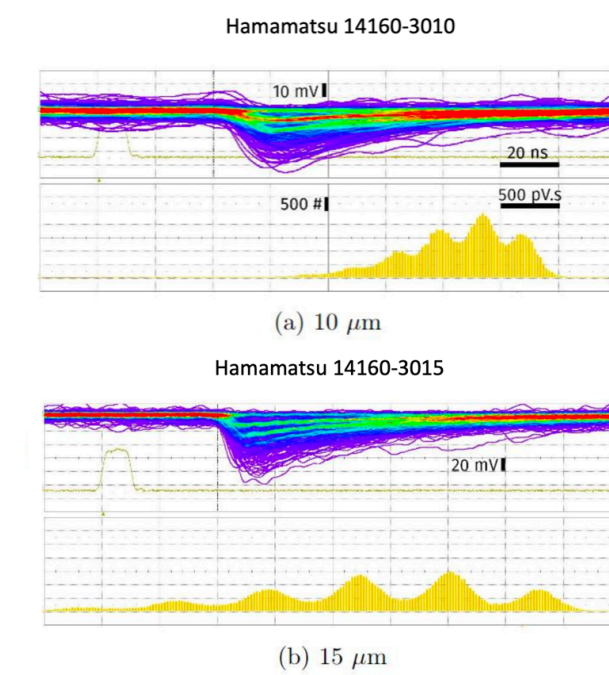|	Insert Calorimeter	Forward HCal	Forward ECal	Barrel HCal	Barrel ECal	Backward ECal	Backward HCal
SiPM analog waveform	TBD	TBD	TBD	TBD	TBD		TBD

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Time line – detector hardware, bench tests

	Insert Calorimeter	Forward HCal	Forward ECal	Barrel HCal	Barrel ECal	Backward ECal	Backward HCal
2023 Q3		First testbeam					
2023 Q4							
2024 Q1	First prototype						
2024 Q2							
2024 Q3							
2024 Q4							
2025 Q1							
2025 Q2							
2025 Q3							
2025 Q4							

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