TIC meeting - gaseous trackers

The FEE SALSA and its coupling to the ePIC gaseous trackers

Monday August 14th 2023

Marco Bregant
on behalf of SALSA collaboration

Outline

- The SALSA project
- SALSA analogic specifications
  - Any issue reading out the 2-D readout elements of the ePIC tracking detectors?
- SALSA architecture and the DAQ streaming readout
- Status of SALSA Project

The SALSA Project

Common initiative of Sao Paulo Universities and CEA Saclay IRFU

- Sao Paulo University (USP) + associated institutes designed the SAMPA chip (readout chip for ALICE TPC), experts in on-chip ADC and digital processing
- IRFU developed several MPGD front-end chips (AFTER, AGET, DREAM,...) and other kinds of chips (SAMPIC and HGCROC TDC,..), experts in low-noise radiation-hard generic front-ends
- Large amount of complementary competences to collaborate on a common versatile front-end chip including digitization and digital processing

The SALSA Project

HEPIC IFUSP

Motivations of the project

- To develop a new versatile multi-channel readout chip in the framework of the EIC project and beyond
  - adapted to streaming readout DAQ
  - for different kinds of MPGD detectors: trackers, TPC, photon detectors,...
  - and different kinds of usage: physics readout, calibrations, detector tests, etc...
  - with possible further developments for other kinds of detectors (calorimeters, non-MPGD photon detectors) and/or specific constraints (for instance ps-level time resolutions)
- Large ranges in term of signal amplitudes, electrode capacitances, peaking times, signal rates
- Integrated per-channel ADC and digital processing
- TSMC 65nm technology for improved performances and sustainability
- Blocks developed by CERN in TSMC 65nm are also reused

Salsa: target specification

Versatile front-end characteristics

- 64 channels
- Large input capacitance range, optimized for 50-200pF, reasonable gain up to 1nF
- Large range of peaking times (50-500 ns) and gain ranges (50 to 5000 fC max amplitude), programmable scaling of the input stage
- Large range of input rates, able to go much larger than 25 kHits/s/channel (EIC conditions), 100 kHz/ch with fast CSA reset (anti-saturation circuit)
- Reversible polarity, front-end elements can be by-passed

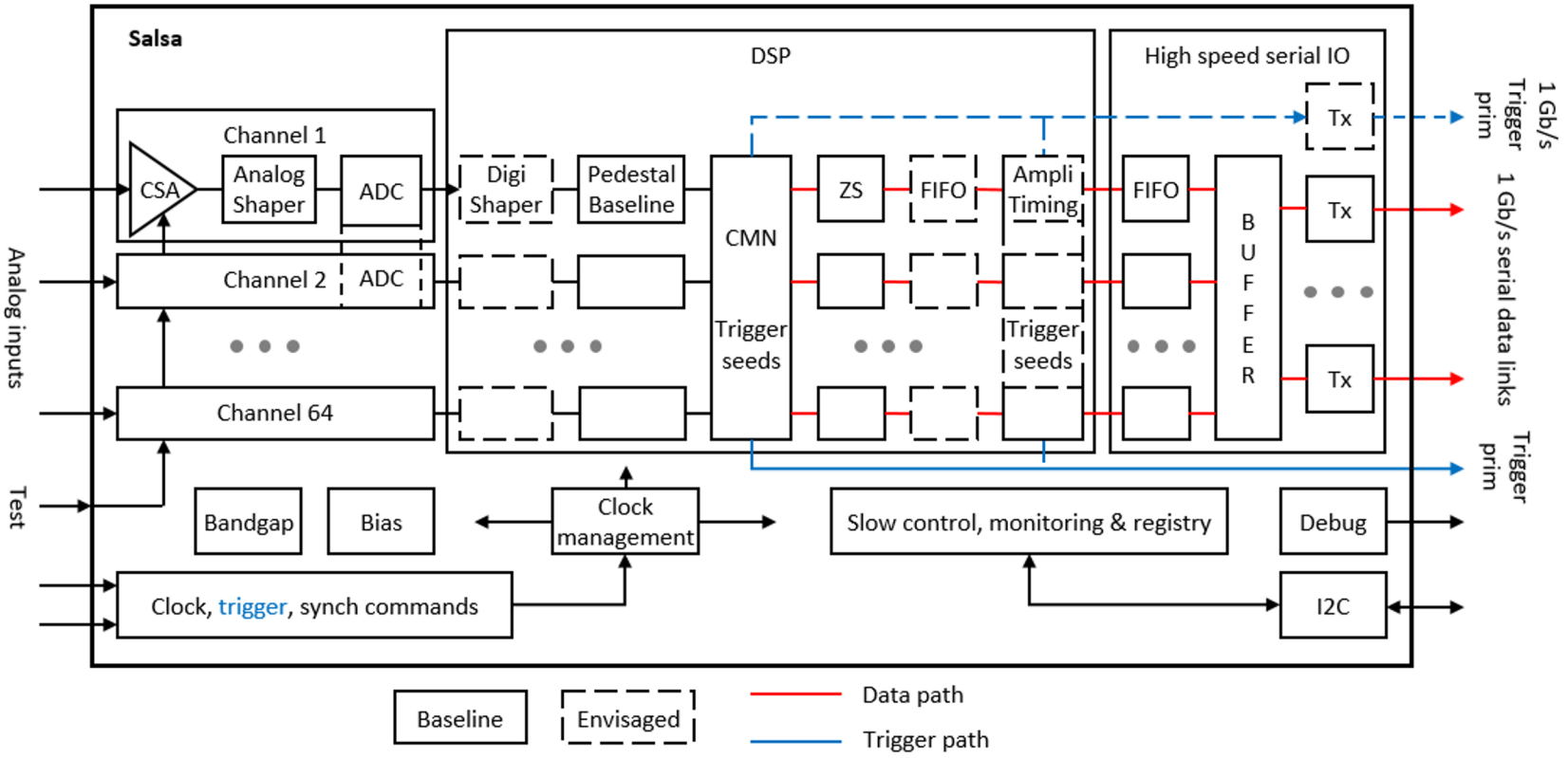
Digital stage

- Fast sampling ADC for each channel on 12 bits (> 10 effective bits) at up to 50 MS/s at least, possibility to double rates by coupling pairs of channels
- Integrated DSP for internal data processing and size reduction: pedestal equalization, common mode correction, zero suppression, peak finding, trigger generation, hit scalers for monitoring, other digital filtering; processes to be activated according to user needs
- Continuous readout compatible with streaming DAQ foreseen at EIC, triggered mode also available
- Several 1 Gb/s output data links

General characteristics

- ~1 cm^2 die size, implemented on modern TSMC 65nm technology
- Low power consumption ~ 15 mW/channel at 1.2V
- Radiation hardened (SEU, TID), working at 2T magnetic field

Preliminary design of SALSA



How are we organized

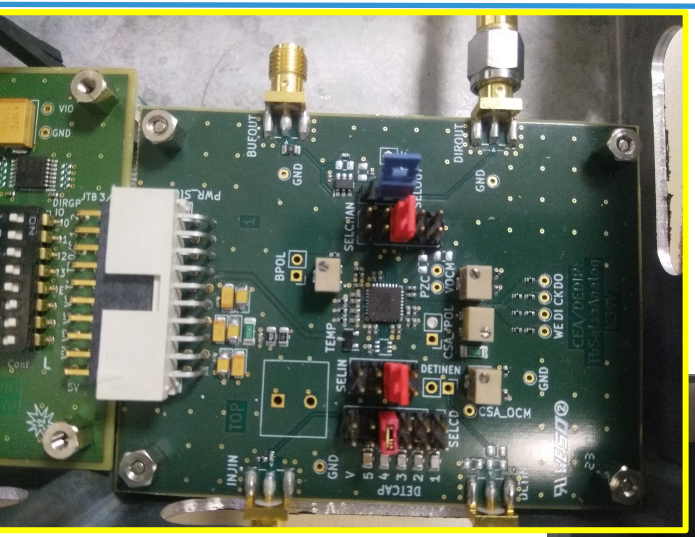
Main project structure

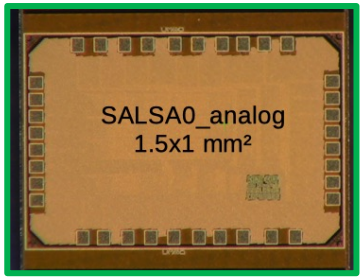
- Split in different tasks
- Front-end (IRFU)
- ADC (USP)
- DSP (USP + IRFU for algorithms)
- General services (clock, slow-control, analog biases, high speed links) + architecture (IRFU with help of USP, some CERN blocks to be reused)
- Parallel development of the different tasks, with constant interactions between groups for common issues, in particular interfaces between tasks
- Design, production and tests of several prototypes foreseen to complete the project

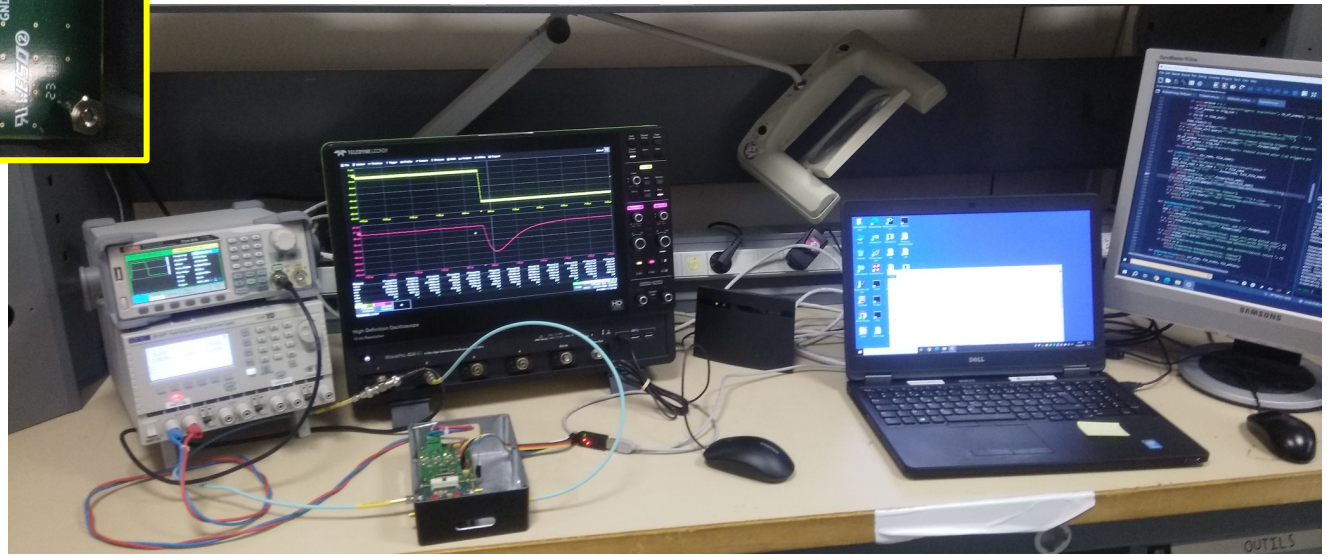
PRISME side project (Lead by IRFU)

- Goal: to develop a 65nm hybrid PLL IP block for clock generation, to be used in SALSA, also available for other usages
- Large frequency ranges or input (40-125 MHz) and output (up to 1.6GHz)
- 4 programmable clock outputs with individual frequency and phase tuning
- Very low internal time jitter, ~3ps RMS up to 1 GHz

Salsa0_analog already being tested







Any issue reading out the 2-D readout elements of the ePIC tracking detectors?

HEPIC IFUSP

from “SALSA’s aims”:

- Large input capacitance range, optimized for 50-200pF, reasonable gain up to 1nF
- Large range of peaking times (50-500 ns) and gain ranges (50 to 5000 fC max amplitude), programmable scaling of the input stage
- Large range of input rates, able to go much larger than 25 kHits/s/channel (EIC conditions), 100 kHz/ch with fast CSA reset (anti-saturation circuit)
- Reversible polarity

SALSA was thought since the very beginning to be “compatible” with a variety of potential detectors, including high signals and coping with high detector capacitance

from “SALSA’s aims”:

- Radiation hardened (SEU, TID), working at 2T magnetic field

2T magnetic field was already planned.

I collect the following information: ~10krad over 10 years, and 1×10^{11} n_{eq}/cm^2 over 10 years

TID values does not seem so worrisome (nevertheless, to be tested!)

neutron fluence does not look so high (again, test! test! test! to be sure SEE rate is low!)

About Streaming Readout

from “SALSA’s aims”:

- Integrated DSP for internal data processing and size reduction: pedestal equalization, common mode correction, zero suppression, peak finding, trigger generation, hit scalers for monitoring, other digital filtering; processes to be activated according to user needs
- Continuous readout compatible with streaming DAQ foreseen at EIC, triggered mode also available
- Several 1 Gb/s output data links

Streaming readout functionalities will be addressed during the DSP development.

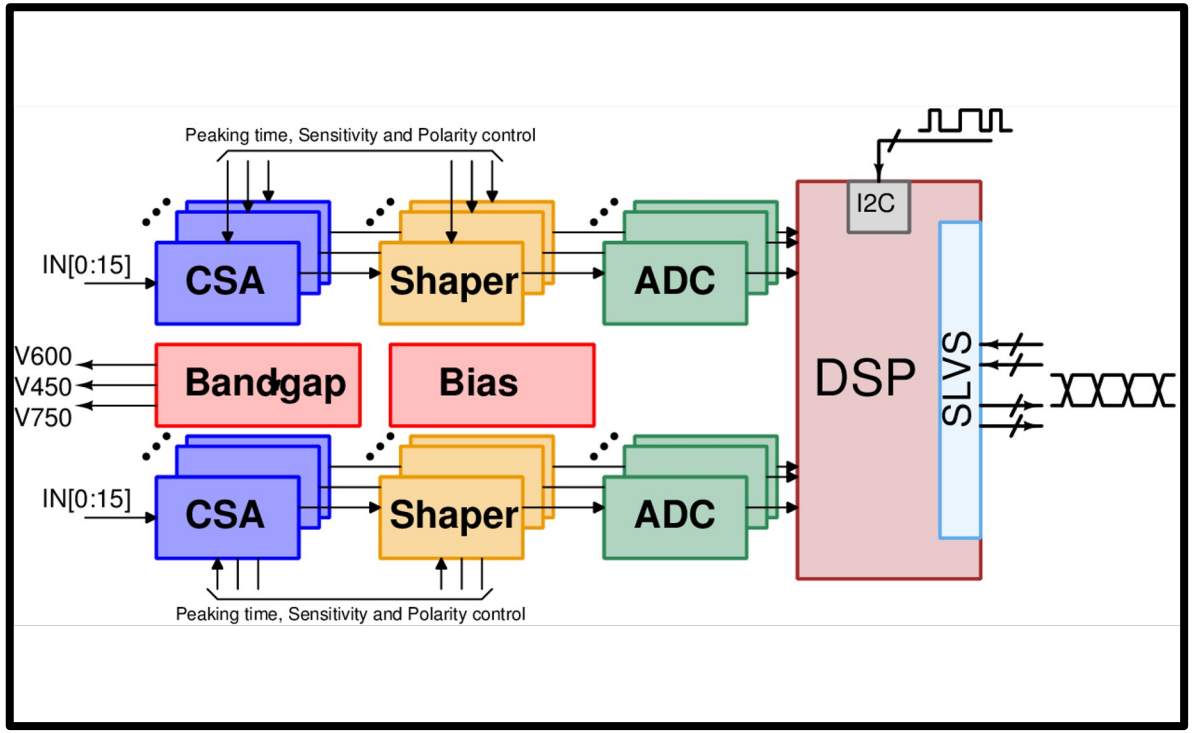
Here there is an interplay between ASIC developers and DAQ designers:

- what do we need/like to have?
- what’s the data bandwidth?

There are already some studies and presentation about possible streaming data collection by Irakli.

From my personal experience: SAMPA

One ASIC (preAmp, shaper, ADC, DSP), for 32 Chs



in some way SALSA aims to be a succesor of SAMPA. Let's see what was done here for streaming

What can be done: SAMPA example

- 4 primary filter blocks
  - Individual correction per channel
  - Baseline correction
    - 1 FIR filter
    - 1 Slope based filter
    - 1 IIR filter
    - Lookup table correction(Pedestal Memory) f(t);f(din)
    - Conversion f(din)
    - Fixed correction
  - Tail cancellation
    - 1 IIR filter

- Selectable number of serial links up to 11
  - 320/160/80Mbps
  - Channels divided among links, no load sharing
  - Which channel goes to which link and in which order can be selected
  - Data is packet based (header + payload)

- Configuration
  - Configurable through I2C
  - 1 global register unit, 32 sets of channel registers
- Radiation tolerant
  - TMR on almost all flip-flops
    - except on part of data path
  - Hamming protected headers

- Event modes
  - Triggered
  - Continuous
  - Selectable event length up to 1024 samples
  - 192 pre-trigger samples

- Event buffer per channel
  - 6144(6K) words of compressed samples
  - 256 words of headers
  - Header still created if data memory goes full

- Daisy chain
  - Multiple devices can share a single serial link to readout unit
  - 2K word buffer in the receiving side

- Direct ADC serialization
  - Data serialized directly from ADC at 32xADC speed over 10 links
  - Raw data, no filtering, no headers
  - Sync pattern on startup, receiver should maintain sync after that
  - 2 modes
    - 10 bits is sent consecutively for channel 0-31 each 32xADC cycle
    - 5 lower bits, then 5 higher bits consecutively for channel 0-15 is sent on link 0-4 and for channel 16-31 on link 5-9
  - Clockgate the rest of the system to save power

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what filters to be implemented
fundamental for data reduction
at FEE level !

drawback: it's HARD coded
(only configurables: registers)
defined years before experiment will run
and collect data

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A PROVOCATION

just stream the full data, do data reduction "later" by a FPGA based system
GOOD: algorithm can be adapted any time

drawback: huge bandwidth needed
definitevely not so practicable…

- Event modes
  - Triggered
  - Continuous
  - Selectable event length up to 1024 samples
  - 192 pre-trigger samples

- Event buffer per channel
  - 6144(6K) words of compressed samples
  - 256 words of headers
  - Header still created if data memory goes full

- Daisy chain
  - Multiple devices can share a single serial link to readout unit
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- Direct ADC serialization caveat: ALICE TPC use it at 5MSps
  - Data serialized directly from ADC at 32xADC speed over 10 links
  - Raw data, no filtering, no headers
  - Sync pattern on startup, receiver should maintain sync after that
  - 2 modes
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Status of SALSA project

Timeline

- Discussions and reflections on the project (2021-2022)
- SALSA0 prototypes to study first designs (2022-2023)
- SALSA0_analog featuring 4 front-end channels
- SALSA0_digital featuring an ADC block
- PRISME prototype for PLL block + first version of general services (2023)
- SALSA1 prototype to test full front-end + ADC chains, + simplified DSP (2023-2024)
- SALSA2 prototype to test fully featured ASIC, but with limited number of channels (2024-2025)
- SALSAf as pre-serial prototype with nominal number of channels if budget available (2025-2026)

Present status

- ✓ SALSA0 prototypes submitted in November 2022 and January 2023, received in June, SALSA0_analog already mounted in the test boards, SALSA0_digital presently being packaged
- ✓ Finalization of PRISME prototype design completed, submitted July 19th 2023 to TSMC
- ✓ At a first, quick, look SALSA0_analog seems fine
- In deep characterization of SALSA0, building blocks, is going to start in the forthcoming weeks
- Reflection on SALSA1 architecture ongoing, front-end - ADC interface in progress, submission foreseen beginning of 2024

Thanks!