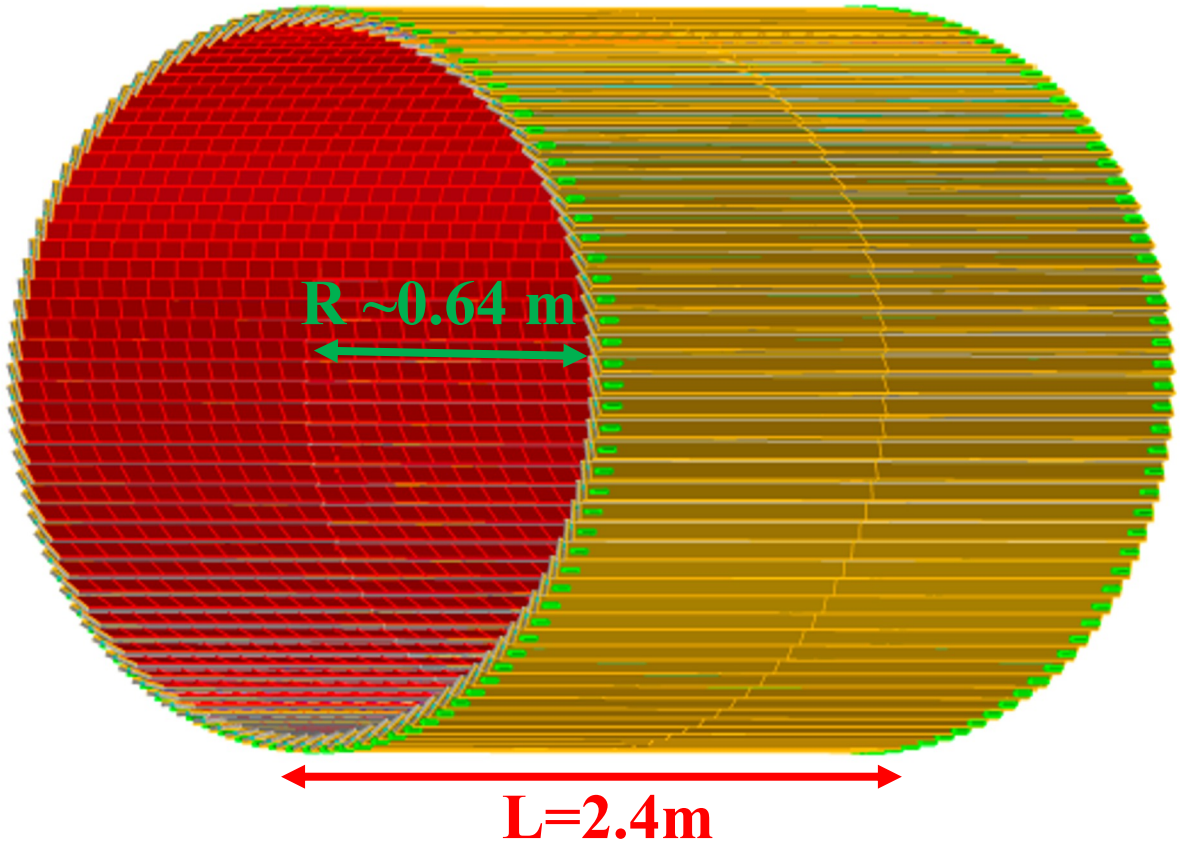
ePIC TOF DWG -> ePIC TOF DSC

- **ePIC AC-LGAD TOF Detector System**
  - Barrel: 1 cm*500 um strips, ~10 m^2, ~2M channels
  - Forward: 500*500 um^2 pixels, ~1.4 m^2, ~6M channels
- **TOF Detector Working Group**
  - Convener: Constantin Loizides (ORNL), Frank Geurts (Rice), Wei Li (Rice), Zhenyu Ye (UIC)
  - DAQ contact: Tonko Ljubicic (BNL)
  - Simulation contact: Nicholas Schmidt (ORNL)
  - LGAD consortium, eRD109 (ASIC & Electronics), eRD112 (Sensor & Mechanics)
- **TOF Detector Subsystem Collaboration**
  - **Nominated for DSL and Deputy DSL**: Zhenyu Ye (UIC), Satoshi Yano (Hiroshima University)
  - In the process of collecting institutional interests/responsibilities and defining working groups/packages
  - **Institutions**:
    - **USA**: Brookhaven National Laboratory, Los Alamos National Laboratory, Oak Ridge National Laboratory, Ohio State University, Purdue University, Rice University, University of California Santa Cruz, University of Illinois at Chicago
    - **Japan**: Hiroshima University, RIKEN, Shinshu University, University of Tokyo
    - **India**: IIT Mandi, National Institute of Science Education and Research
    - **Taiwan**: National Central University, National Cheng Kung University, National Taiwan University
    - **China**: South China Normal University, University of Science and Technology of China
    - …

Barrel TOF Layout

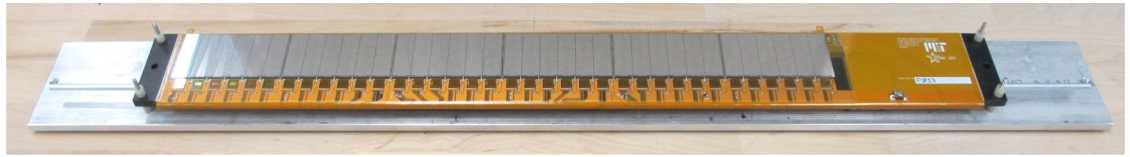
More details: https://indico.bnl.gov/event/16765/

ePIC Barrel TOF (~1% X_0)



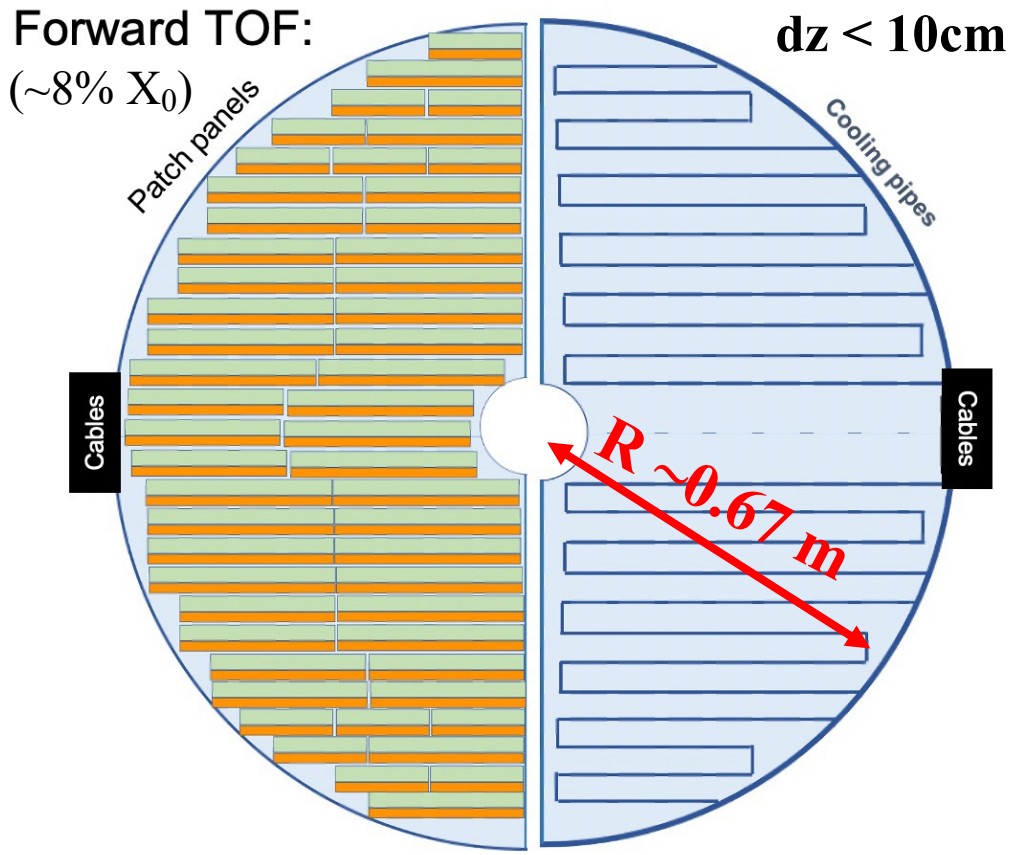
STAR Intermediate Silicon Tracker

- 288 staves, each with 32 strip sensors wire-bonded to 64 frontend ASICs on low mass Kapton flex and CF support
- Power consumption: ~4 kW for 500μm x 1cm strips (2.4 kW for ASIC, 1.0 kW for DC-DC, 0.6 kW for sensor+cable+RB)



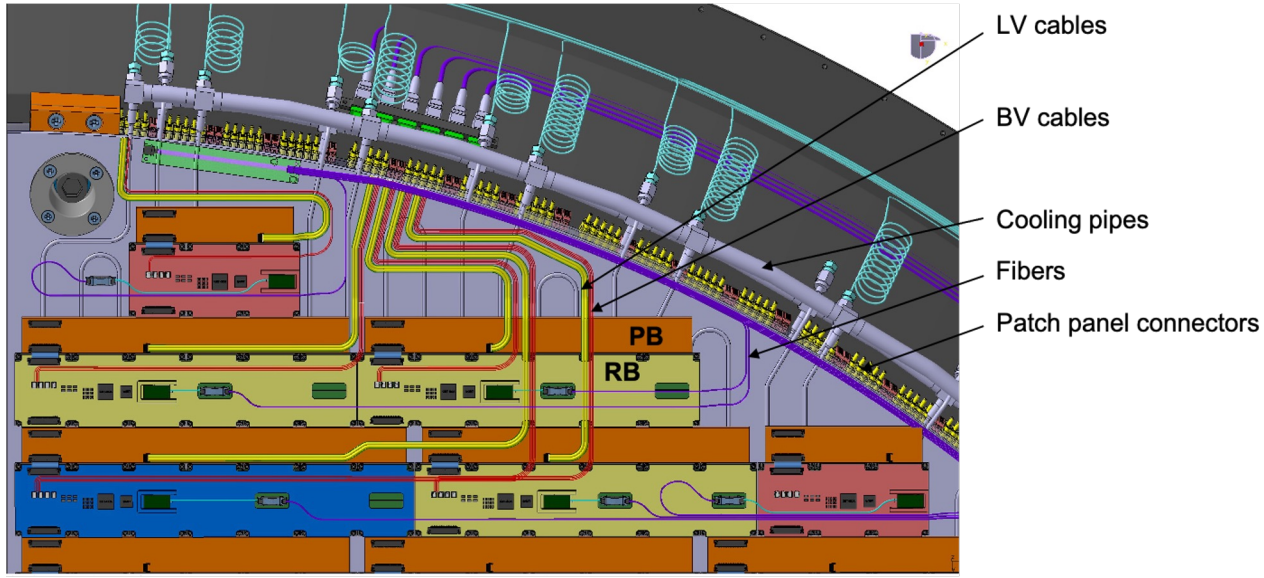
Forward TOF Layout

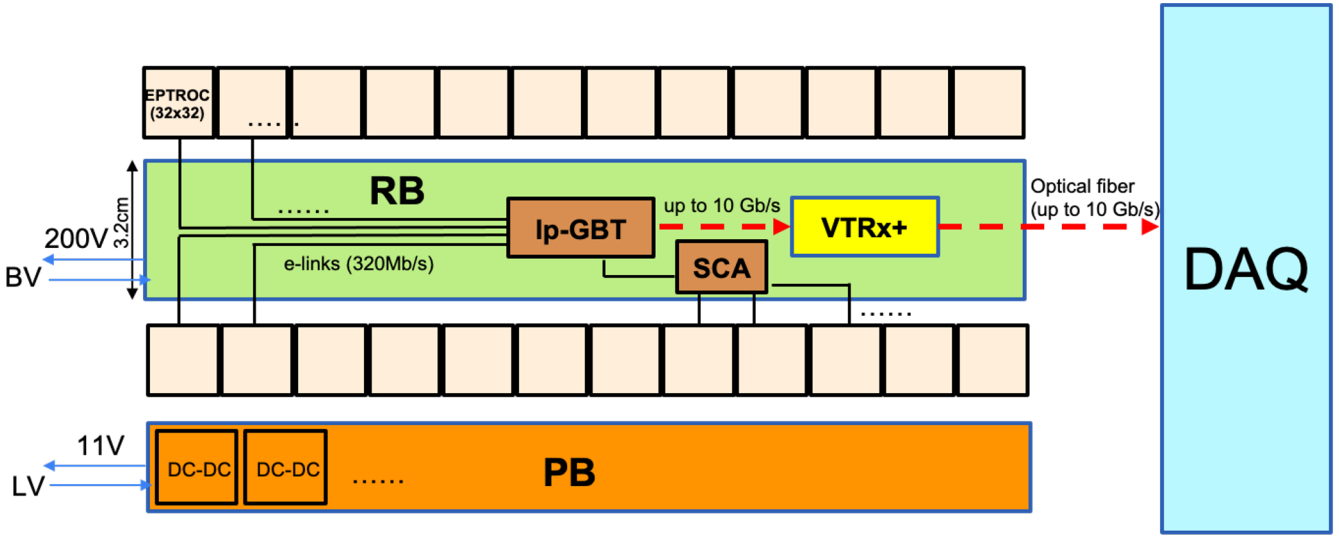
More details: https://indico.bnl.gov/event/17336/



- 212 modules, each with 24 to 96 bump-bonded pixel sensor + ASIC assemblies on Al disk
- Power consumption: 13 kW for 500x500 μm^2 pixels (6 kW for 800 x 800 μm^2)

CMS Endcap Timing Layer





TOF On-going/Planned Work

[1] https://wiki.bnl.gov/EPIC/index.php?title=TOFPID
[2] https://www.overleaf.com/read/vftxyvjtjrvp
[3] https://wiki.bnl.gov/conferences/index.php/ProjectRandDFY23

Simulation [1]

- DD4HEP geometry, digitization, reconstruction (**ORNL, UIC, Hiroshima, BNL, OSU**)
  - Timing resolution requirement
  - Spatial resolution requirement
  - Material budget requirement

Project Engineering and Design (PED) [2]

- Mechanical engineering (**NCKU/Purdue, ORNL**)
  - Mechanical support and services
  - Cooling system
- Electric engineering (**BNL within DAQ WG**)
  - Precision clock distribution (<5 ps)
  - Timing chips and streaming readout
  - Readout board

eRD112 [3]

- Sensor (**BNL-IO, UCSC, UIC/Fermilab, LANL, ORNL, Rice**)
  - BNL-IO, HPK and FBK productions
  - Lab/beam test, irradiation
- Sensor-ASIC integration (**UIC**)
- Module mechanical structure (**NCKU/Purdue**)
  - Low-density composite structure

eRD109 [3]

- Frontend ASIC:
  - EICROC (**IJCLab/OMEGA, BNL**)
  - FCFD (**Fermilab**)
  - Fast/HPSoC/ASROC (**UCSC**)
- Frontend electronics
  - Low-mass flexible Kapton PCB (**ORNL**)
  - Barrel TOF service hybrid (**ORNL**)
  - Endcap TOF service hybrid (**Rice**)

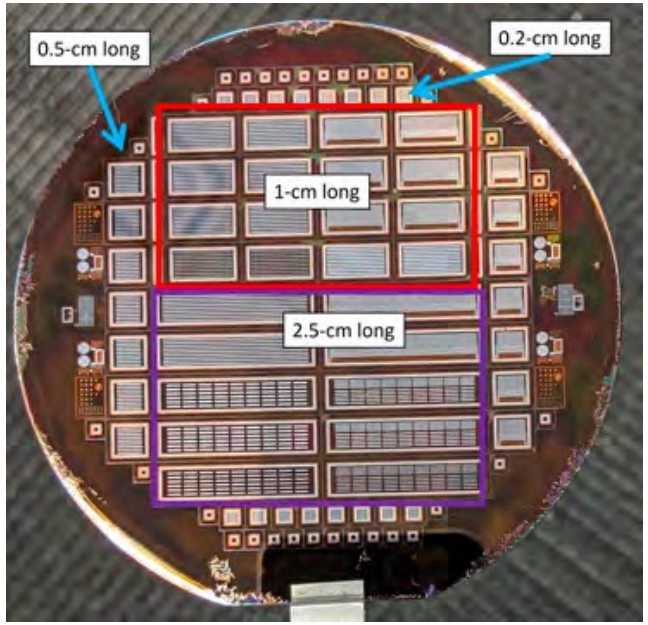
TOF in Simulation

- Status of the implementation of geometry/detector services/digitizer
  - Real BTOF material (~1%X_0) within the acceptance -1.4<eta<1.4, missing service outside the acceptance
  - Average FTOF material (5%X_0) within the acceptance 1.7<eta<3.7, missing service outside the acceptance
  - Digitizer has the correct timing and spatial resolution, but no charge sharing
- Are there open performance issues?
  - No open issue but improvements planned (see below)
- Are there any issues to be addressed?
  - Implement real FTOF geometry by Nicholas Schmidt (ORNL)
  - Implement charge sharing by Prithwish Tribedy (BNL) and Simone Mazza (UCSC)
  - Implement TOF services outside the TOF acceptance by TBD
- Real material/acceptance vs average material/acceptance
  - BToF: real material within the acceptance -1.4<eta<1.4, missing service outside the acceptance
  - FTOF: average material within the acceptance 1.7<eta<3.7, missing service outside the acceptance

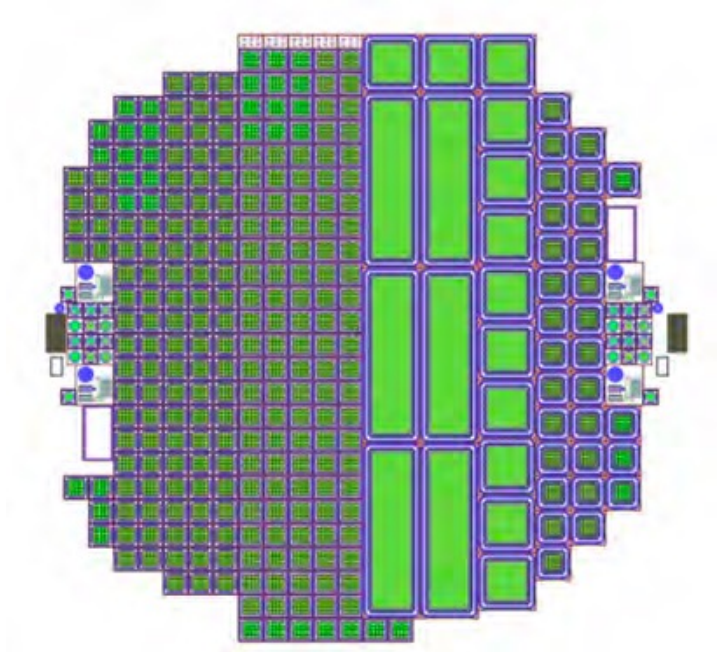
AC-LGAD Sensor R&D

- Production of medium/large area sensors with different doping concentration, pitch and gap sizes between electrodes and Si thickness to optimize performance by BNL IO and HPK.
  - 1st BNL (06/2021-11/2021): 5-25 mm strips with 500 μm pitch, 100-300 μm electrode width, 50 μm active Si
  - 2nd BNL (06/2022-11/2022): 5-25 mm strips with 500-700 μm pitch, 50-100 um electrode width, 20-50 μm Si
  - 3rd BNL (08/2022-12/2022): pixels with 500-700 μm pitch, various electrode shapes, 20-50 μm Si
  - 1st HPK (06/2022-04/2023): strip+pixel sensors with different electrode width, active thickness and n^+ doping
  - 4th BNL (02/2023-06/2023): deep gain layer to increase signal amplitudes

1st/2nd BNL Production

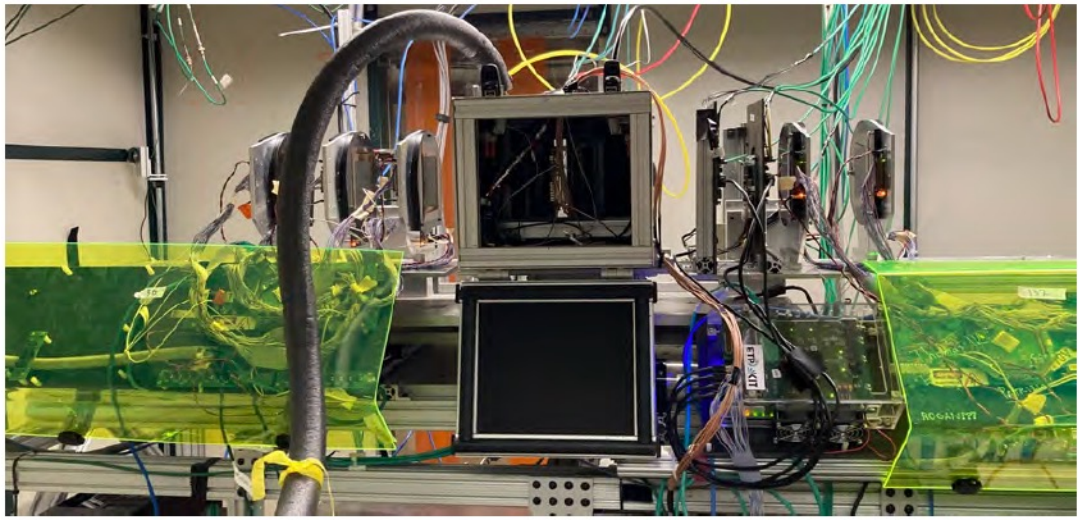


3rd BNL Production



Joint HPK Production

eRD112: 1st BNL AC-LGAD Sensor Production



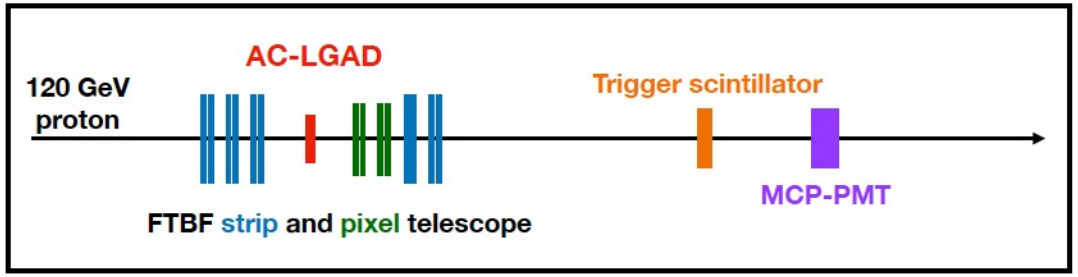


Figure 7: Picture (top) and diagram (bottom) of the FTBF silicon telescope and reference instruments used to characterize AC-LGAD performance. The telescope comprises five pairs of orthogonal strip layers and two pairs of pixel layers, for a total of up to 14 hits per track.

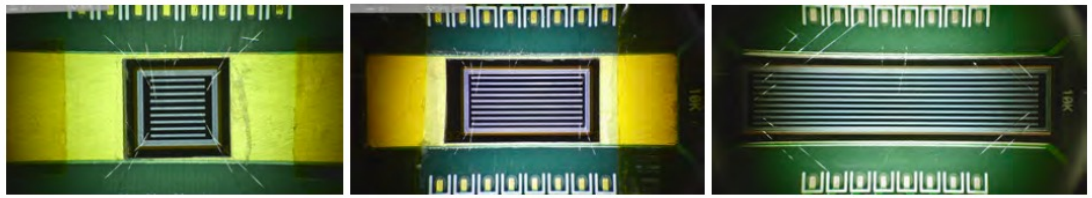
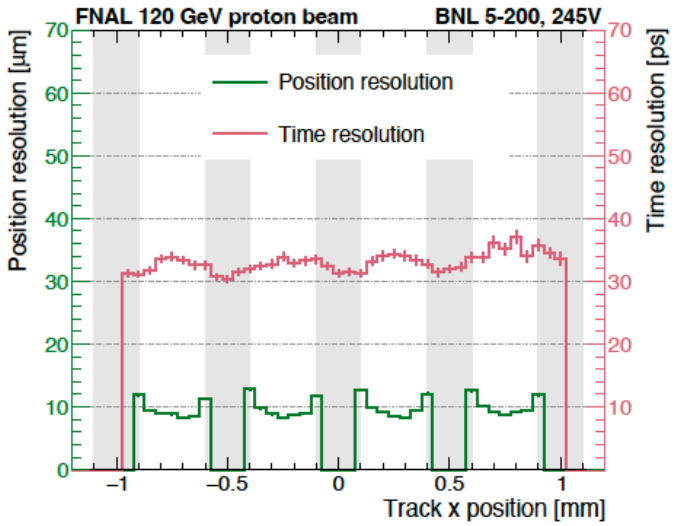
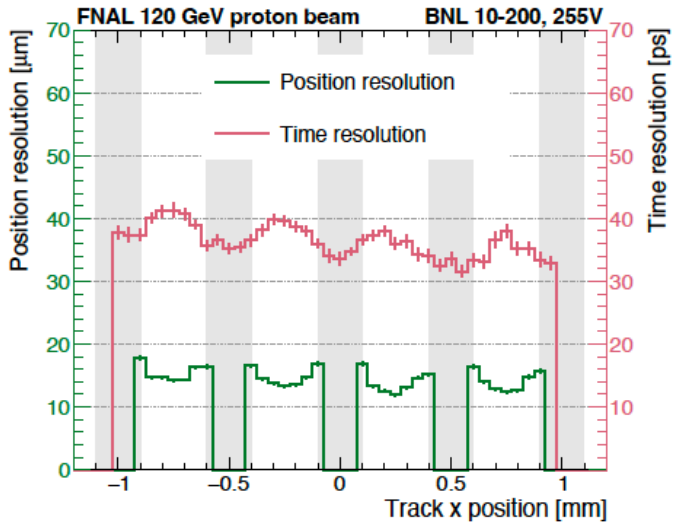


Figure 8: Three AC-LGAD strip sensors wire-bonded on Fermilab test board and tested at FTBF: BNL 5-200 (left), BNL 10-200 (middle) and BNL 25-200 (right). See text for details.





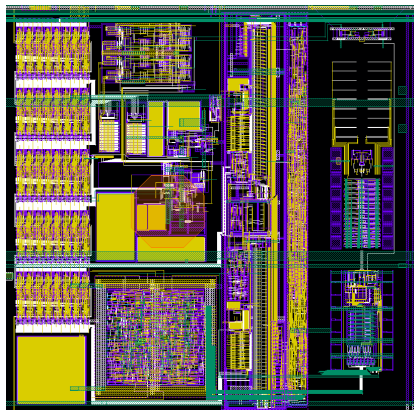
- Timing and spatial resolutions of 1 cm long strip sensors from 1st BNL production demonstrate good performance, making strip sensors a promising candidate for EIC applications.
- Production of medium/large area sensors by BNL IO and HPK with different doping concentration, pitch and gap sizes between electrodes and Si thickness to optimize performance.

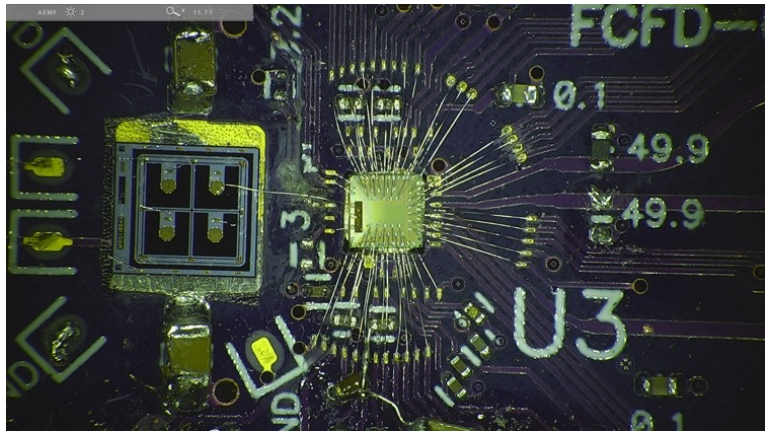
C. Madrid et al., arXiv:2211.09698

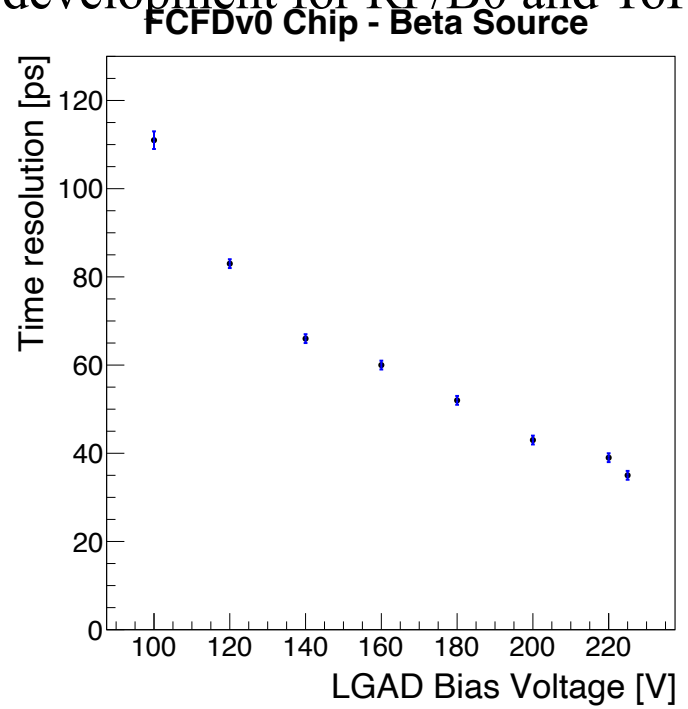
Frontend ASIC R&D

[7] eRD112 R&D Proposal

- **R&D Goals**
  - 15-20 ps jitter with minimal (1 mW/ch) power consumption, match AC LGAD sensors for EIC
- **Plan**
  - Continue the ASIC prototyping efforts and utilize the design and experience in ASICs for fast-timing detectors from ATLAS and CMS, and investigate common ASIC design and development for RP/B0 and ToF







EICROC by Omega/Irfu/AGH

- Preamp, discri. taken from ATLAS ALTIROC
- I2C slow control taken from CMS HGCROC
- TOA TDC adapted by IRFU Saclay
- ADC adapted to 8bits by AGH Krakow
- Digital readout: FIFO depth8 (200 ns)

FCFD by Fermilab

- Adapt the Constant Fraction Discriminator (CFD) principle in a pixel paired with a TDC, one time measurement gives the final answer.
- Charge injection consistent with simulations: ~30 ps at 5 fC, and <10 ps at 30 fC
- Tested with laser, beta source and beam

Possible Working Group Structure for TOF DSC

- **Barrel TOF**
  - **Sensor**: sensor, sensor-ASIC integration
  - **Frontend electronics**: ASIC, service hybrid
  - **Detector Module**: module structure, module assembly
- **Forward TOF**
  - **Sensor**: sensor, sensor-ASIC integration
  - **Frontend electronics**: ASIC, service hybrid
  - **Detector Module**: module structure, module assembly
- **Common systems**
  - **Backend Electronics**: power supplies, DAQ system
  - **Mechanics**: support structure, cooling system
  - **Alignment system**
  - **Slow control**
- **Detector Performance**
  - **Simulation and reconstruction**
  - **Database**