Status and Plan on FCFD

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May 16, 2023

Constant Fraction Discriminator ASIC (FCFD)

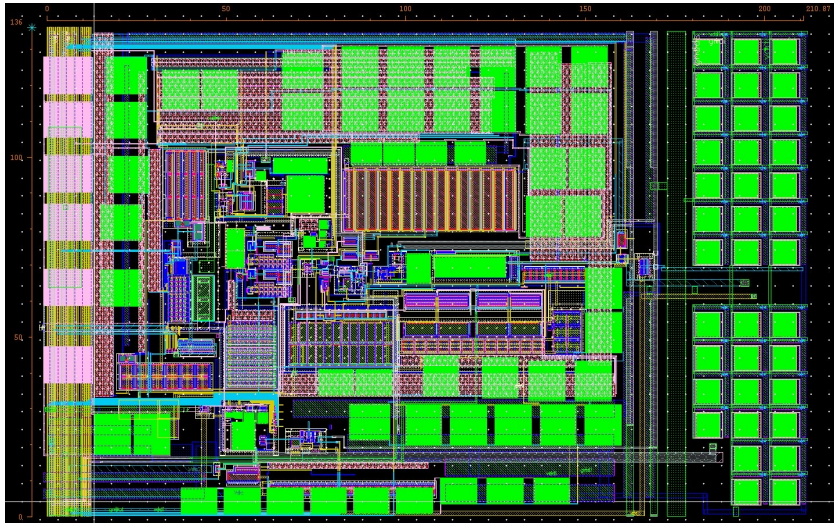
- Develop a robust fast-timing measurement technique for LGADs
  - Easy to use and stable: no corrections, or calibrations and threshold adjustments
- The first (FCFDv0) version was designed, produced and tested with DC-LGAD sensors
  - Excellent performance demonstrated with charge injection, laser and beta source
- The next version (FCFDv1) is being optimized with EIC sensor specifications
  - In close collaboration with the EIC detector experts and AC-LGAD developers
- CFD approach achieves better performance, especially for low S/N systems, such as LGADs **(NIM A 940 (2019), pp 119-124)**

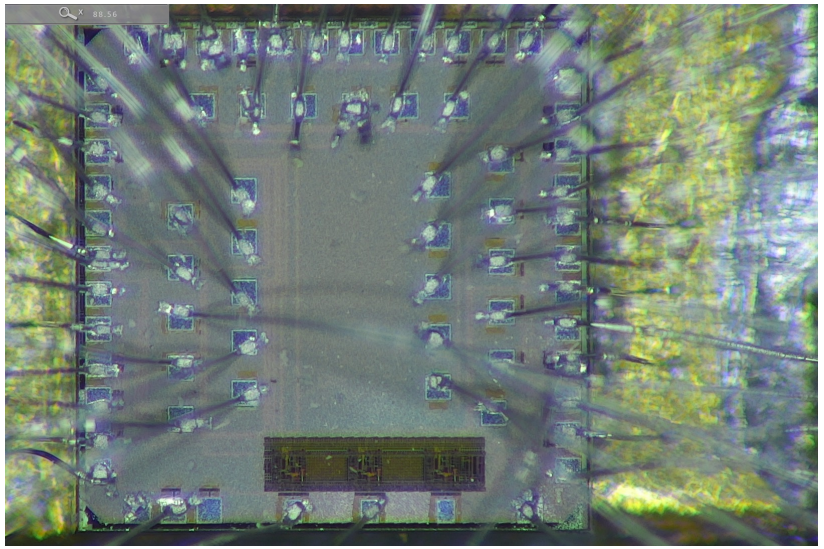
Advantages of CFD approach

- The difference was studied in detail in **NIM 940 (2019)**
  - At low signal amplitudes, CFD algorithm outperforms LE
  - CFD algorithm offers significant reduction in noise, as demonstrated in TOFHIR ASIC for CMS barrel timing detector
    - Improvement in the time resolution by x3.5 in TOFHIR
  - CFD-based readout is much simpler in operation and maintenance
    - No need to maintain the calibration and monitoring system, computing workflows, database maintenance, payloads, etc…
  - Power consumption for analog front-end LE and CFD comparable
    - Consumption for the digital parts is expected to be low, completed blocks exist

FCFDv0

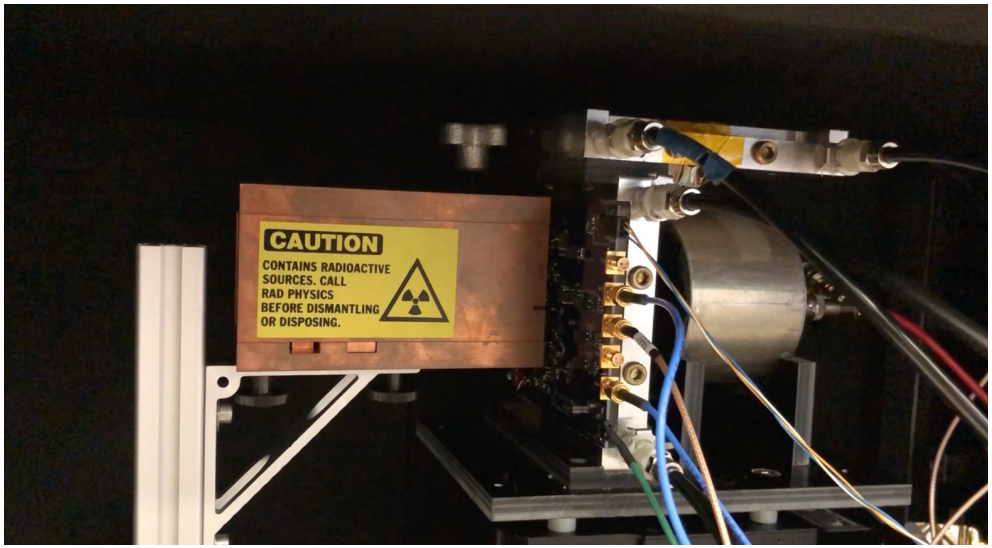
- First version of the chip to test and study the approach
  - Only analog output to measure the performance of the CFD approach
  - Measurements first performed using the internal charge injection circuit



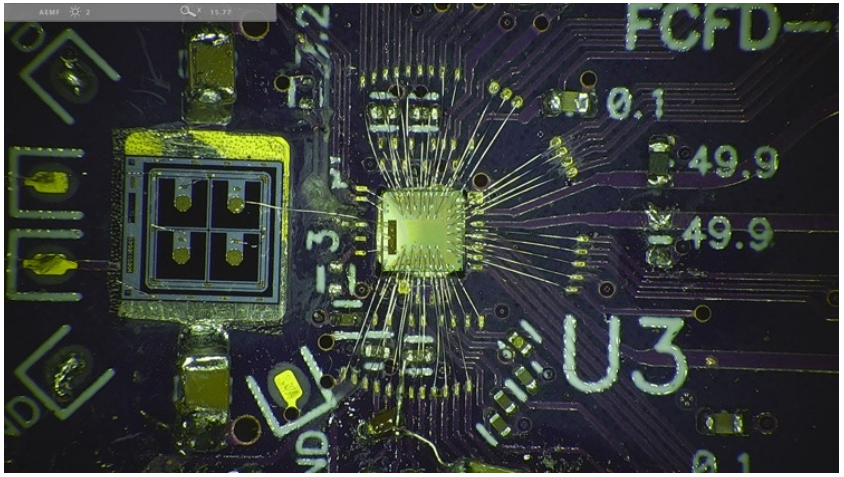


Beta-testing setup

- Board with sensor mounted inside environmental chamber in SiDet
- Tests have been performed with laser, beta-source, and test beam



Board mounted with β-source

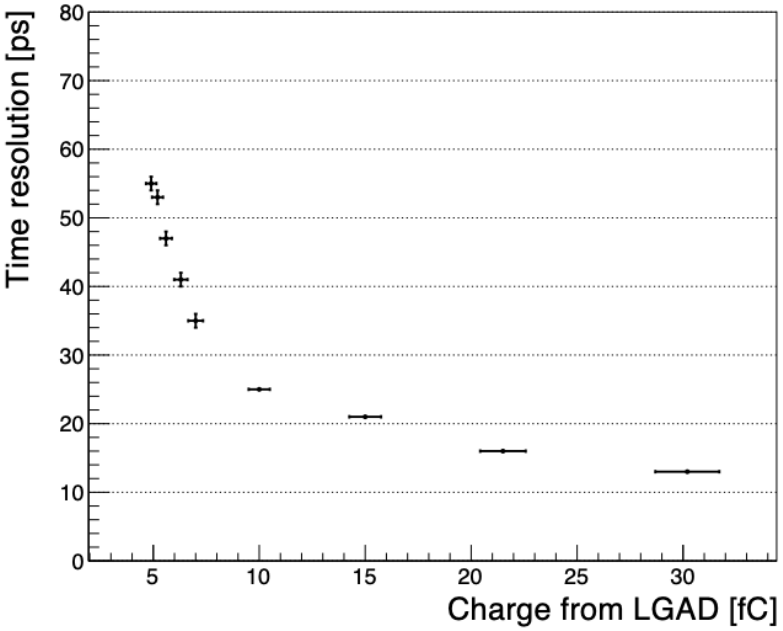


FCFD0 chip mounted to LGAD

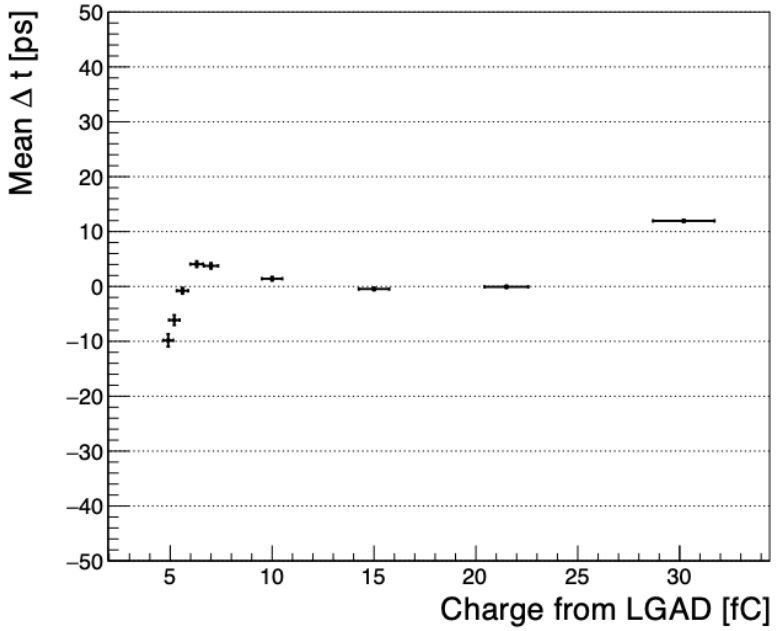
Fermilab

Timing ASIC with CFD

- Measurements with laser confirm the excellent intrinsic performance of the ASIC in time resolution and low jitter



Time resolution with 1.3x1.3 mm^2 LGAD sensor

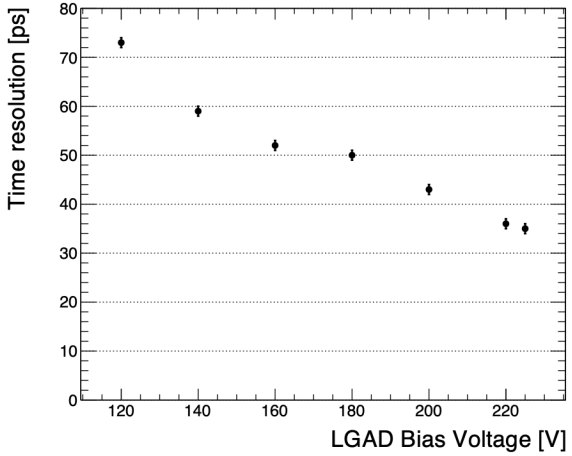


Jitter with 1.3x1.3 mm^2 LGAD sensor

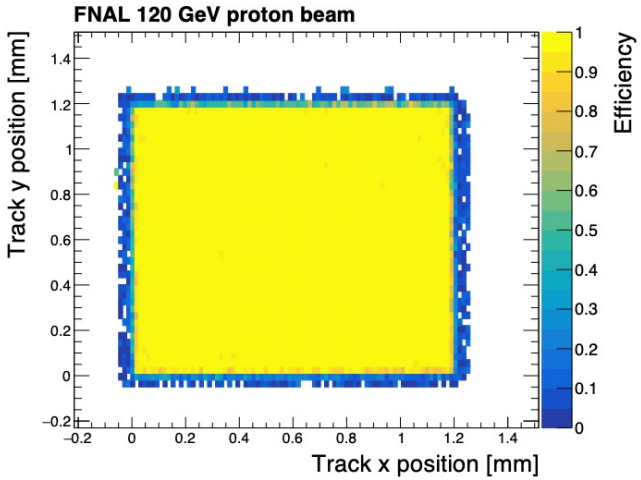
Fermilab

Timing ASIC with CFD

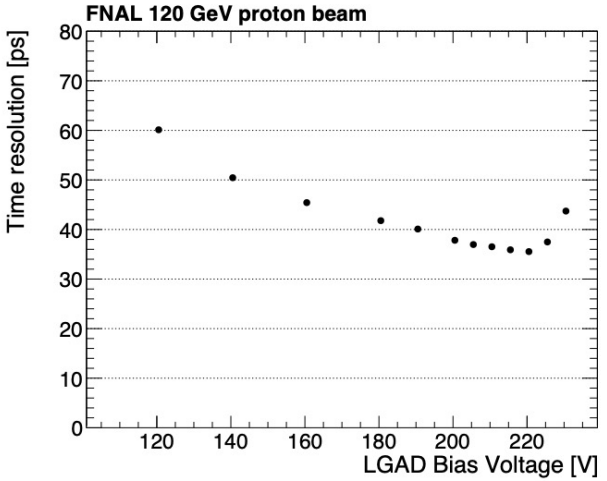
- Measurements with beta-source and test beam demonstrate performance with real signals and uniform response over the full sensor area



Beta source



Test Beam at Fermilab: hit efficiency over sensor surface



Test Beam at Fermilab

Development plans for 2023 (presented in Jan, 2023)

- Develop the next version targeting EIC AC-LGADs
  - Focus on AC-LGAD readout which needs both amplitude and timing information from each channel
  - Extended dynamic range for readout of smaller signals from AC-LGAD
  - Multichannel chip for AC-LGAD strip detector, 10 channels
  - ADC for amplitude readout
- Preliminary specs from our test-beam studies of AC-LGADs
  - AC-LGADs with 500 μm pitch and 1.0 cm length of strips
  - Details have been presented in previous eRD112 meetings
- Will also develop the readout board to wire-bond to AC-LGAD sensors
  - To be used for measurements with laser, source and beams

Timeline and milestones in 2023 (from Jan, 2023)

- Finish the design in Spring 2023
- Receive back from TSMC: Summer 2023
  - After the chip is submitted, design and submit the readout board for testing the ASIC coupled with AC-LGAD strip sensors
- Testing of FCFDv1
  - Initial bench testing with charge injection: late Summer 2023
  - Testing with beta-source and laser: Fall 2023
  - Test-beam once Fermilab Test Beam comes online: Fall-Winter 2023

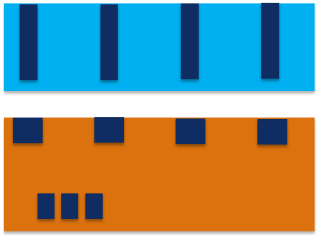
Developments in 2024 and 2025

- After the successful demonstration of the system readout with a multi-channel system during FY23
  - In 2024 focus on the full chip: full-size FCFDv2
    - If the sensor geometry is not finalized yet, we could target a scaled-down version to demonstrate the rest of the system.
    - Complete system including the digital readout that would interface with the EIC experimental DAQ
- The final, mixed-signal ASIC will be produced and tested during FY25, and its performance will be characterized using a single-layer AC-LGAD demonstrator at FTBF

Design status

- The chip design is finished, now working on the final layout
- Submission reserved for July 19 through Europractice MPW
  - Assuming 500 µm pitch sensors means for 10 channels the ASIC needs to be at least 5 mm long.
  - Wirebond-pads need to be arranged for various input and output signals, powers, grounds, monitoring etc.
  - Chip periphery becomes very crowded and need to increase the area to accommodate all pads.
- Cost scales linearly with area:
  - Quotation: 5x2 mm2 EUR 37,000, 5x1 EUR 18,500
  - We requested $40k for funding FCFDv1 costs from eRD109 ($25k for submission and $15k for readout boards)

Size optimization



- No need for 10 channels prototype to demonstrate performance
  - Main goals are to demonstrate the **wider dynamic range** and **amplitude readout** for position measurement
  - These goals can be achieved with 5 or 6 channels
  - 6-ch ASIC will provide 4 “groups” of 3-channels to perform **position measurements**, sufficient for qualification &uniformity of timing precision
- After optimization converged on **3.5 x 2.0 mm^2**
  - We will make the chip wider, and place the pads on the sides
  - Allows placement of all needed pads, some of them in 3 rows

Conclusion

- Studies of FCFDv0 very encouraging, good performance and simple operation
- Design of FCFDv1 focused on adapting the ASIC for EIC style AC-LGAD sensors
  - Wider dynamic range and addition of charge measurement for position reconstruction
  - Design is now complete, working on the layout now
  - Submission reserved for mid-July