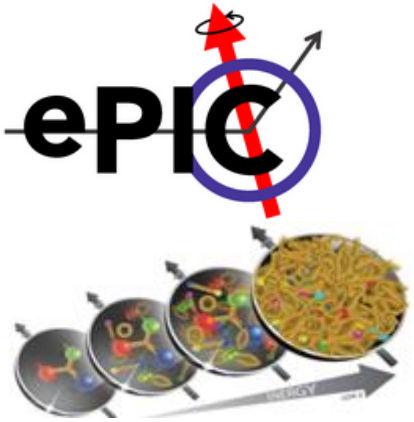


DOE/eRD109

The EICROC Project

Update on EICROC0 testing effort at IJCLab and perspectives

eRD112/ AC-LGAD meeting, 06/06/2023

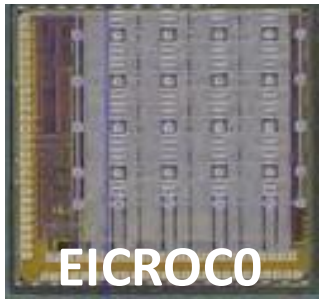
Dominique Marchand

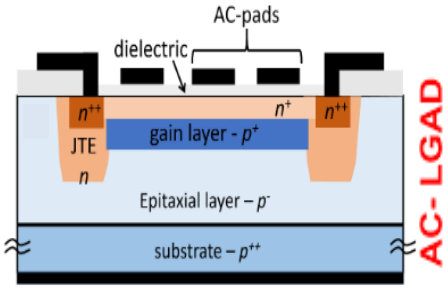
on behalf of the EICROC Project Team

Ultimate objective: **Development** and **characterization** of an **ASIC EICROC (32 x 32)** able to read-out the new generation of pixelated (500 x 500 μm^2) silicon sensors: **AC-LGAD** (**L**ow-**G**ain **A**valanche **D**iode) coupled **AC** for the **Electron Ion Collider** (EIC) Far Forward detectors: the **Roman Pots**

OUTLINE

Present objective: **ASIC prototype (EICROC0 : 16 channels, 4 x 4) design and characterization** dedicated to the read-out of **AC-LGAD** pixelated silicon sensors (500 x 500 μm^2) for the **EIC Roman Pots**





4D reconstruction (timing & position)

- **EICROC0 Requirements**
- **EICROC0 Design**
- **EICROC test bench @ IJCLab (Orsay, France)**
- **Progress report on EICROC0 characterization**
  - **Charge injection system**
  - **TZ Pre Amplifier Probe output signals: amplitude versus injected charge**
  - **TDC Performance**
  - **ADC Performance**
- **Summary**
- **Perspectives**
- **EICROC Project status**

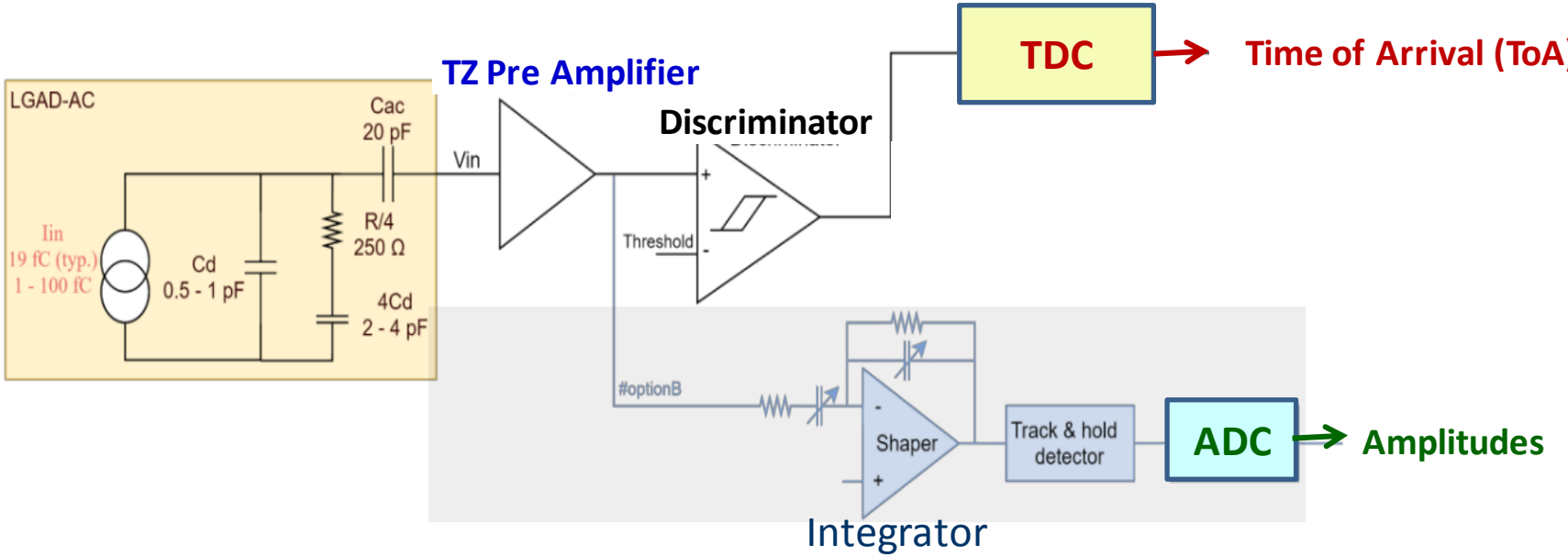
EICROC0 requirements and design: 16 channels (4x4)

Requirements:
- pixel size **0.5 x 0.5 mm²** *(HGTD 1.3x1.3 mm²)*
- low power consumption < **2 mW/channel**
- low jitter **~ 20 ps**
- low noise **~ 1 mV/channel**
- sensitivity to low charge **(2 fC)**

Charge sharing studies (simulation + β source w/ ALTIROC1_v2)

EICROC0 design:
- **TZ Pre Amplifiers** from ALTIROC (ATLAS/HGTD)
- 10 bit **TDC** from HGCROC (CMS, CEA/Irfu/DEDIP)
- **8 bit ADC** for time-walk correction (AGH Krakow, adapted from HGCROC)

1 channel (1 pixel) schematics

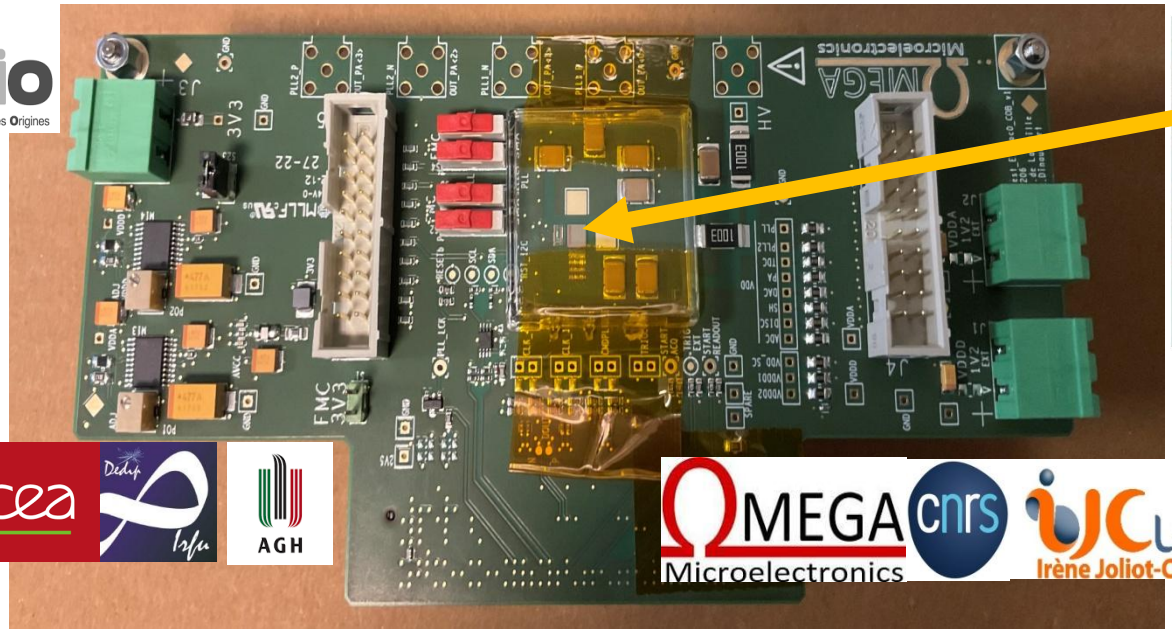


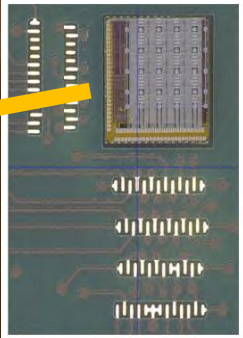
Compared to ALTIROC, ToT TDC (non-linear behavior versus the deposited charge) replaced by an ADC (8 bits)

EICROC0: EIC Roman Pots 4x4 AC-LGAD readout test chip

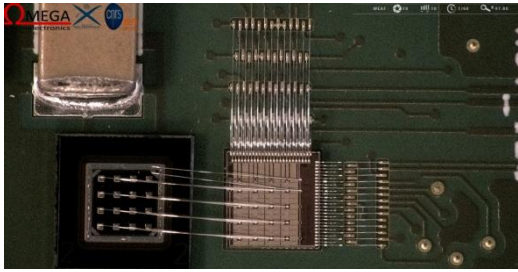
- Submitted through a Multi Project Wafer (**130 nm** CMOS technology) in March 22
  EICROC0 chips delivered mid-July 22
- **Test board** (PCB) designed by OMEGA, 10 pieces **delivered end of July 22**
  - test board partially cabled by IJCLab
- **Wire-bonding** of EICROC0 to test boards by **BNL collaborators**
- Delivery at IJCLab of 3 test boards w/ EICROC0 chip in **Oct. 22**
- Interface board (Xilinx ZC 706): (I^2C communication)firmware/software developments (IJCLab)

EICROC0 Test board





EICROC0 chip



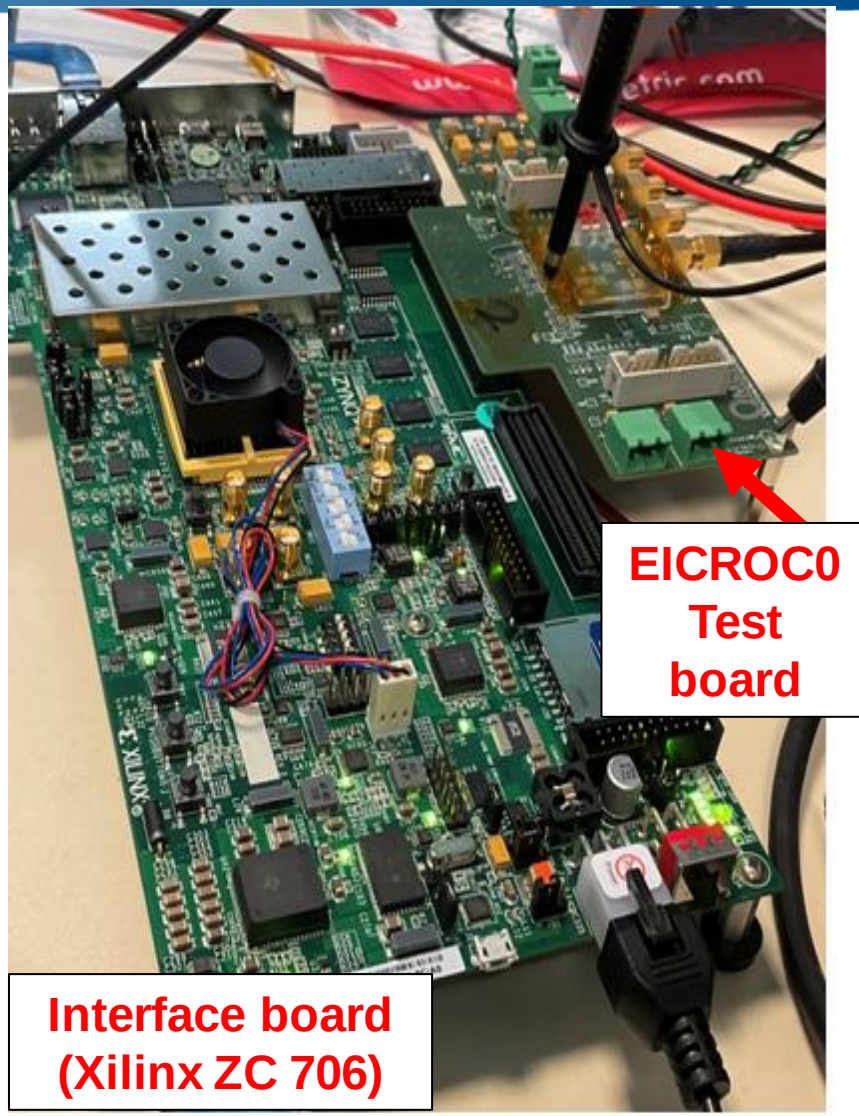
Status of EICROC0 Test Bench at IJCLab

- ✓ I^2C communication (firmware dev.)
- ✓ Data stream written/read
- ✓ EICROC0 DC levels
- ✓ Discri. threshold exploration
- ✓ **EICROC0 charge injection system fixed**
- ✓ **EICROC0 decoding (TDC, ADC) Firmware + software updated**
- ✓ **External trigger**: *signal directly injected into TDC*
  (No input into Pre Amplifier nor discriminator)

EICROC0 test bench operational since March '23

Preliminary studies [board #2 w/ EICROC0, no AC-LGAD]

- Characterization of the charge injection system
- Pre Amplifier output signal amplitudes vs injected charge
- Noise evaluation & evaluation of couplings to 160 MHz clock
- TDC performance
- ADC performance



EICROC0 Charge Injection System: « CMD Pulse »

In configuration file: Global parameter: Register **0x20C** dacb_pulser [**0** (Max value) -> **63** (Min value)]

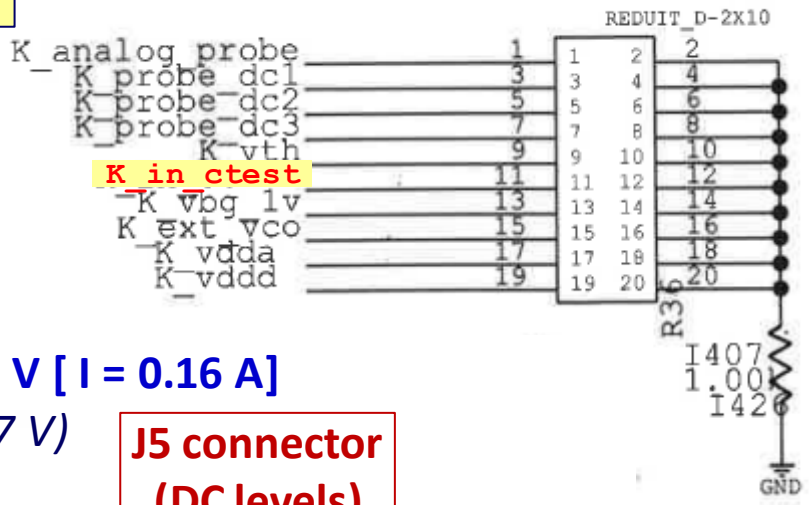
Measurements of **K_in_ctest** (DC level) versus dacb_pulser value

	Board #2	
Reg 0x20C dacb_pulser value	**Tension [mV]**	**Charge [fC]**
0	249,1	24,91
1	245,3	24,53
2	241,4	24,14
4	233,4	23,34
8	218,2	21,82
16	187,3	18,73
32	124,8	12,48
63	5,05	0,505

Q [fC] = **C** [fF] x **U** [mV]

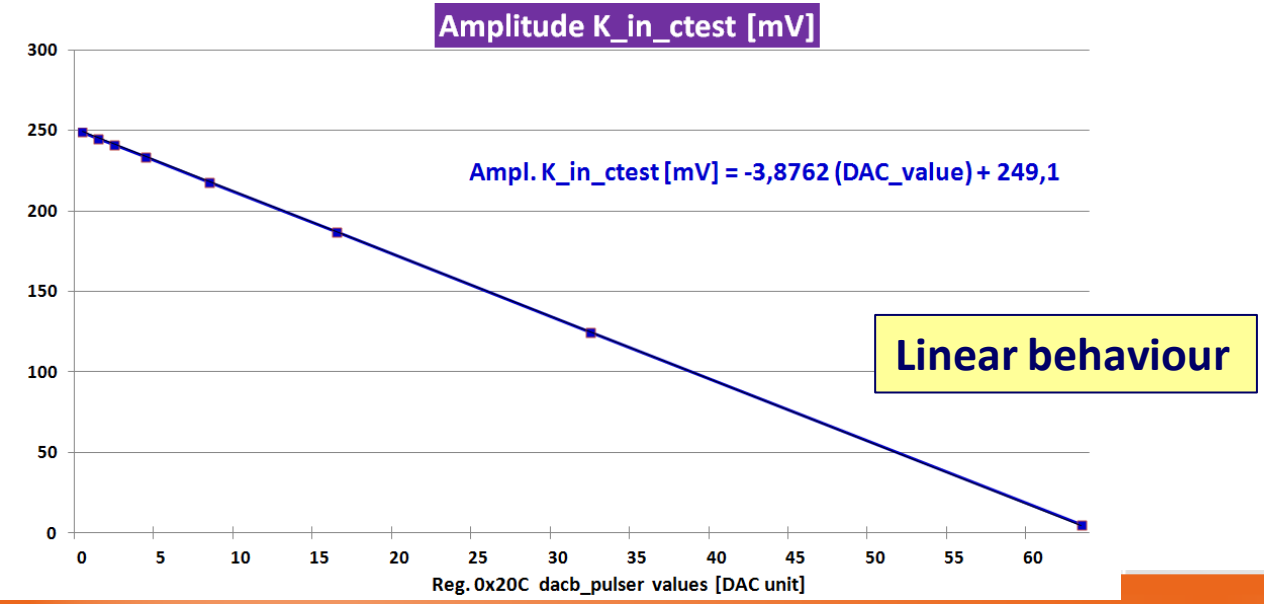
***C** = 100 fF*

J5 connector



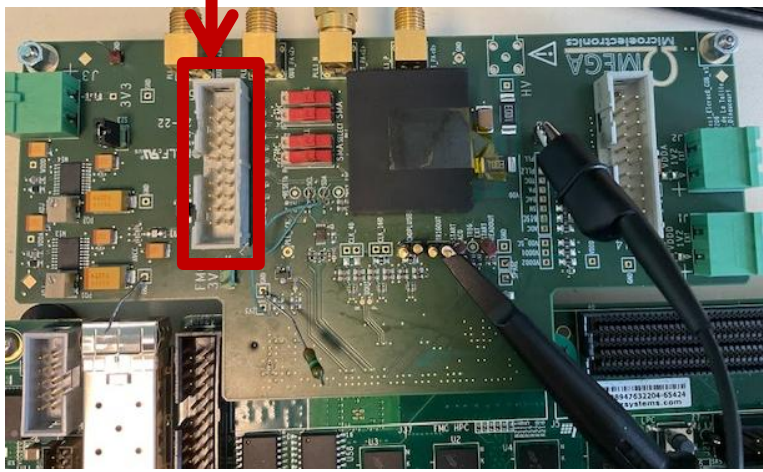
Board #2 Voltage applied: 3.3 V [I = 0.16 A]

(VDDD = 1.203 V ; VDDA = 1.207 V)



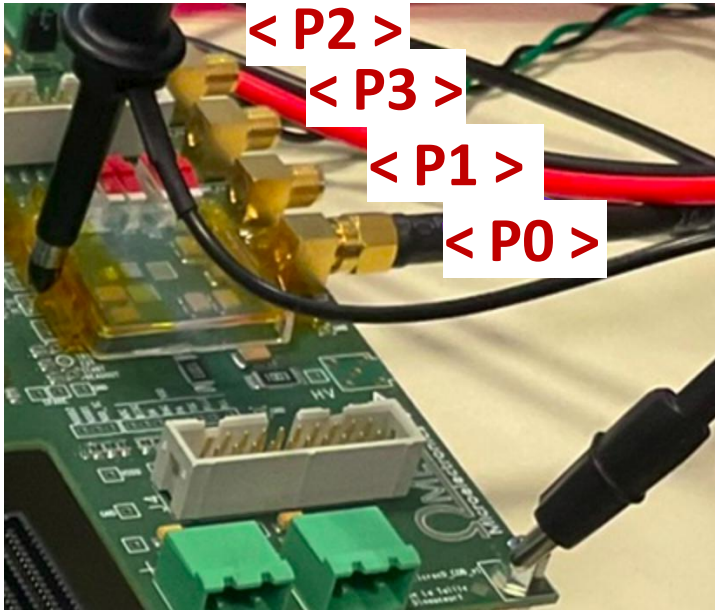
Linear behaviour

J5 connector (DC levels)



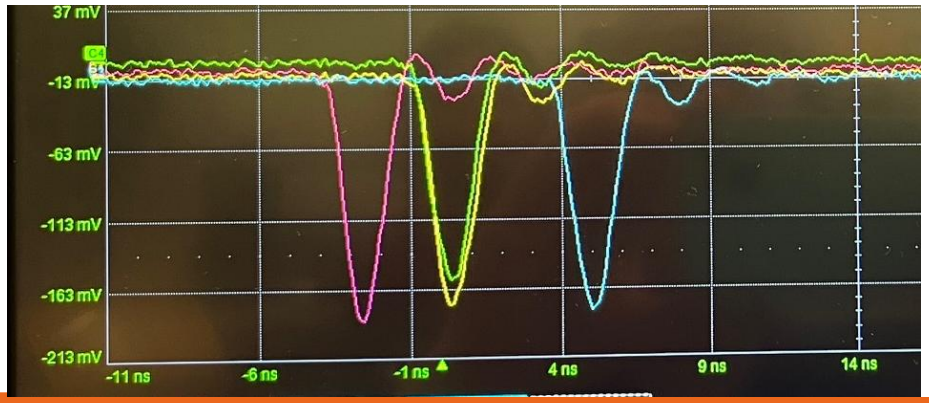
EICROC0 TZ Pre Amplifier Probe output signals

Pixel / Channel Mapping	Column 0	Column 1	Column 2	Column 3
Line 0	Pixel (**0**,0) **#00**	Pixel (**1**,0) **#04**	Pixel (**2**,0) **#08**	Pixel (**3**,0) **#12**
Line 1	Pixel (**0**,1) **#01**	Pixel (**1**,1) **#05**	Pixel (**2**,1) **#09**	Pixel (**3**,1) **#13**
Line 2	Pixel (**0**,2) **#02**	Pixel (**1**,2) **#06**	Pixel (**2**,2) **#10**	Pixel (**3**,2) **#14**
Line 3	Pixel (**0**,3) **#03**	Pixel (**1**,3) **#07**	Pixel (**2**,3) **#11**	Pixel (**3**,3) **#15**



PA output signals through SMA connector s (PCB back plane)

< P# > : Probe PA associated to **column** #



Feature of EICROC0:

Observing 4 Probe PA channels simultaneously

1 Probe PA per column

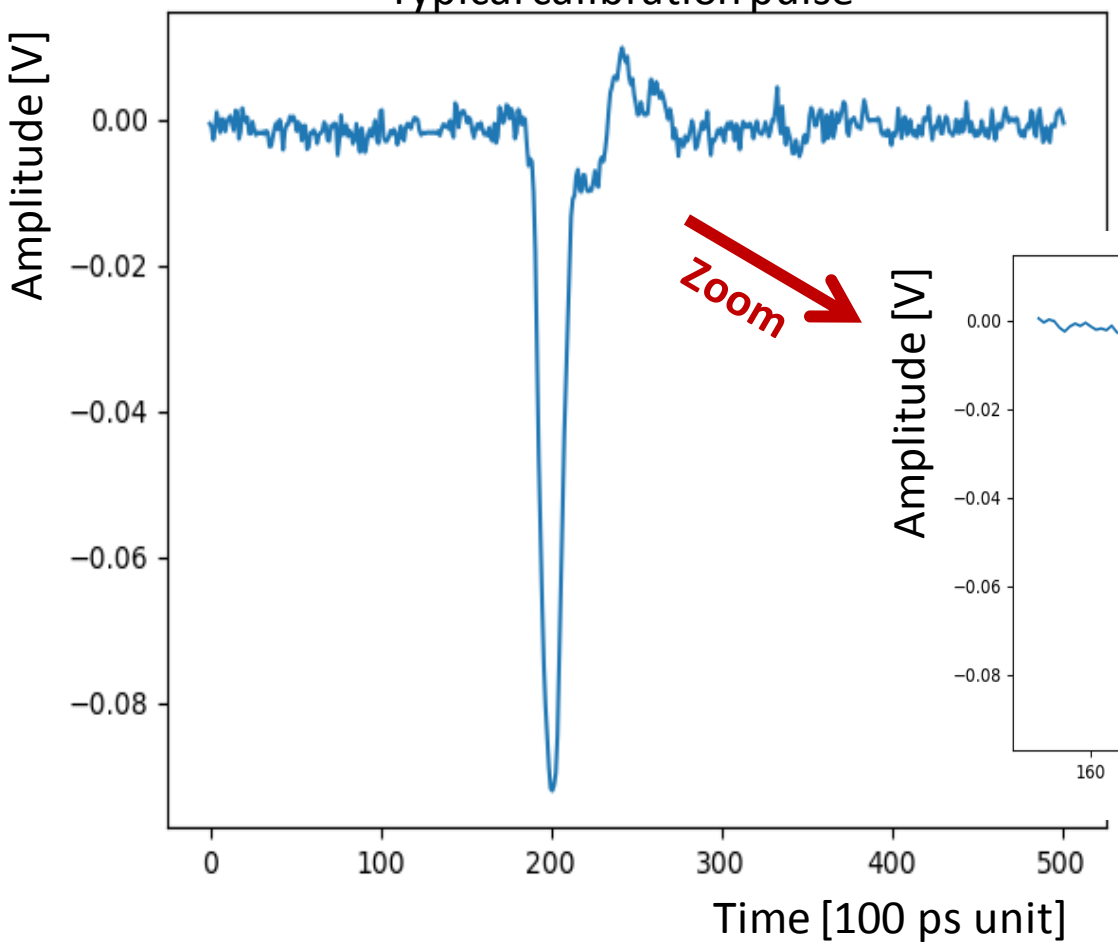
Ex.: #00, #04, #08, #12

EICROC0 TZ Pre Amplifier Probe output signal amplitudes (1)

Look at preamplifier probe output (one probe PA per column). **Input charge 12.5 fC** (CMD pulse 125 mV)

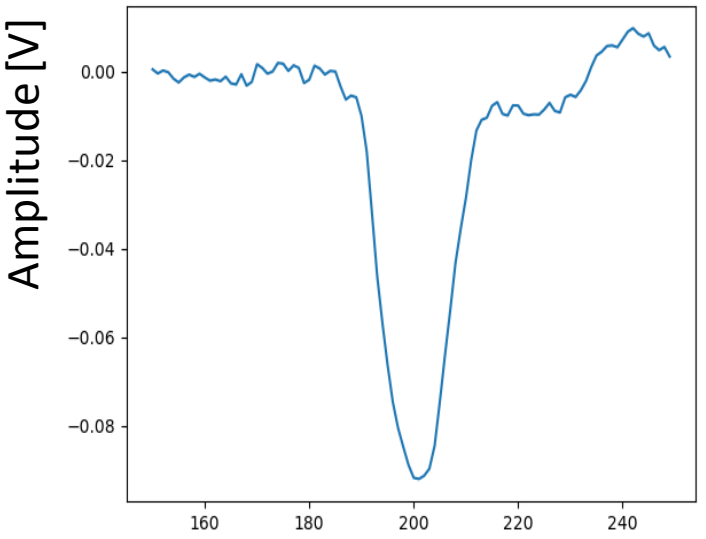
(Channel #8)

Typical calibration pulse



|Max. Amplitude| 95.5 mV

RMS 0.6 ns



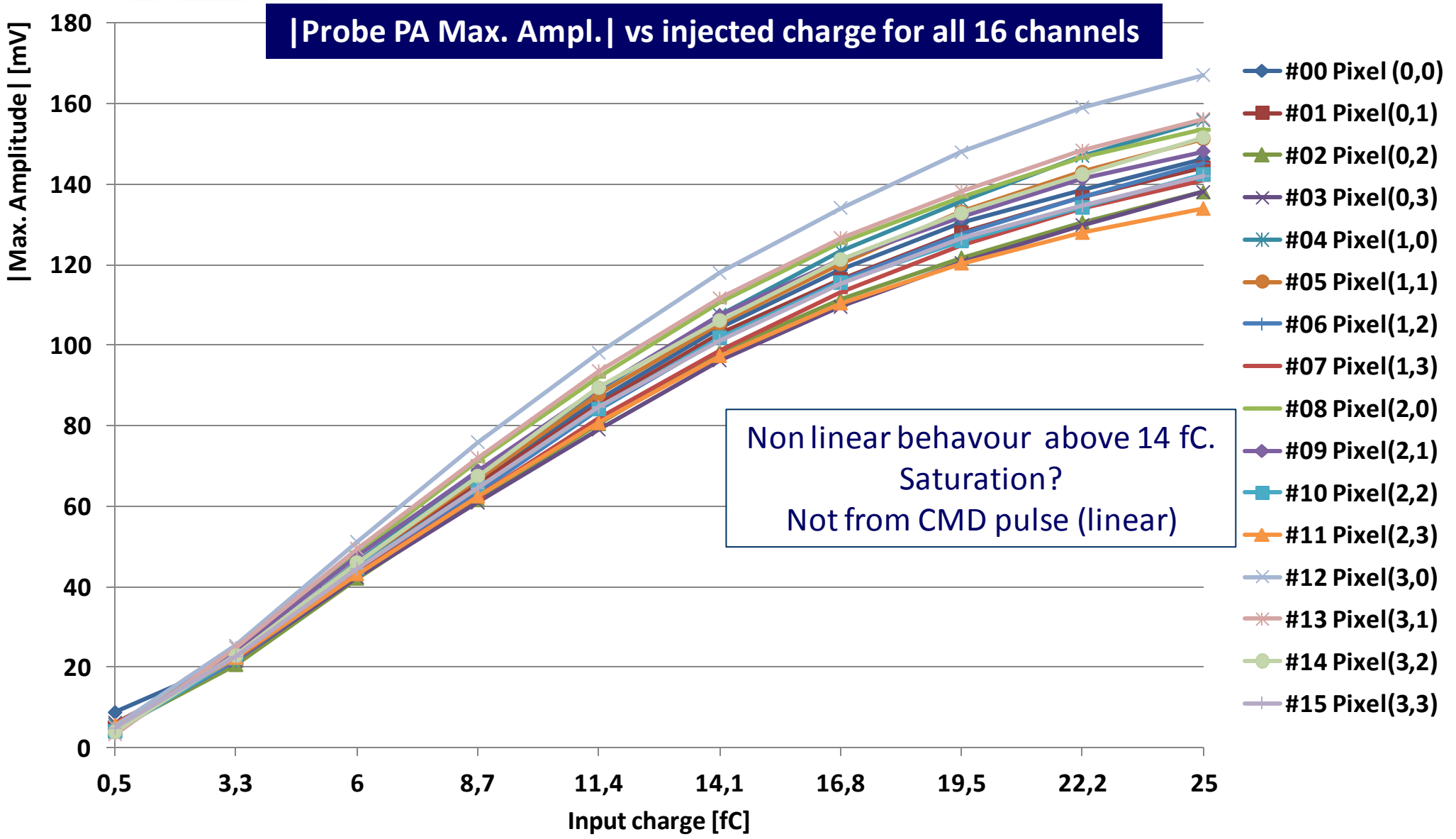
(scope units)

Rise (Fall) Time (RT) computed between 10% and 90% of |Max. - Ampl.|

RT 0.7 ns

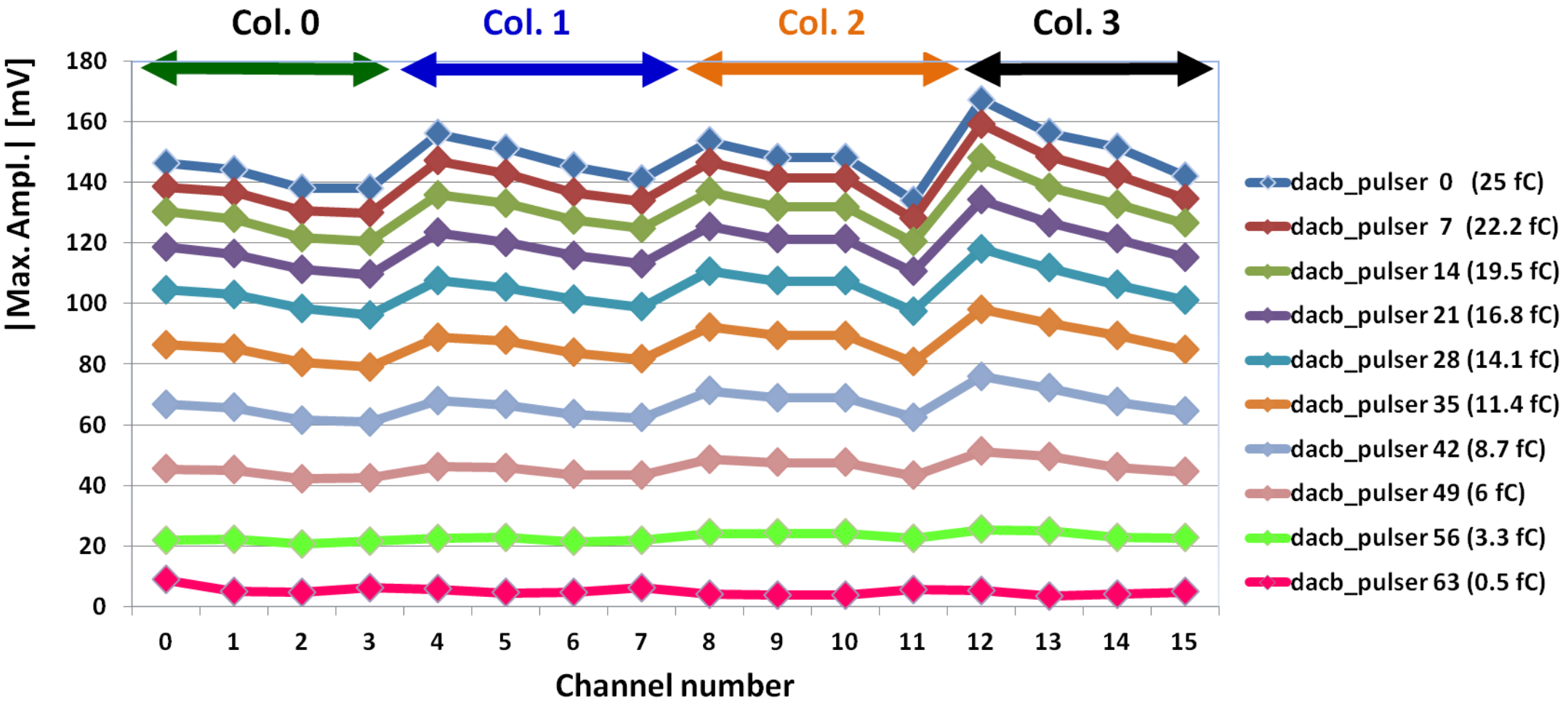
50Ω scope termination for each channel

EICROC0 TZ Pre Amplifier Probe output signal amplitudes (5)

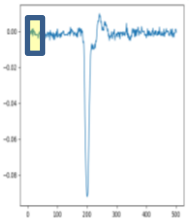


EICROC0 TZ Pre Amplifier Probe output signal amplitudes (4)

|Probe PA Max. Ampl.| vs channel number for several dacb_pulser value

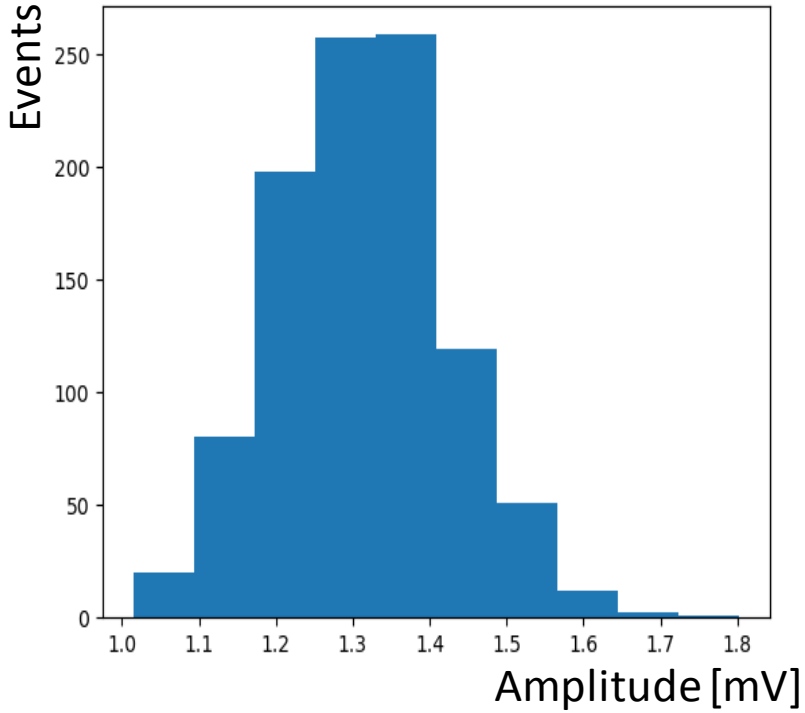


EICROC0 TZ Pre Amplifier Probe output signal amplitudes (2)



"Amplitude" refers as |peak amplitude|

PA signal RMS Distribution
(50 samples, first 5 ns time range)

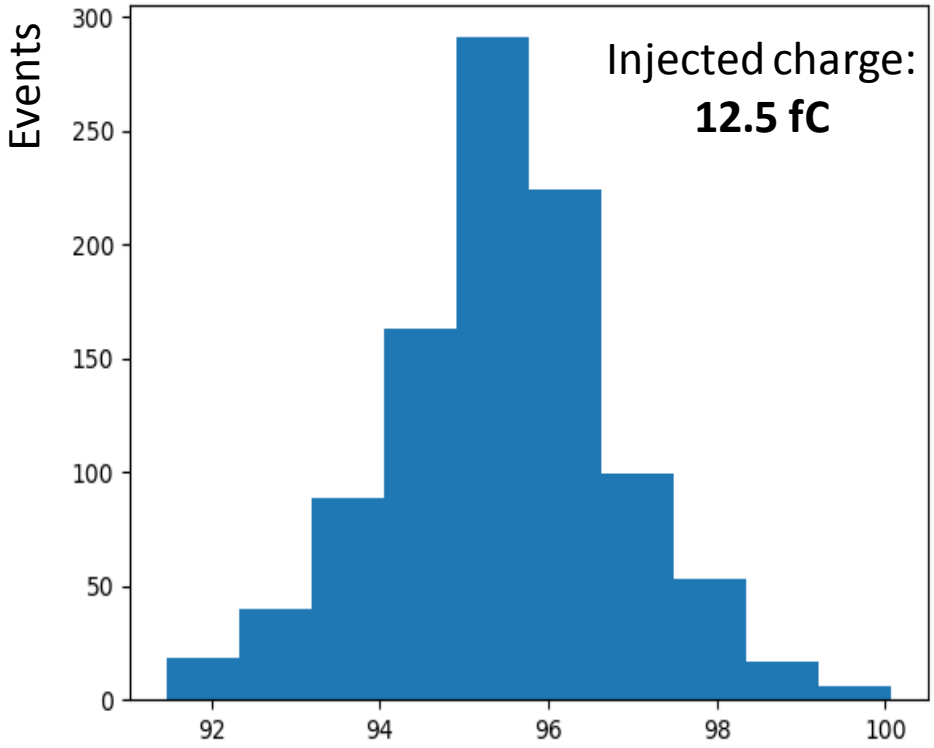


< Noise > = 1.31 mV

→ **S/N > 70** for 12.5 fC input *(95.5/1.31)*

→ Expect **S/N > 5** for 1 fC input

PA |Amplitude| Distribution

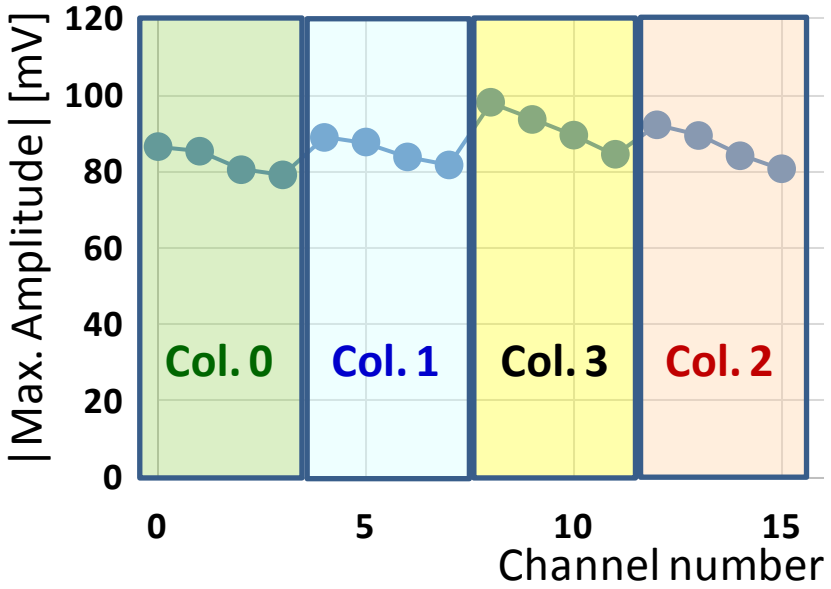


< |Max. Amplitude| > 95.5 mV, RMS 1.36 mV

(Channel #8)

EICROC0 TZ Pre Amplifier Probe output signal amplitudes (3)

PA |Max. Amplitude| vs channel number
(13.8 fC input charge)

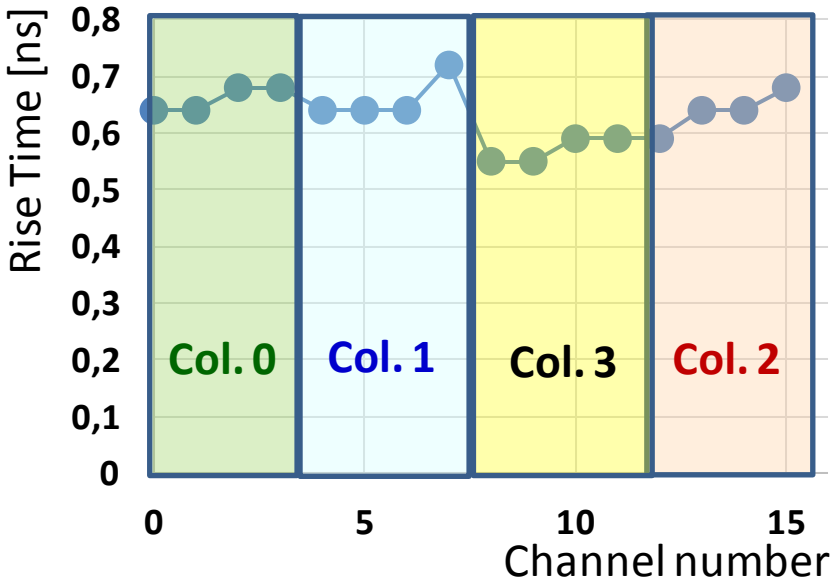


PA Probe output not designed to be uniform:

- |Max. Amplitude| decreases along one column
- Variation from column to column (possible attenuation from column to column could currently come from the use of different cable length for each column)

Rise (Fall) Time (RT) computed between 10% and 90% of |Max. - Ampl.|

Rise Time (RT) vs channel number
(13.8 fC input charge)



- Variation of RT value from column to column
- Slight variation within one column
- Probe output signal is probably slightly slower than PA signal processed by TDC, due to the Probe Follower

EICROC0 TZ Pre Amplifier Probe output signal amplitudes (6)

Output Probe PA Jitter Evaluation

On scope, data (Time ; Amplitude) recorded
event by event (pulse corresponding to each trigger)

Time distribution computed for a **Constant Fraction discriminator**
(***threshold at 20 % of the |Max. Ampl.|***)
With a linear extrapolation between samples

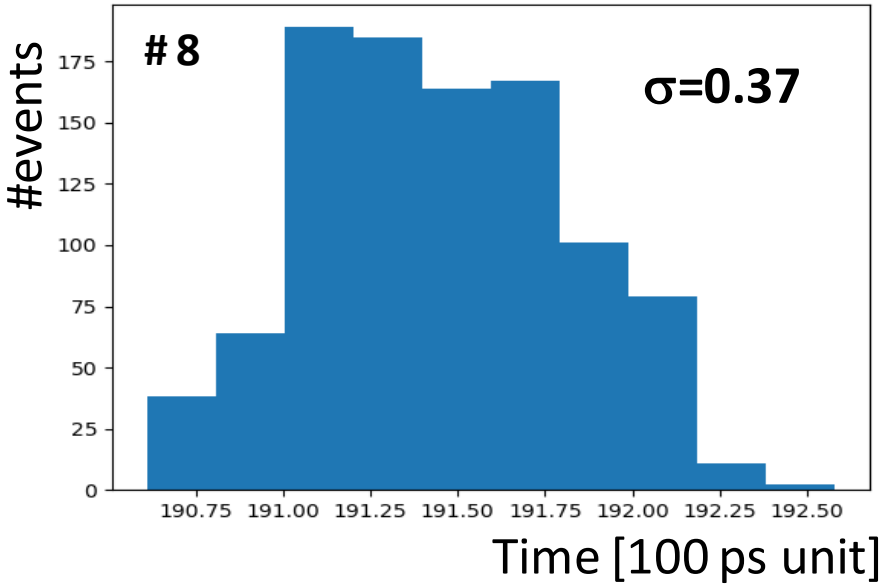
σ = 0.37 [100 ps unit] → **Jitter = 37 ps**

Jitter **quite good** **BUT** theoretical jitter would be:
0.9 ns (rise time) / **[**95,5 (signal) / 1.3 (noise)**]** = **12 ps**

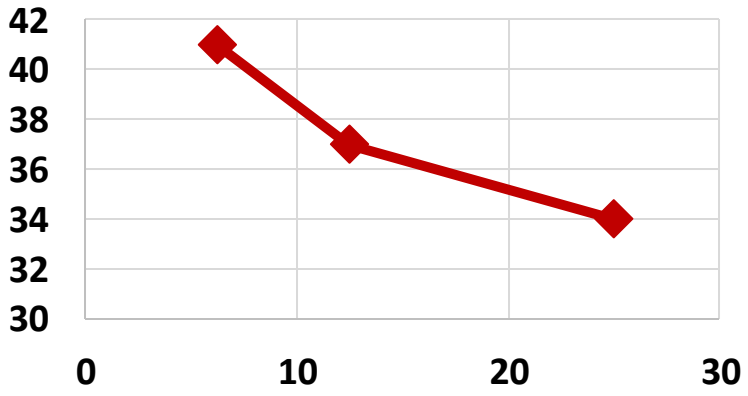
Injected Q [fC]	Jitter [ps]
25.00	34
12.50	37
6.25	41

Need to investigate floor jitter contribution
from command pulse injection

12.5 fC input charge



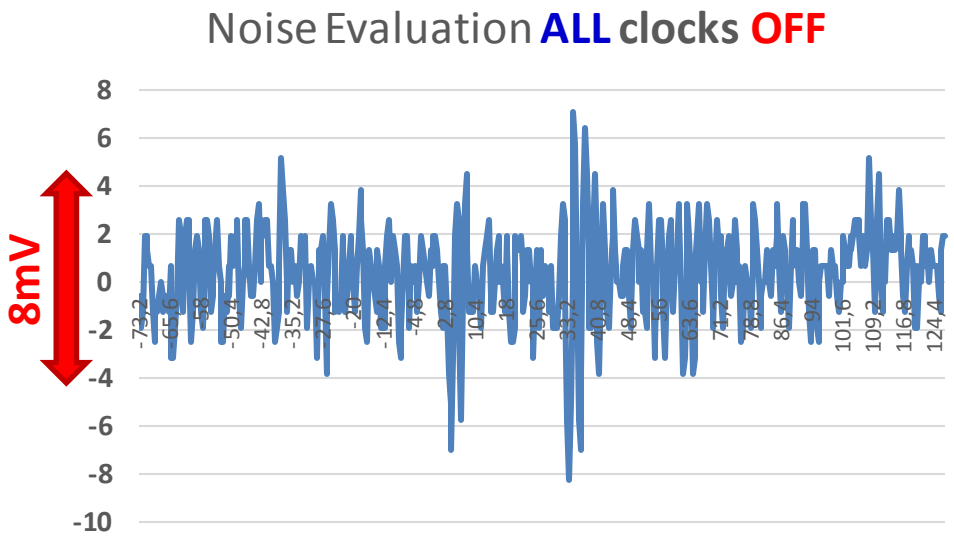
Probe PA Jitter [ps] vs injected charge [fC]

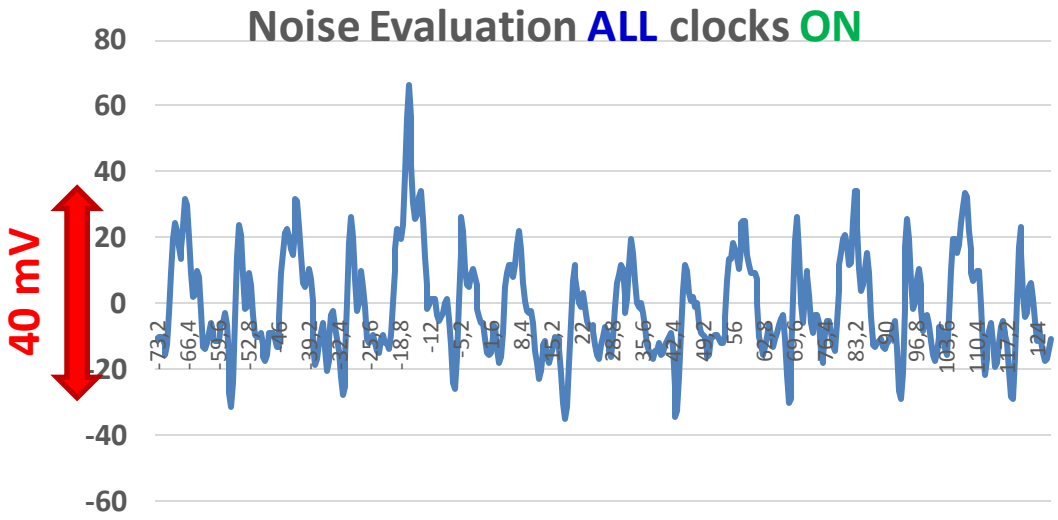


EICROC0 TZ Pre Amplifier Probe output signal amplitudes (7)

Preamplifier performance with clock switched ON/OFF

160 MHz clock (mandatory for TDC) [40MHz inherited from 160 MHz (/4) for ADC]

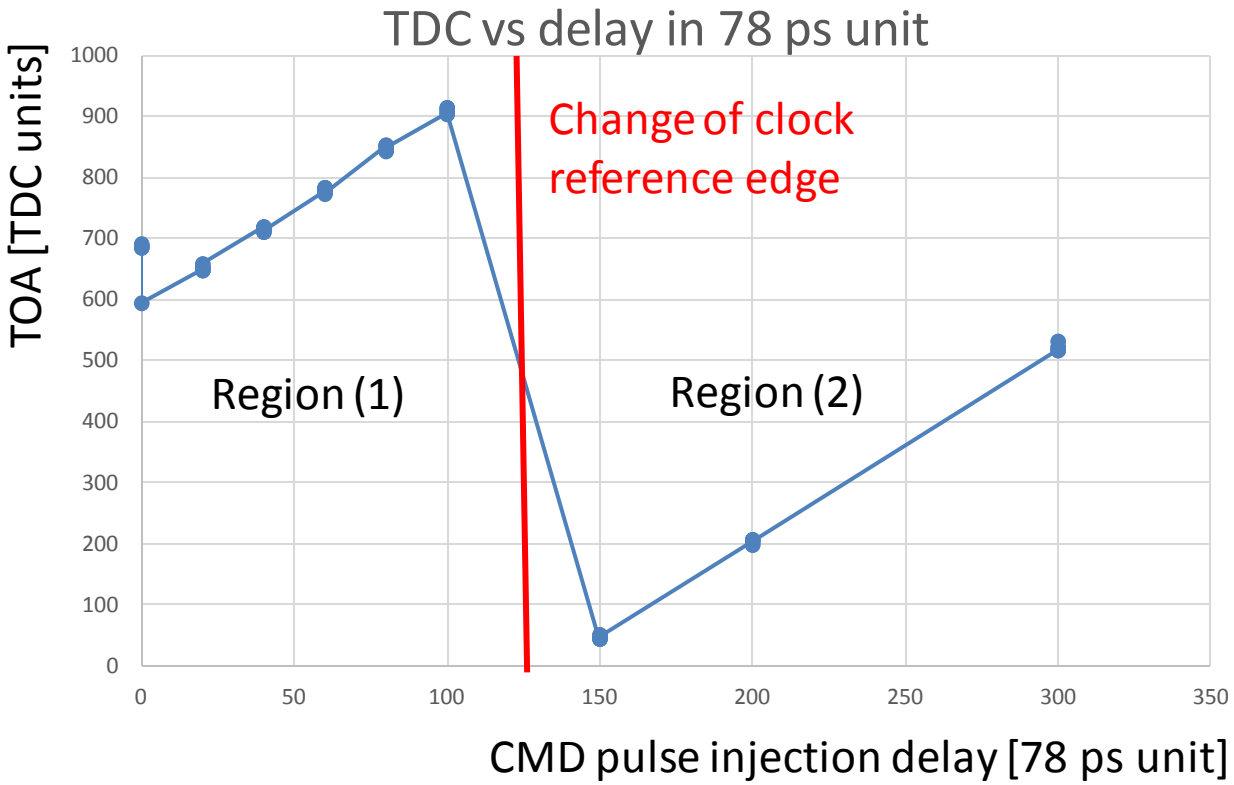




When **160 MHz** clock is **ON**: noise **larger by a factor 5-6**
due to a clear coupling to the PA input

Sill under investigation (ground PA, PCB…) but up to now limitation for Time measurement with TDC

EICROC0 TDC Characterization (1)

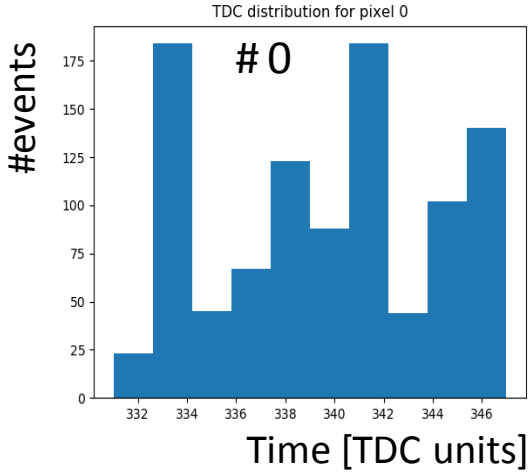


* Nominal TDC quantification step: 25 ps

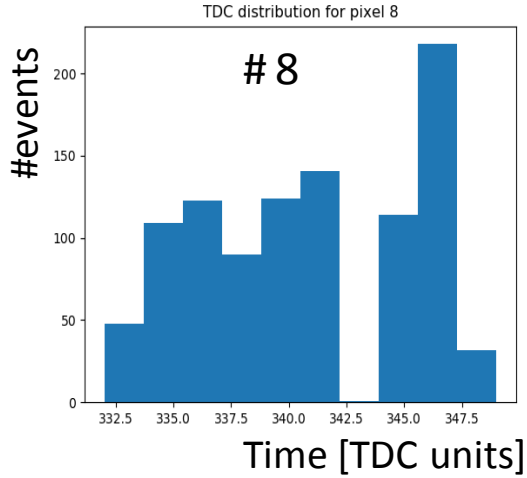
Slope region 1 (2) : **24,6 (24,2) ps**
=> in fair agreement with nominal TDC quantification step

Can be adjusted to nominal through slow control parameters

EICROC0 TDC Characterization (2)



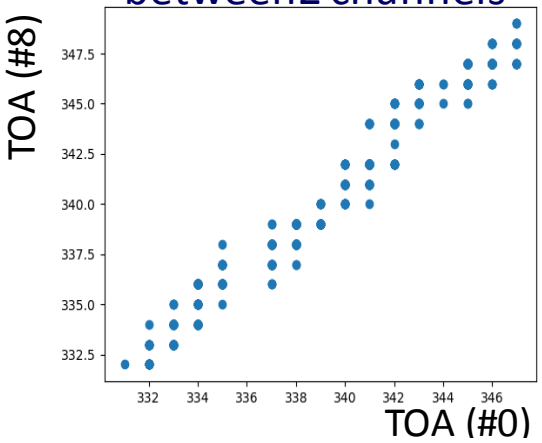
RMS = 4.4 → **110 ps**

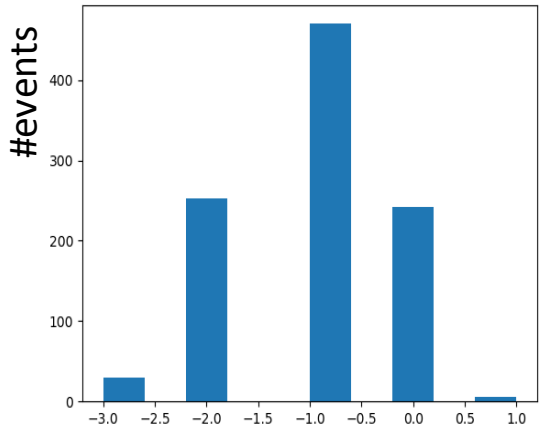


RMS = 4.8 → 120 ps

Individual TOA jitter not so good

Time correlation between2 channels





RMS = 0,79

Clock noise strongly correlated between channels
→ computation of time difference

ΔT = 0. 79 TDC units
→ 19.7 ps

Assuming an identical resolution for each channel:

The achievable TDC time resolution is:

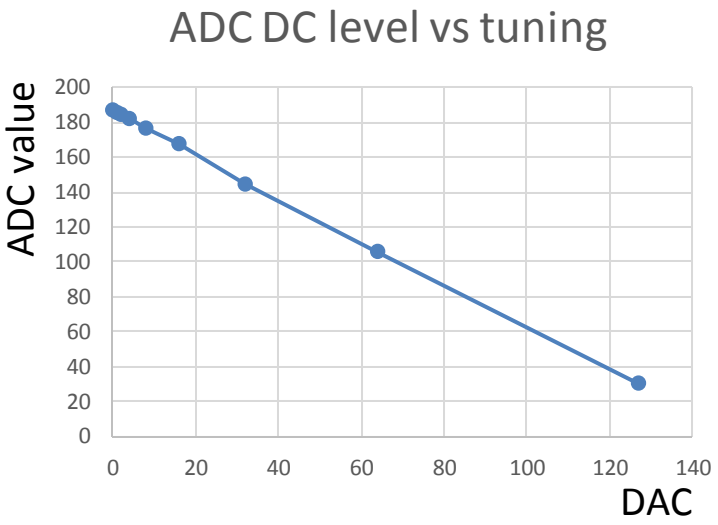
19.7/sqrt(2) = **14 ps**

for the entire chain (PA+discri+TDC)
if PA clock coupling issue is solved

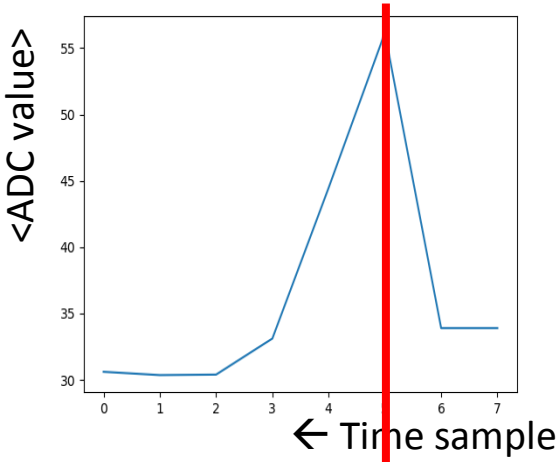
[DACB_pulser used: 250 mV]

EICROC0 ADC (8 bits) Characterization (1)

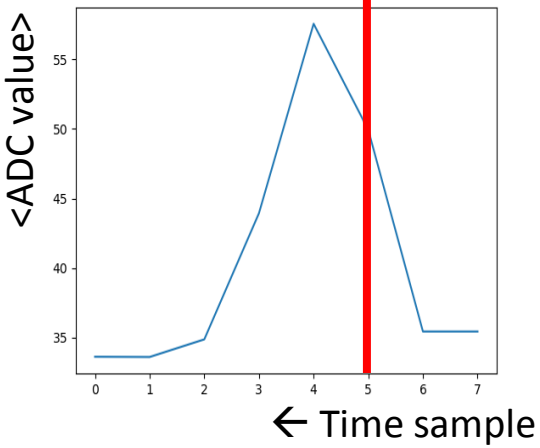
PA is followed by an **integrator** digitized with a 8 bits 40 MHz ADC providing 8 time samples (every 25 ns)



DC level (pedestal) can be tune per channel
(Vref_cor parameter, 7 bits)

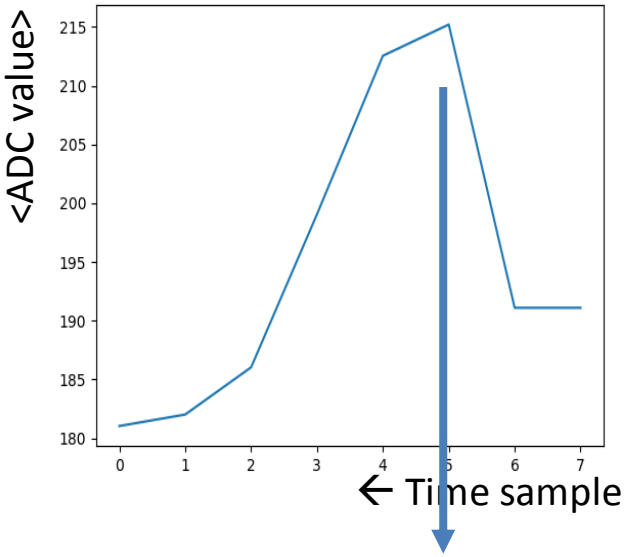


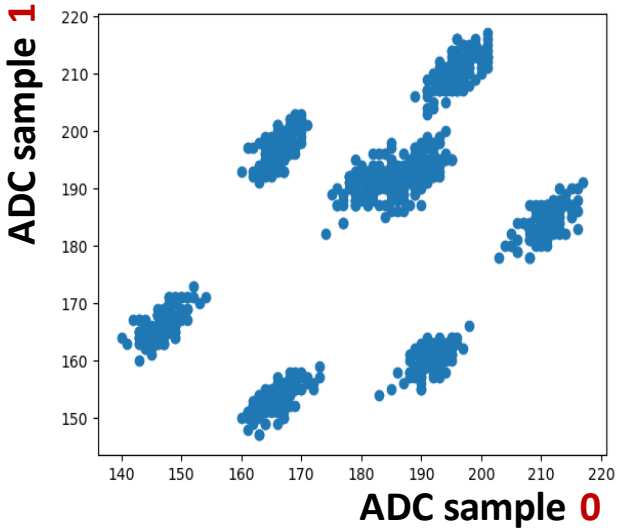
PA + integrator can be seen,
shifting with CMD pulse delay

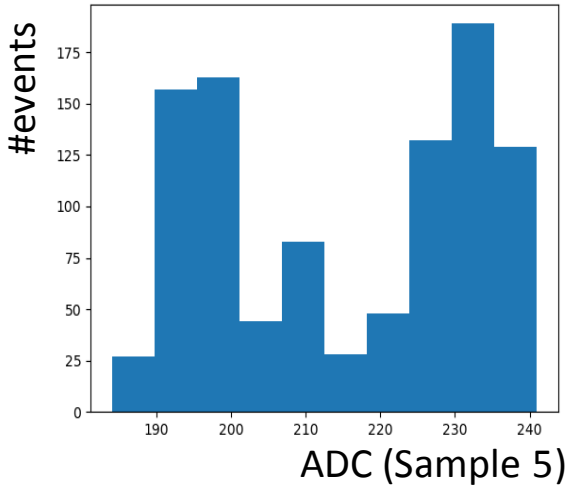


BUT signal shape not as expected
distorted by a large coherent
noise between all channels

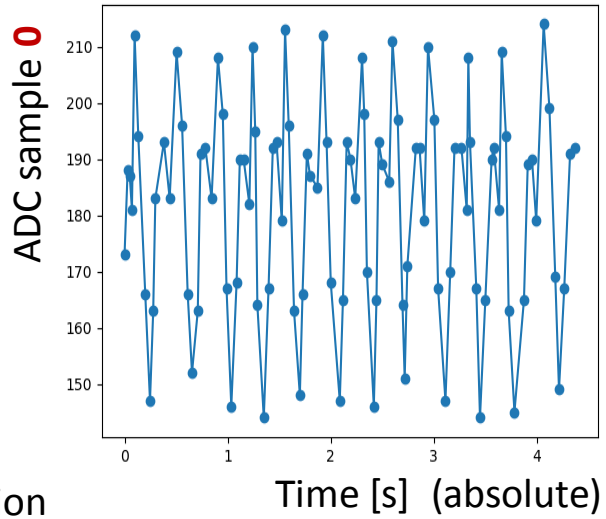
EICROC0 ADC (8 bits) Characterization (2)







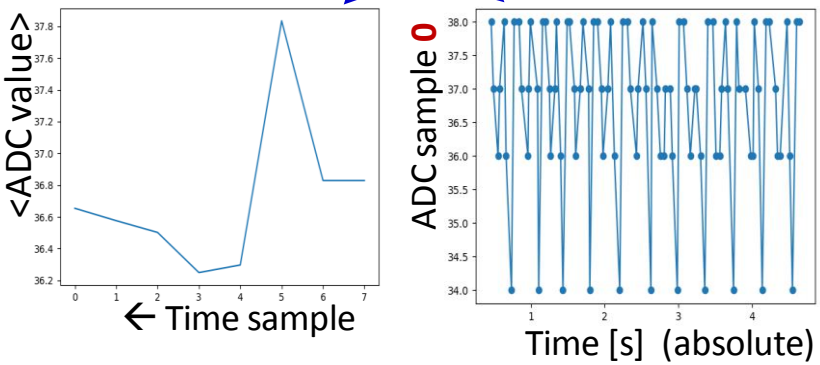
Large noise and non gaussian distribution



8-fold noise structure observed:

- Correlated between all channels
- Low frequency noise

Switching off the integrator (no gain)



- Very low amplitude PA signal
- Lower ADC noise dispersion but still 8-fold structure low Frequency (a few Hz)

More investigation needed ….

EICROC0 Progress Report: Summary

- EICROC0 test bench operational at IJCLab
- So far only 1 board w/ EICROC0 « alone » under test
- **Individually** Pre Amplifier, TDC and ADC performances are in agreement with design
- 4 simultaneous PA Probe outputs can be efficiently exploited for detector characterization
- Observed integration/noise/coupling issues require further investigation:
  - 160 MHz clock coupling to PA
  - low frequency noise ADC (integrator?)

EICROC Project: Perspectives

- Keep on investigating board w/ « ASIC alone » (noise & coupling, more systematics measurements, cross-talk) [IJCLab –OMEGA]
- Testing board #4 (w/ EICROC0 and AC-LGAD sensor) => evaluation of charge sharing [IJCLab]
- Start EICROC0 characterization at BNL (basic documentation sent), support from IJCLab and OMEGA
- Development of software scripts to automate acquisition and analysis software tools [BNL-IJCLab]
- Production of addtional (or new) EICROC0 PCB, depending on results of coupling/noise investigations (more EICROC0 chips will be available within 3 to 4 months)
- Start design of next ASIC iteration (fixing observed issues, …, lower power consumption ADC? , EIC clocks?)

EICROC Project Status

IN2P3 officially supports OMEGA Microelectronics Technical Contribution in EIC ASIC designs

Funding

- Université Paris-Saclay (P2IO): 75 k€ [2021 – 2022]
- DOE/eRD109: 75 k€ (contract not signed yet due to delay on the French CNRS side
  => will be spent for EICROC next ASIC iteration: EICROC0_v1
  (Submission foreseen 1st quarter of 2024)

- **DOE/eRD109 « FY2024 » proposal:** plan to request 90 k€ budget for EICROC1 submission

Human Resources reinforcement

- **OMEGA:**
  - + Adrien Verplancke (engineer) involved in EIC ASIC design and characterization [May ‘23 on]
  - + 1 PhD student starting Fall ’23
- **IJCLab:**
  - + 1 intern student (2nd year Egineering schoolBoudjerouna [May - July 2023]
  - Université Paris-Saclay (P2I): 60 k€ grant obtained (June ‘23) to hire a postdoc for **1 year**

- Sofiane Boudjerouna (intern)
- Beng Yun Ky
- Dominique Marchand
- Carlos Munoz Camacho
- Laurent Serin
- Ana-Sofia Torrento
- Pu-Kaï Wang (PhD, last year)

- Florent Bouyjou
- Eric Delagnes

- Pierrick Dinaucourt
- Nathalie Seguin-Moreau
- Christophe de la Taille
- Maxime Morenas
- Adrien Verplancke

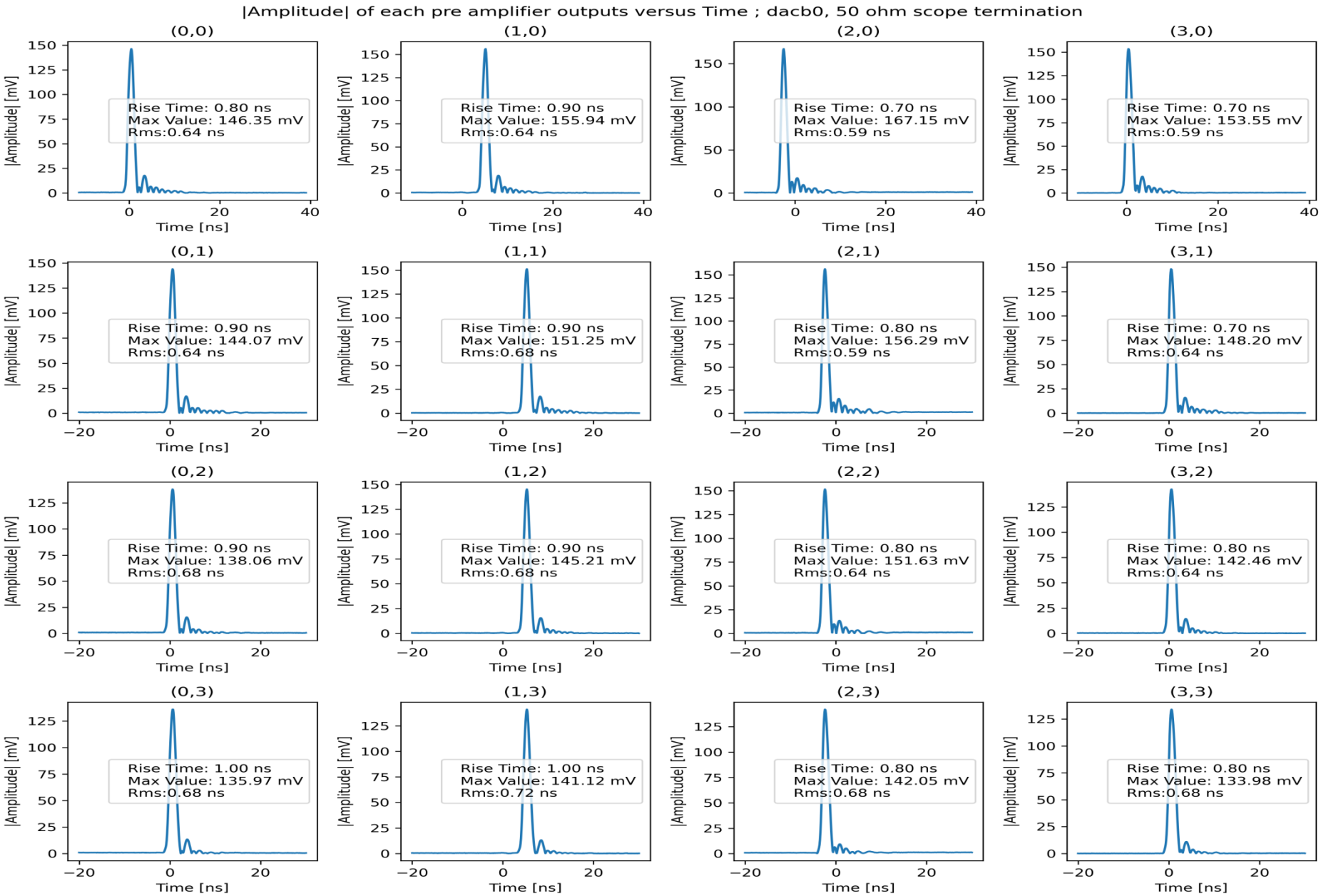
Alessandro Tricoli's team

The EICROC0 Project: a team effort

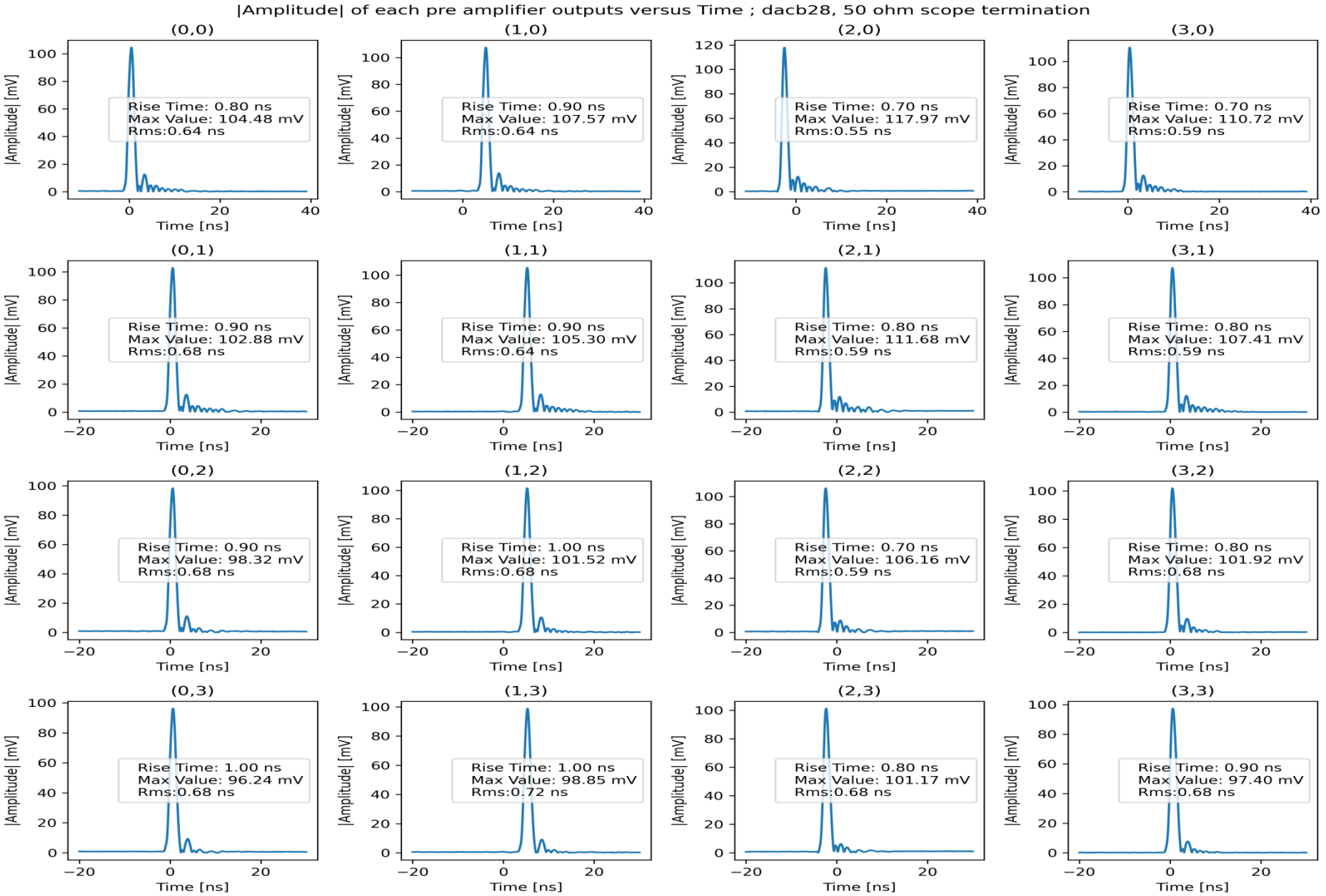
Thank you

Back-Up

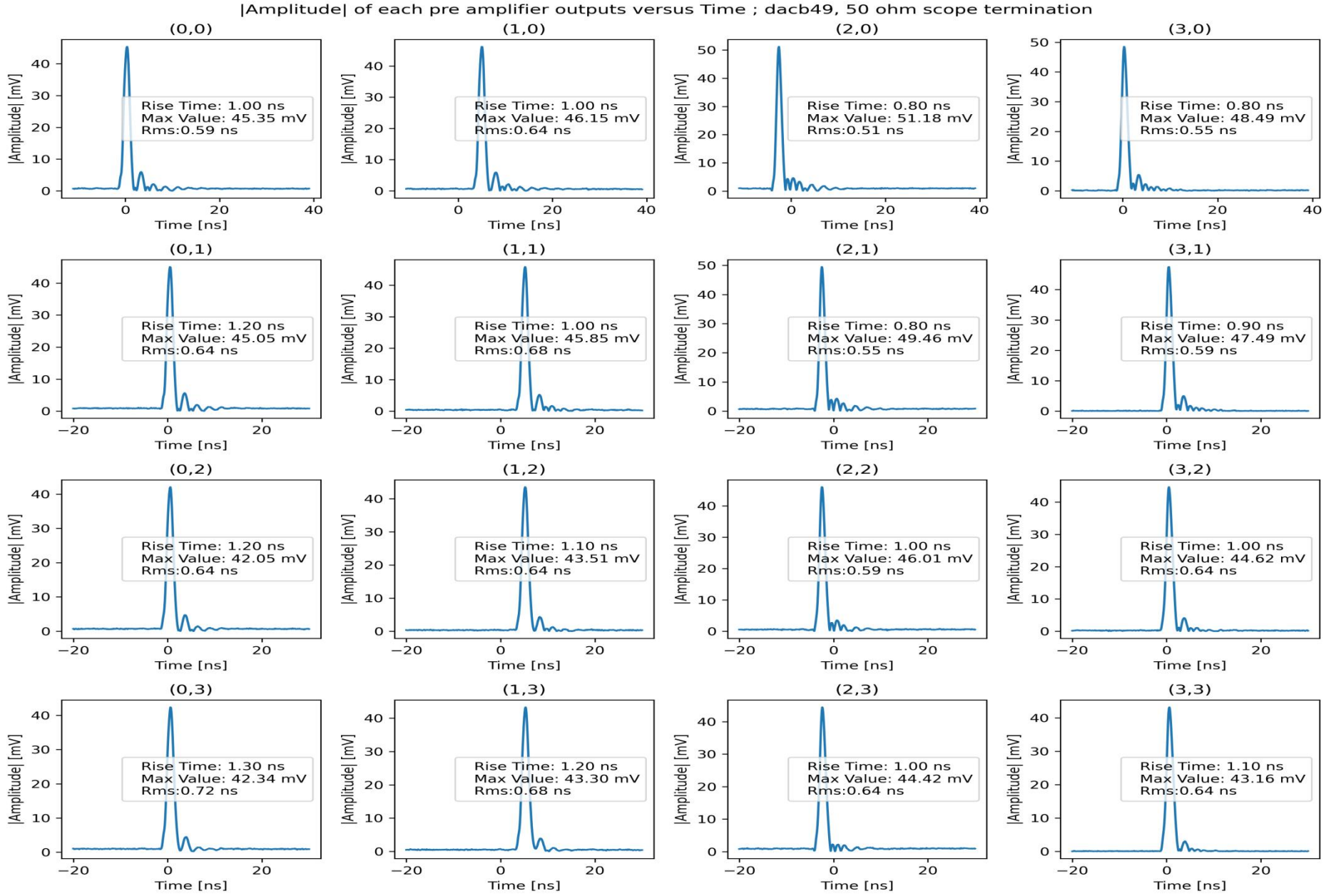
EICROC0 characterization: Probe PA Amplitude 25 fC input charge



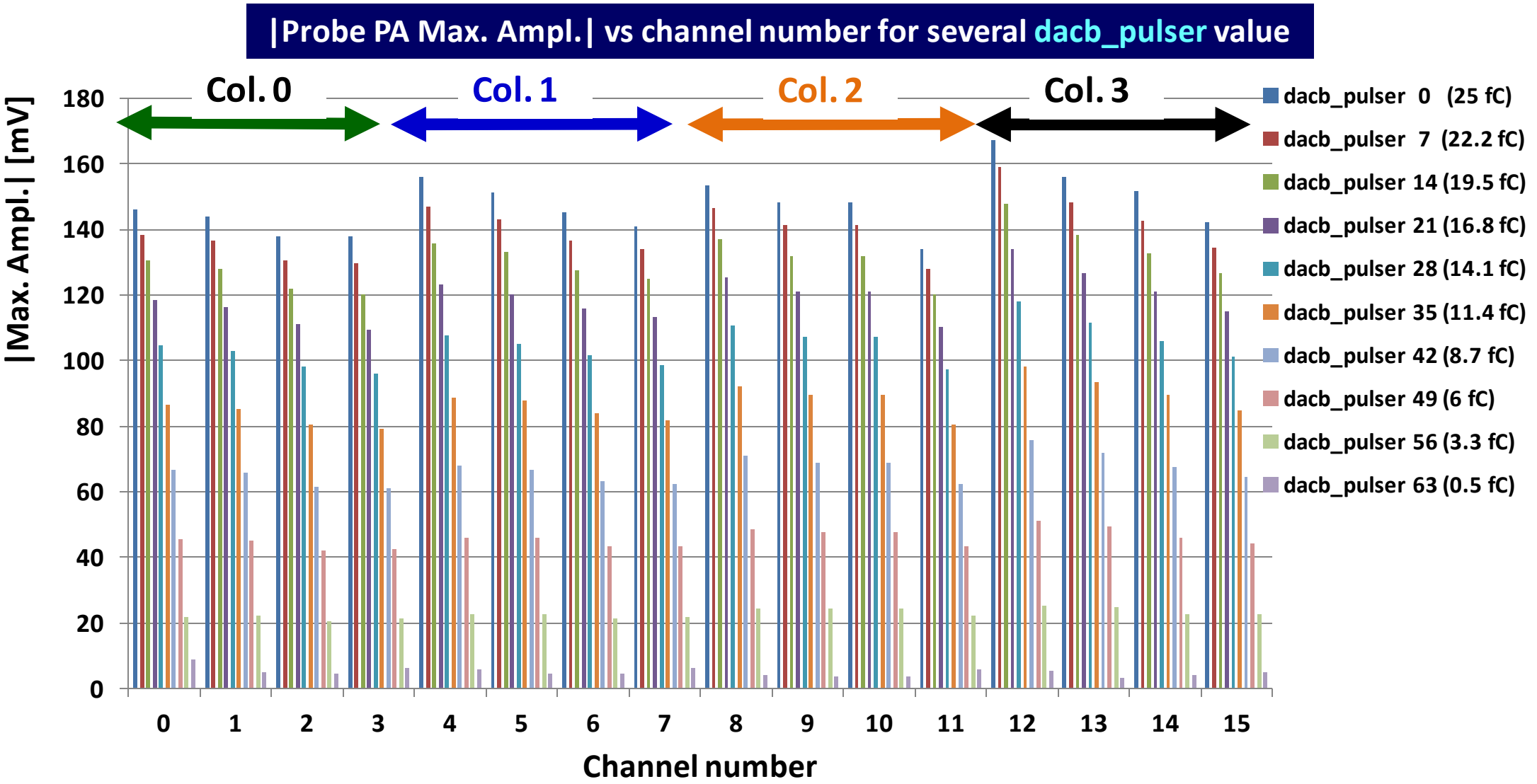
EICROC0 characterization: Probe PA Amplitude 14.1 fC input charge



EICROC0 characterization: Probe PA Amplitude 6 fC input charge

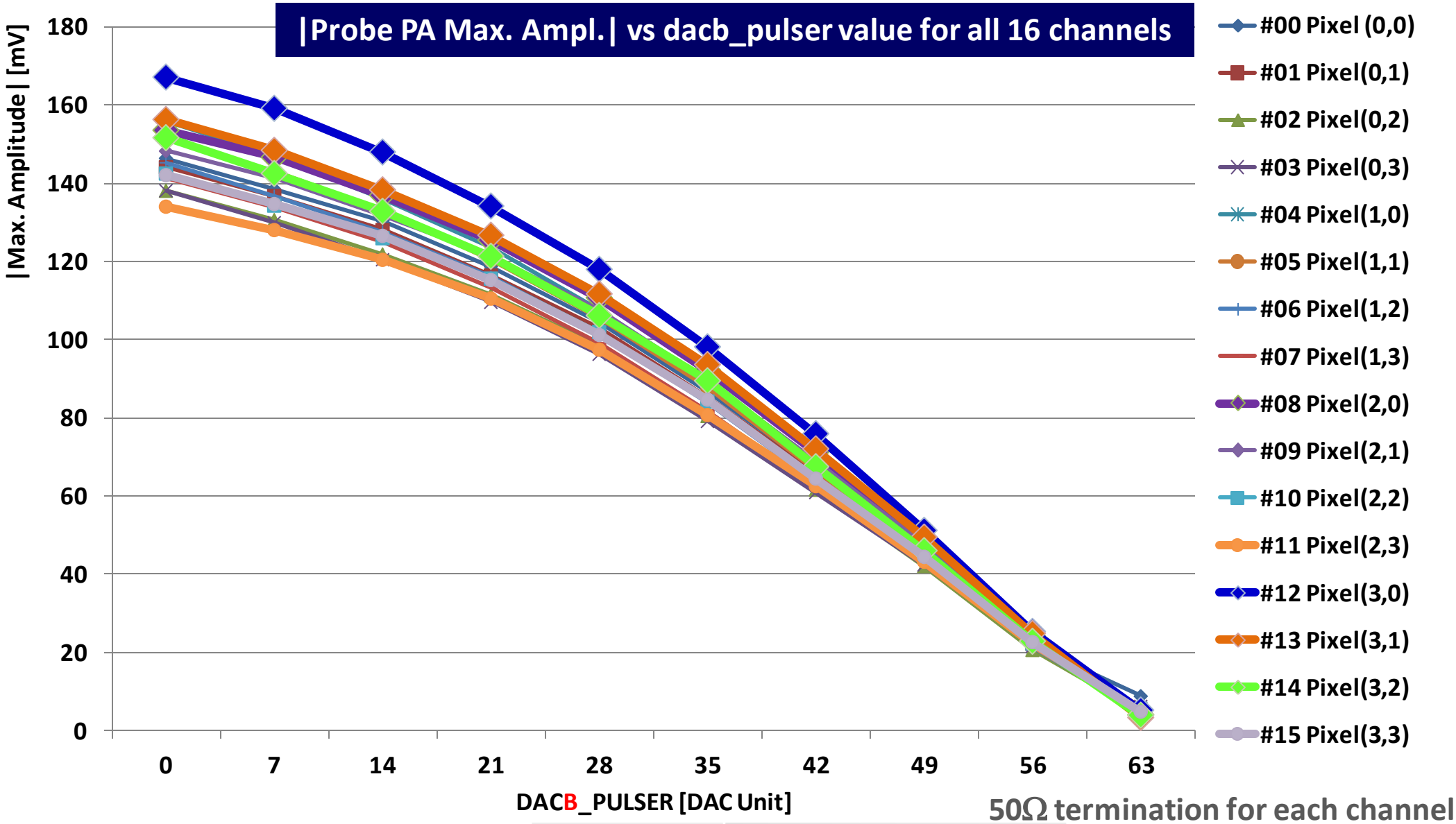


EICROC0 TZ Pre Amplifier Probe output signal amplitudes (4)



Oscilloscope: 50Ω termination for each Probe PA channel

EICROC0 TZ Pre Amplifier Probe output signal amplitudes (5)

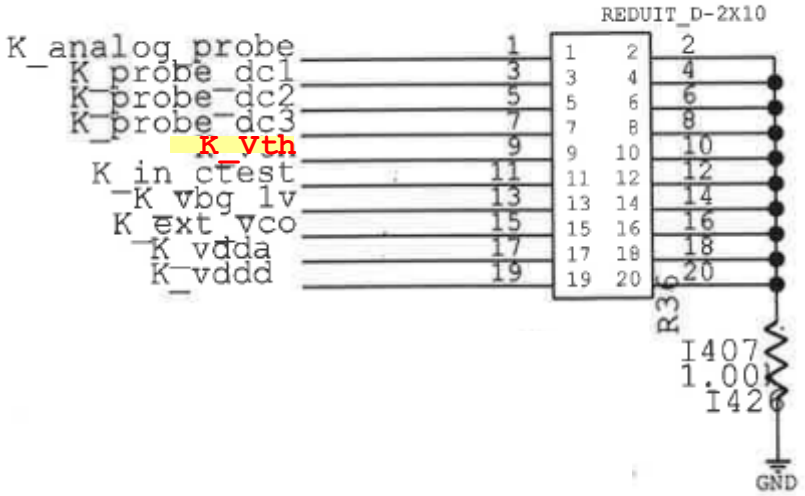


50Ω termination for each channel

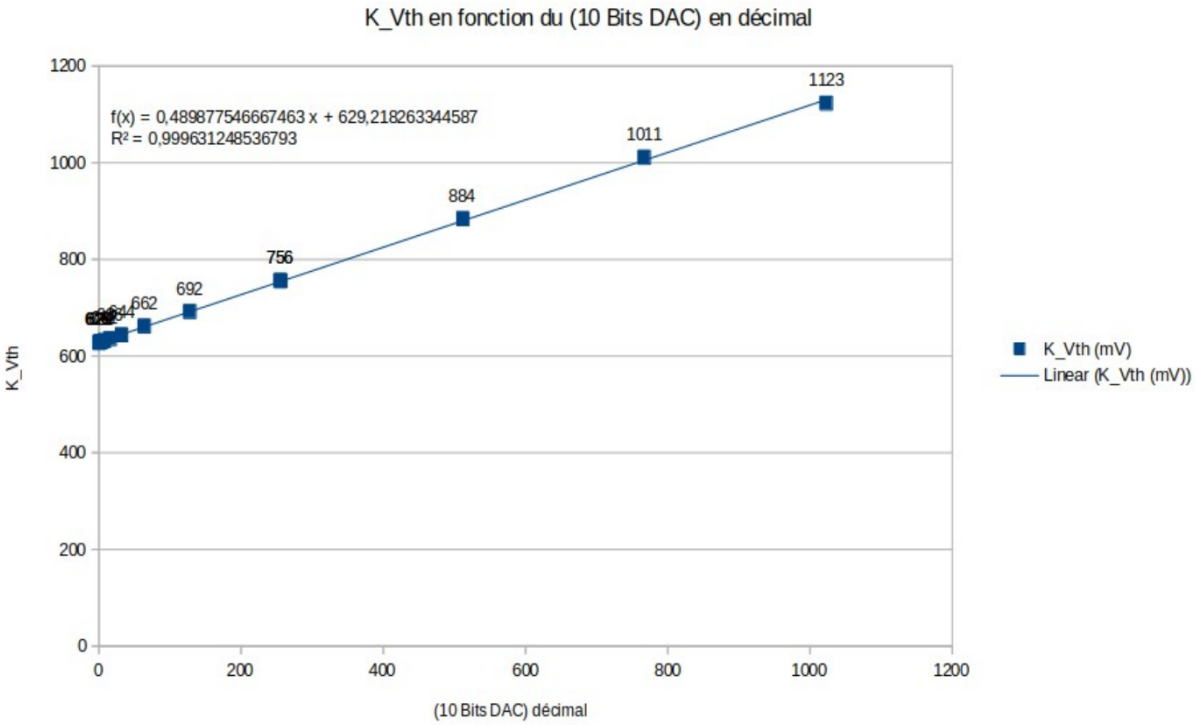
EICROC0 Discriminator Threshold Scan

In configuration file: Global Parameter **10bitDAC** [**0** (Min. value) -> **1023** (Max. value)]
Registers **0x20A** [7:0] & **0x20B** [xxxxxx]-[**9:8**] *Most significant bits*

J5 connector (DC level)



Measurements of **K_Vth** (DC level) versus 10bitDAC value



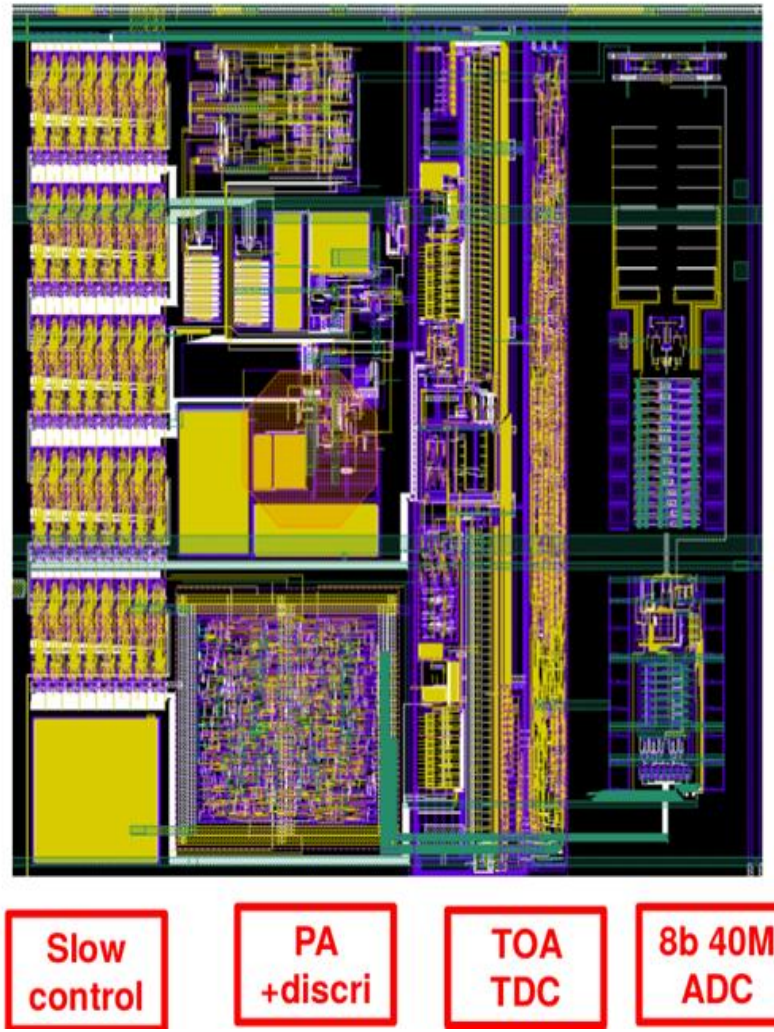
EICROC0: 1 pad (500 x 500 µm²) overview

- High speed TZ PA and discriminator (from ALTIROC)
- I²C slow control (from CMS HGCROC)
- 8 bits 40 MHz ADC (adapted from HGCROC 10 bits ADC, M. Idzik *et al.,* AGH Krakow)
- Digital readout FIFO (depth 8, 200 ns)
- 10 bits **TDC** (TOA) designed by **CEA Irfu/DEDIP**:

HGCROC TDC (1 mm x 120 µm):
- spatially adapted to fit in a pixel of 0.5 x 0.5 mm²
- optimization in terms of dynamic range and resolution (10 ps rms) as well as power consumption
- common block for calibration of all TDC channels

✸ 5 slow control bytes/pixel:
- 6 bits local threshold
- 6 bits ADC pedestal
- 16 TDC calibration bits
- Various on/off and probes

EICROC0 layout (1 pad = 1 channel)



EICROC0 boards repartition status (June 1st, 2023)

Board	Location	EICROC0	AC-LGAD	Modifications/comment	Status
B1	Nantes?	✓	X	None For HGTD 40 MHz PLL testing (OMEGA)	Presently activated
B2	IJCLab	✓	X	**R5** & **R17** (cmd_pulser) **replaced (90Ω -> 150Ω)** **+ Jumper alim + Jumper (spare 1 - spare 2)**	**Under test**
B3	**OMEGA**	✓	X	None For HGTD 40 MHz PLL testing	Retrieved from irradiation
B4	**OMEGA** *	✓	✓	**R5** & **R17** (cmd_pulser) **replaced (90Ω -> 150Ω)** **R57**&**R58** values inversed: **replaced** **R54**&**R52** values inversed: **replaced** Reg. **M13** & **M14** *cabled upside down*: **replaced**	**Under investigation**
B#	**OMEGA** *	X	X	None	Part. cabled
B#	**OMEGA** *	X	X	None	Part. cabled
B#	**BNL**	✓		Reg. **M13, M14** OK (photo)	
B#	**BNL**	X		Reg. **M13, M14** OK (photo)	
B#	**BNL**	X		Reg. **M13, M14** OK (photo)	
B10	**Irfu/DEDIP**	X	X	None	Part. cabled

* Board transferred from BNL to CERN (Christophe) in Feb 2023.

EICROC0 chips left: 7 at BNL, 6 at CEA/Irfu [20 currently considered lost …]

Xilinx ZC706 boards: 1 at IJCLab, 1 presently isolated in Nantes (OMEGA), 1 at Irfu, 1 (or 2) at BNL?