eRD109 R&D for waveform digitizing FEB for ePIC forward ECAL

It is R&D for a high-resolution waveform digitizing readout (similar to STAR FCS),
although also working with ORNL group to evaluate whether HGCROC can meet performance requirements instead.

In the meanwhile it is *also* development of mechanical, power, SiPM bias, cooling, and interfaces of an FEB
which fits the forward ECAL application – whether the readout be HGCROC or a waveform digitizer.

Waveform digitizer *may* be COTS ADC (assumed for now) + FPGA, or it may be an ASIC (+ FPGA if need be).

G. Visser, Indiana University
5/18/2023 ePIC DAQ/Electronics meeting

forward ECAL requirements and characteristics

- about 19,000 towers (not yet precisely defined)
- each 4× 6x6 mm^2 SiPM's, 15 μm pixel pitch (640,000 pixels)
- light yield roughly 1000 pixels/GeV
- fundamental grouping is 4×4 block of towers (10×10 cm^2) – FEB must fit over that
- temperature compensation of SiPM bias – instead of control of SiPM temperature
- ~10^{11} n/cm^2/year (near beamline)
- waveform digitizing @ (likely) 98.5 MHz / 3 = 32.83 MHz
- pulses shaped to ~8 samples width
- streaming readout (of course)

STATUS/WORK UPDATE

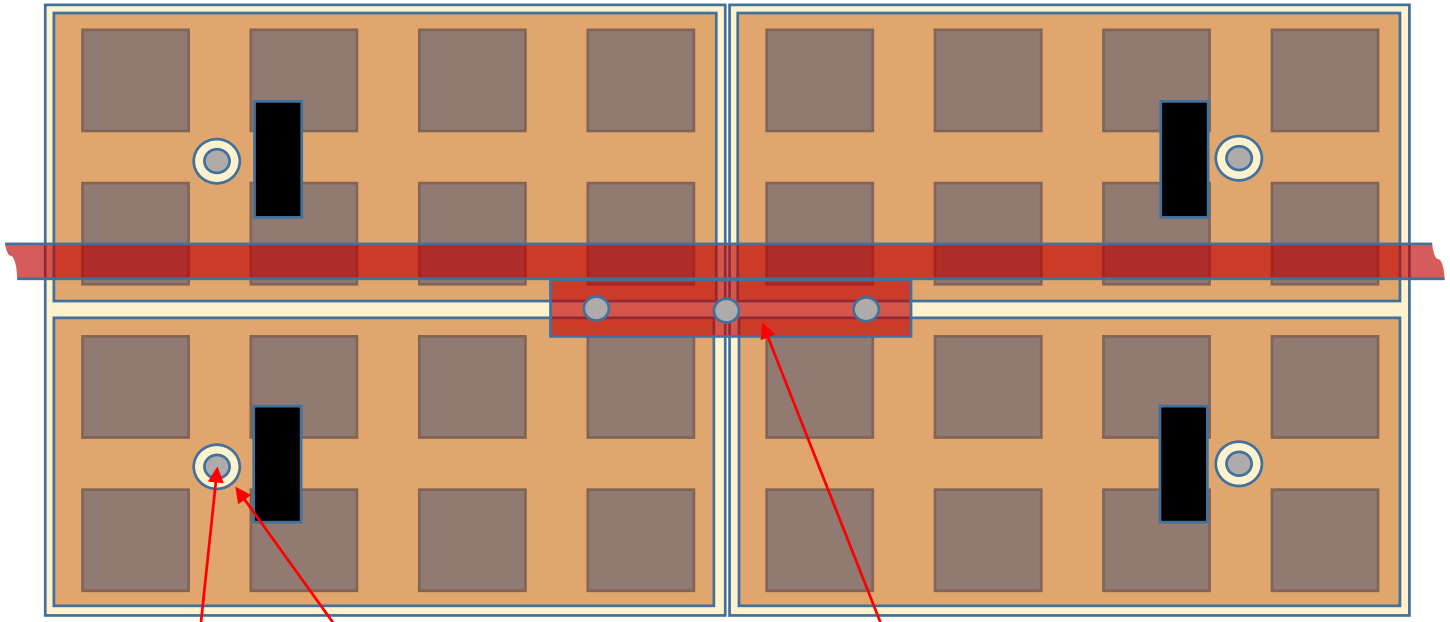
- eRD109 funds finally in place, real work on the FEE development commencing
  - effective start date 5/1/23

- work now in progress:
  - ADC chip selection and procurement (for 1st R&D prototype), and (if feasible) eval board procurement
    - most likely ADC is TI # ADC3422 (compatible ADC3442 for 14-bit, start with that)
    - 44% lower cost than nearest reasonable competitor, performance about same (on paper anyway)
    - 4 channel chips (vs. 16 channel competitor); there are pros and cons both ways, will need to really get into layout details before I know my regrets – the PCB layout will be very challenging either way
  - water cooling prototyping (actually was done in January)
    - looks fine w/ standard 3/16" copper tubing @ 0.25 liters/min
  - design and prototyping for DC/DC converter possibility – for cable size/mass and power reduction
    - 19,000 ADC's: @ 1.8 V → 528 A vs. @ 13 V → 91 A (after accounting for 80% efficiency)
  - (soon): FPGA selection and procurement, FEB-RDO interface planning
    - still thinking about Microsemi PolarFire rad-tolerant FPGA's
      - higher cost, less capable on LVDS serial ADC interface (but good enough??? thinking about it…)
  - SiPM boards mechanical and connectors – plan to make quick cheap dummy PCB (OshPark) soon

FEB & SiPM carrier mechanical cartoons
(dimensioned sketches will be made later)

2-block (32 tower) FEB

FEB not shown (in this view only)
(but see next page)



standoff clearance hole through SiPM carrier PCB

6 or 7 4-40 pan head screws
to attach FEB on 4 standoffs and
2 or 3 thermal tab nuts

cooling water tubing & small "tab" to PCB
0.19" OD, 0.13" ID
copper "refrigeration tubing"
no fittings inside detector

water tubing connection to FEB is also an electrical ground for FEB (important for noise/EMI and safety)

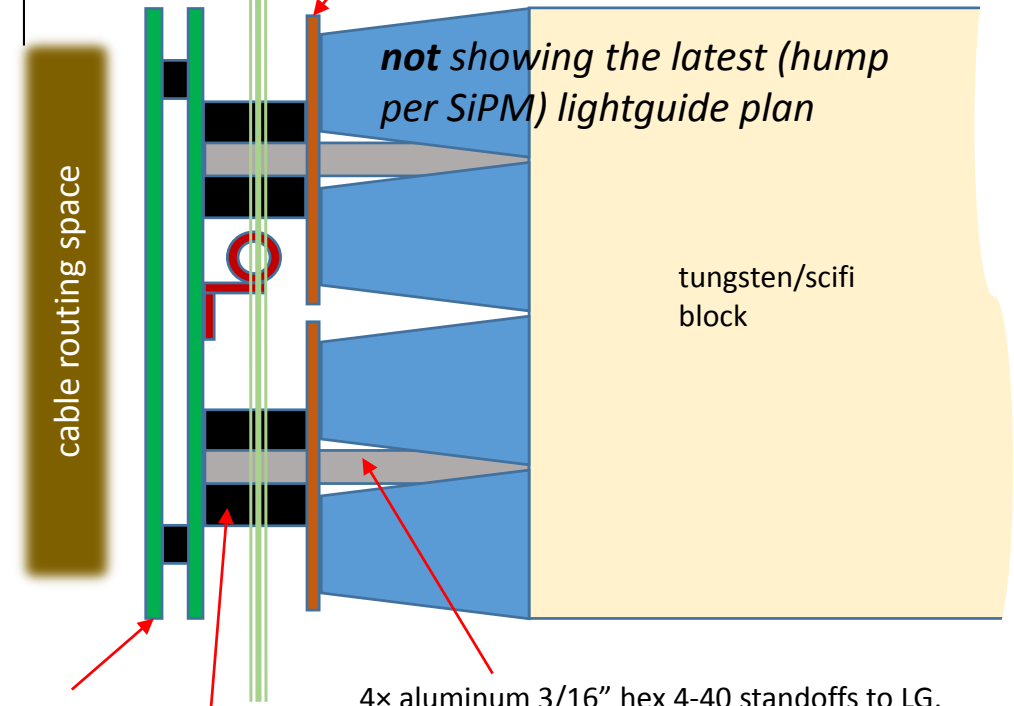
all cables and water tubing route
basically only horizontally on detector

vertical flow air cooling **alternative** (to be studied in R&D) – "plenum" between FEB and SiPM boards

1.4 cm (if water)
3 cm (if air)

5 cm

SiPM carrier PCB, qty. 4,
8 towers (32 SiPM's) each
glued to lightguide block

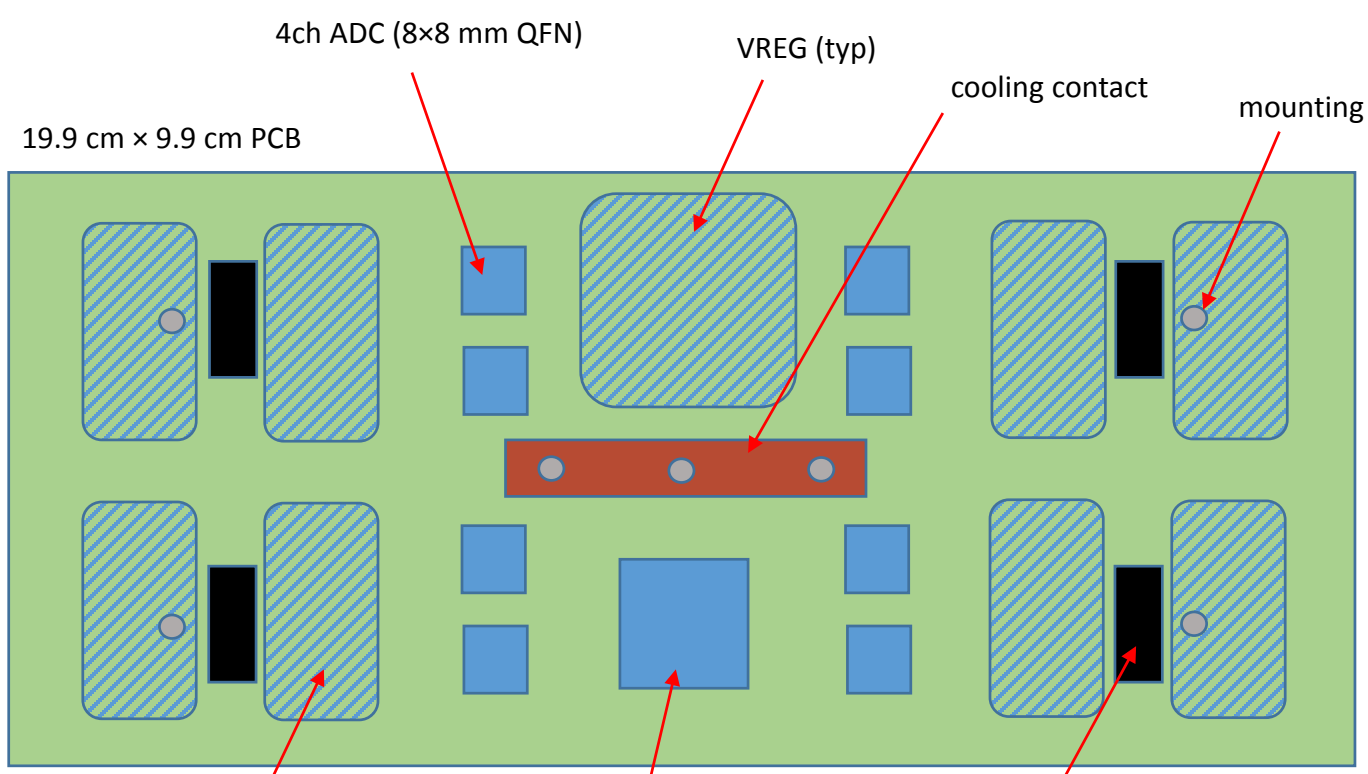


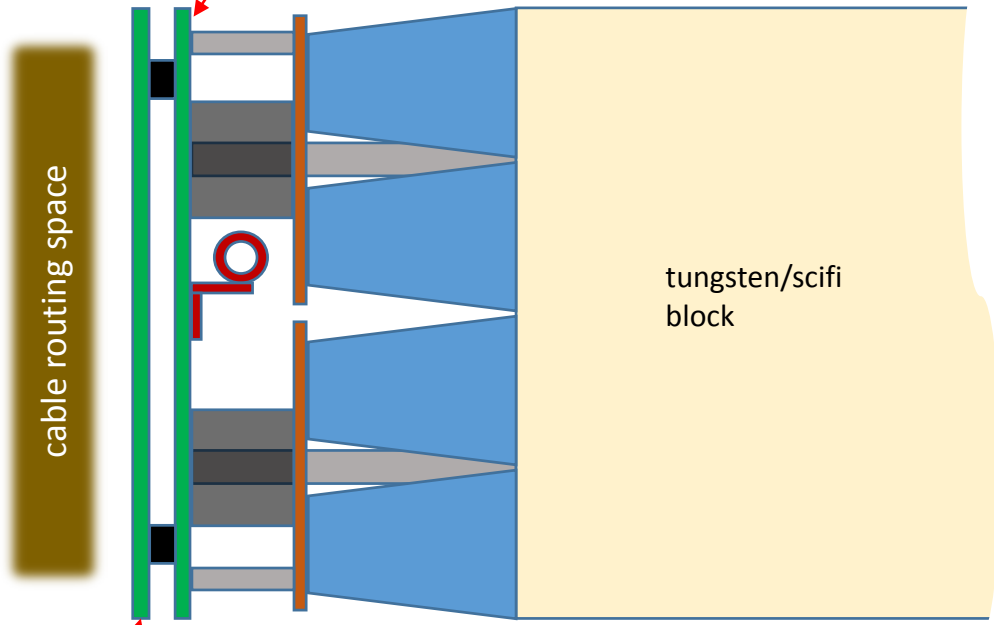
FEB PCB stack
2 – 3 PCB's

4× aluminum 3/16" hex 4-40 standoffs to LG,
support FEB **independent of SiPM boards**

floating connectors, 1 per SiPM carrier
JAE AX01 series (30 pos) or similar

rear view of inner FEB PCB



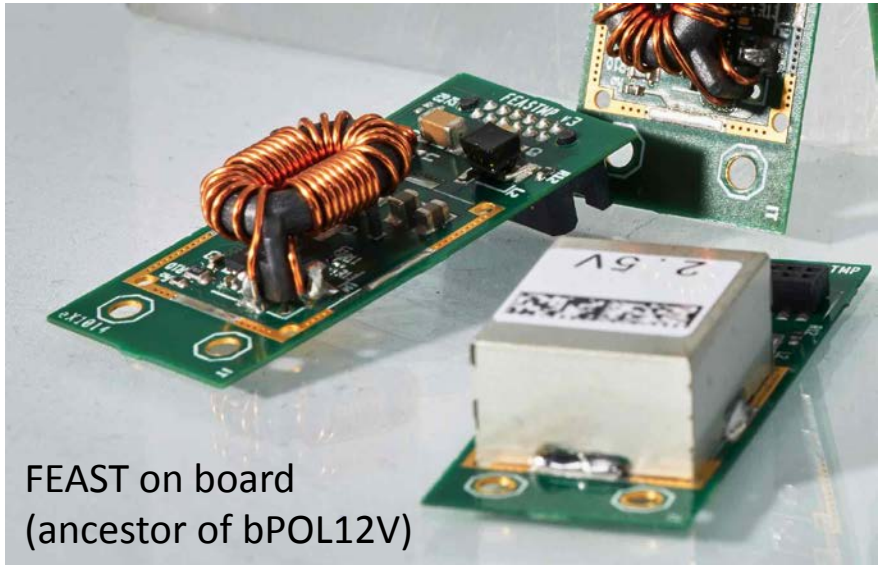


SOME MORE DETAIL ON POWER

This will of course be a universal concern in ePIC design. *Perhaps* with universal solution(s).

It will be *very* difficult to support modern low-voltage components such as FPGA & ADC w/o some DC/DC converters.
The typical requirement will be O(10 V) in, 0.9 to 2.5 V out, a few Watts power level.

In the case of forward ECAL FEB specifically, I'll need 1.8 V @ 0.9 A for ADC's.



FEAST on board
(ancestor of bPOL12V)

Priority list of constraints/requirements on the DC/DC:
- Low noise (at least for FEB application if not for RDO)
- Magnetic field immune
- Small size, low mass
- Reasonable efficiency (70% enough probably)
- Radiation tolerance (COTS ok?)

Solutions:
- Certainly an air-core inductor buck converter
  - High ratio and low noise switched capacitor converters unlikely to be practical
- Frequency of several MHz is a must
  - Tradeoff of inductor size vs. noise and efficiency
- Monolithic, i.e., integrated controller and switches, is needed for small size and low noise
- "Synchronous" (i.e. FET not diode for low side switch) for reasonable efficiency

Chips (for 1.8 V 0.9 A):
- CERN's bPOL12V
  - Very rad hard, 10^{15} n/cm^2
  - Noise and efficiency *may* not be state of the art
- LT # LTC3601 (or LTC3600)
  - Well matched to this load; low noise, ~82% eff.
  - Radiation effects?

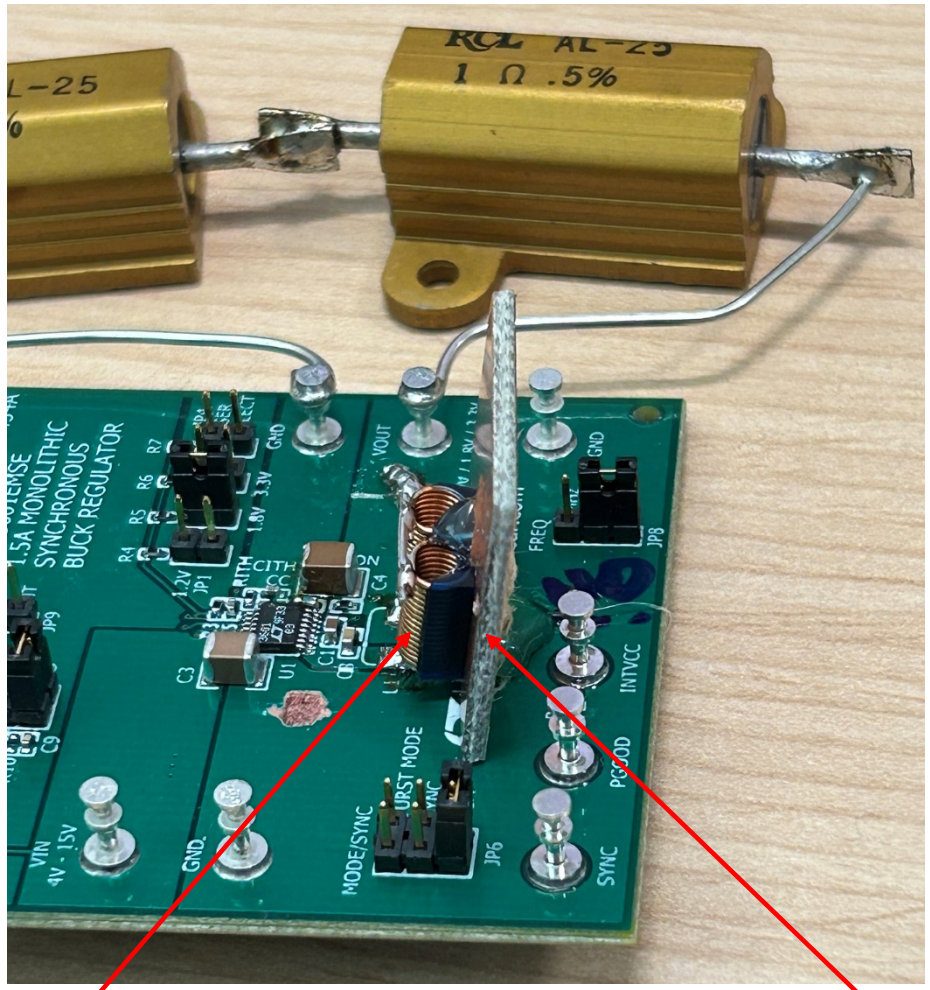
Both (& others?) will be investigated…

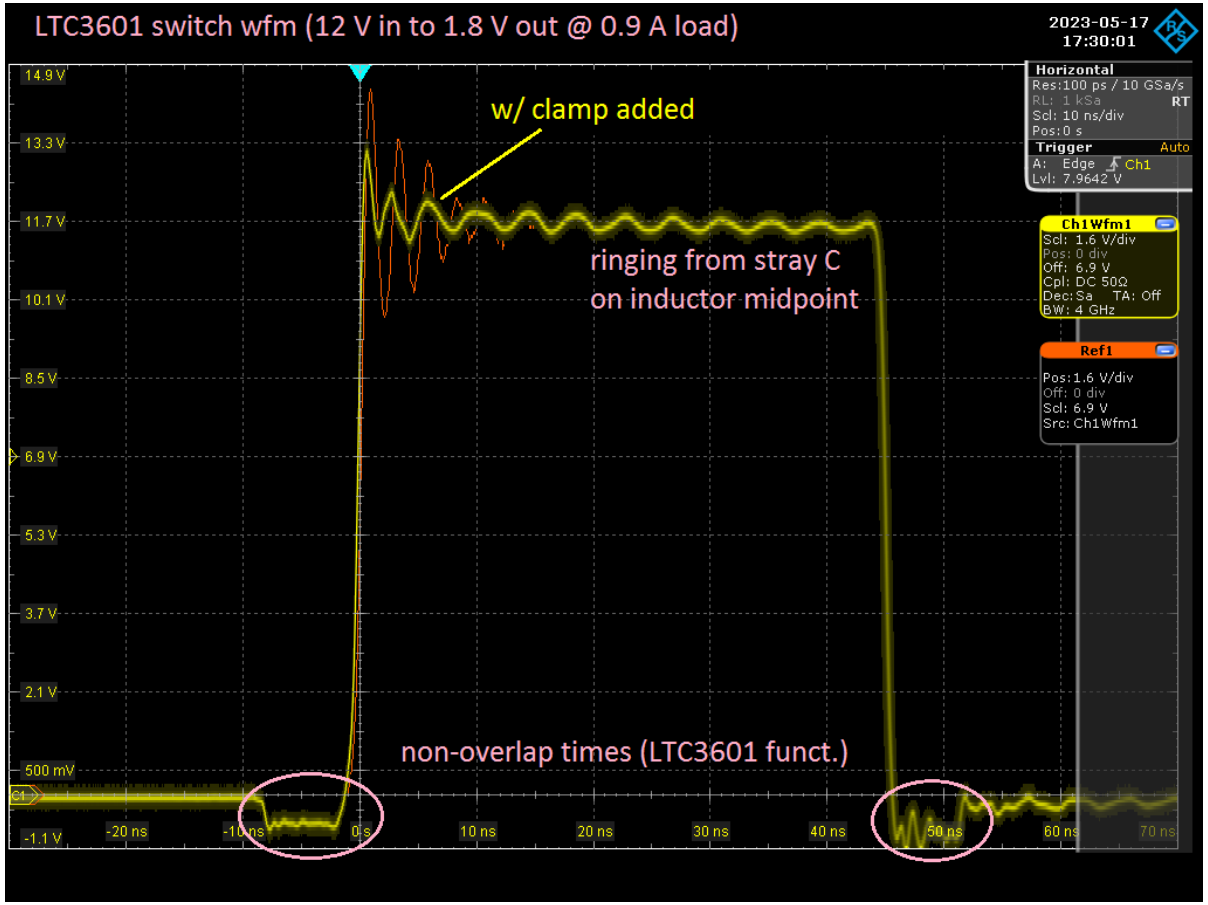
starting with LTC3601 on modified eval board

~3.4 MHz operating frequency

Unfortunately… this eval board is now fried!
(sloppy probing short, my bad)

I will make specific low noise board @ OSHpark, that was needed next anyway.
Also have requested bPOL12V eval board (2×).



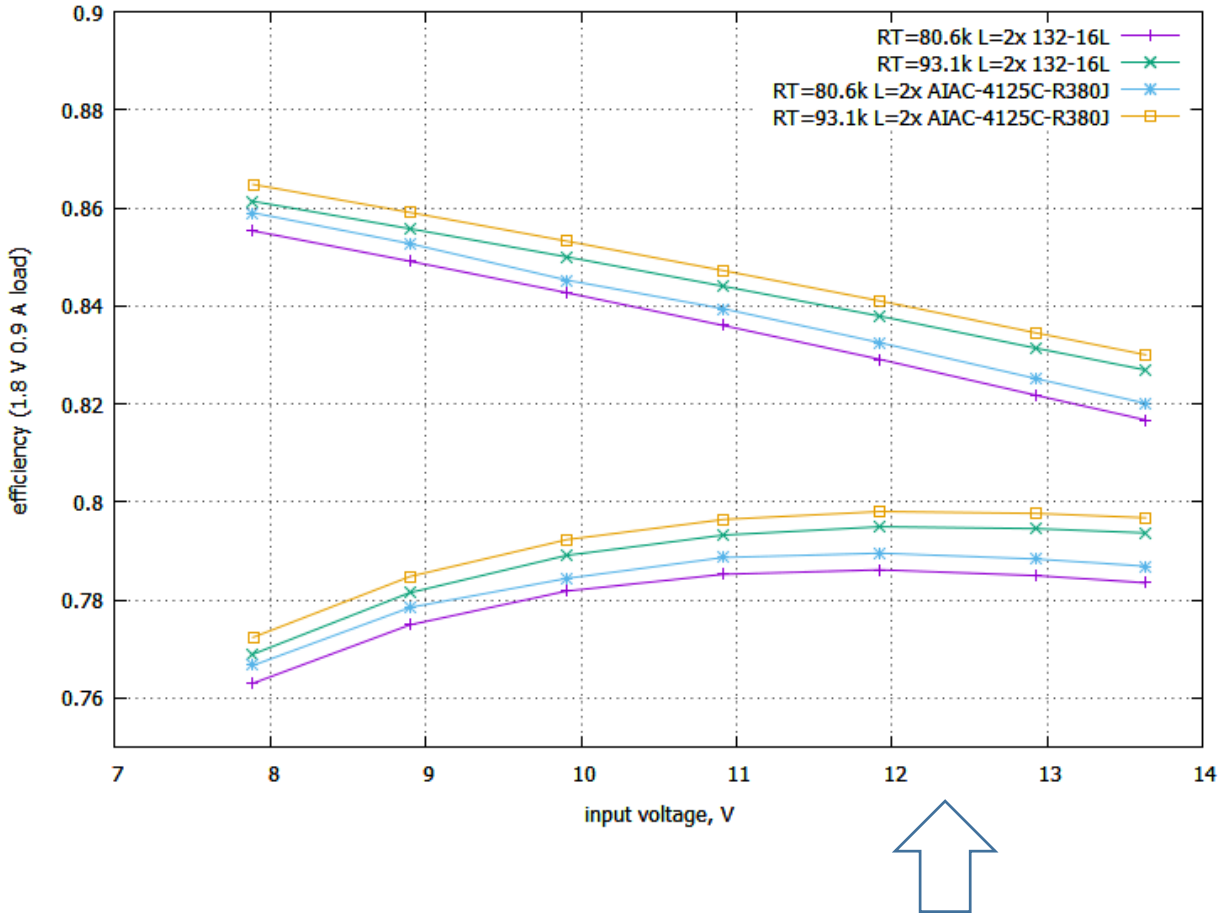


pseudo-toroid
2× 380 nH oriented oppositely, mounted closely
10×10 mm²

ground plane (since the inductors would be over a ground plane on a real board design)

Efficiency to deliver ADC power w/

- board losses only (measured, LTC3601)
- board and 20 AWG cable (50 feet) w/ 4 boards per cable



12 – 13 V is optimal

Compare to efficiency with 0.3 V drop linear regulator

85%

and with **16 AWG** cable (50 feet) to **each** board

73%