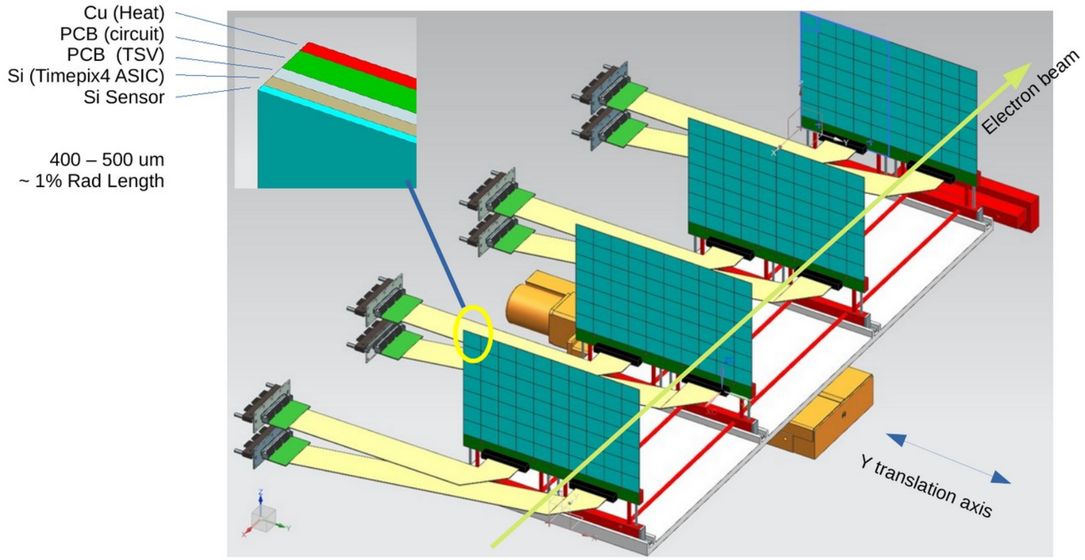
LOW-Q2 SETUP

Tracker

4 tracking layers per Tagger station (30 cm apart – still being optimised)



Pixel-based tracking detectors for a Low Q2 Tagger at EIC – status report:
https://arxiv.org/pdf/2305.02079.pdf

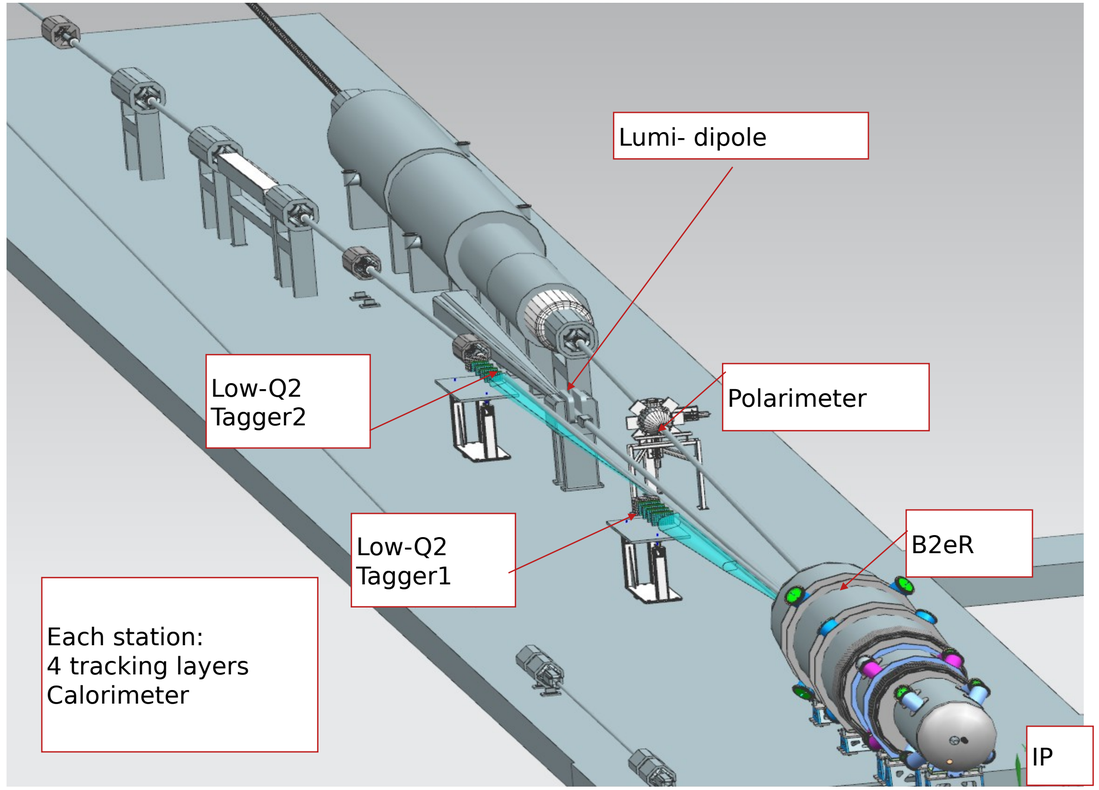
Sensor: Timepix4 + Si Hybrids.

Pixel size: 55x55 um. 448 x 512 pixels per sensor. Area = 6.94 cm^2
Timing resolution 2ns.

Singles rate capability high > 20kHz per 55um pixel

Calorimeter

PbWO4 (?) towers 2x2x20 cm
Total size 26x24cm



Low material budget in front of the setup
2 Si-stations (outside of the primary vacuum)
… but Timepix is designed to operate under 10^{-6} mbar vacuum
working on **possible setup with detector sitting in the secondary vacuum**
Timepix already **demonstrated in high vacuum** (10^{-11} mbar) for beam diagnostics

Location: Tagger 1 23.7 - 24.7 m
Tagger 2 35.7 - 36.7 m

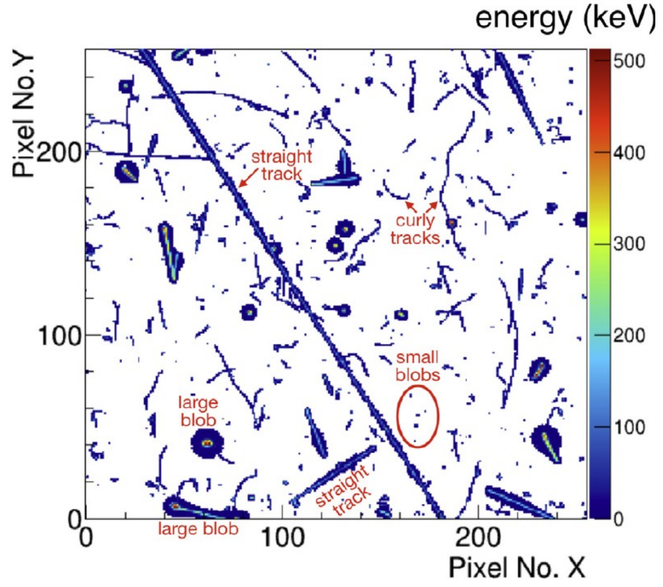
Timepix4

Timepix is a **Hybrid**: ASIC + Sensor (Si, CdTe …)

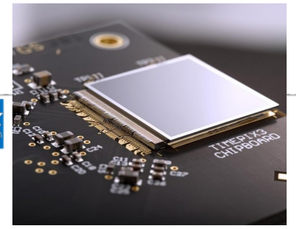
High rate capability

Low noise (individual pixel discriminators)

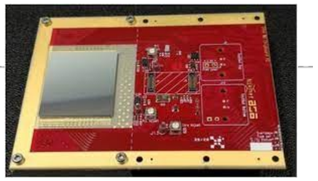
Good PID properties



B. Bergmann, et al. Particle tracking and radiation field characterization with Timepix3 in ATLAS. Nucl. Instrum. Meth. A, 2020. 978:164401. doi:10.1016/j.nima.2020.164401.



Timepix3 → Timepix4



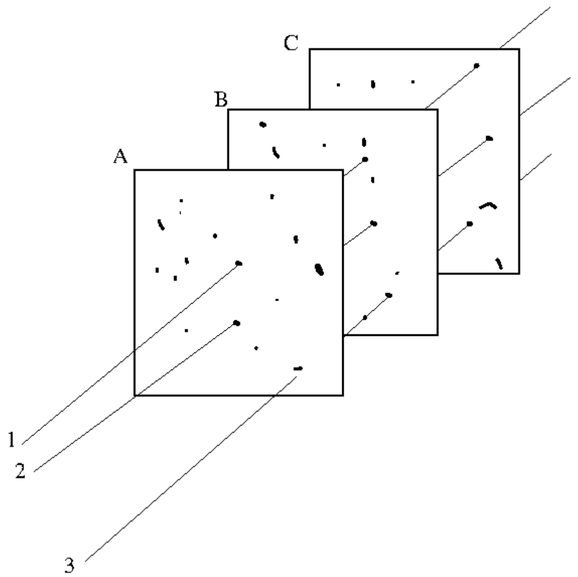
			Timepix3 (2013)	Timepix4 (2019)	
Technology			130nm – 8 metal	65nm – 10 metal	
Pixel Size			55 x 55 µm	55 x 55 µm	
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448	3.5x
Sensitive area			1.98 cm^2	**6.94 cm^2**	
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA		
		Event Packet	48-bit	64-bit	33%
		Max rate	0.43x10^6 hits/mm^2/s	**3.58x10^6 hits/mm^2/s**	8x
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel**	
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)	
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)	
		Max count rate	~0.82 x 10^9 hits/mm^2/s	~5 x 10^9 hits/mm^2/s	5x
TOT energy resolution			< 2KeV	< **1Kev**	2x
TOA binning resolution			1.56ns	**195ps**	8x
TOA dynamic range			409.6 µs (14-bits @ 40MHz)	**1.6384 ms** (16-bits @ 40MHz)	4x
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	**≤163.84 Gbps** (16x @10.24 Gbps)	32x
Target global minimum threshold			<500 e^-	<500 e^-	

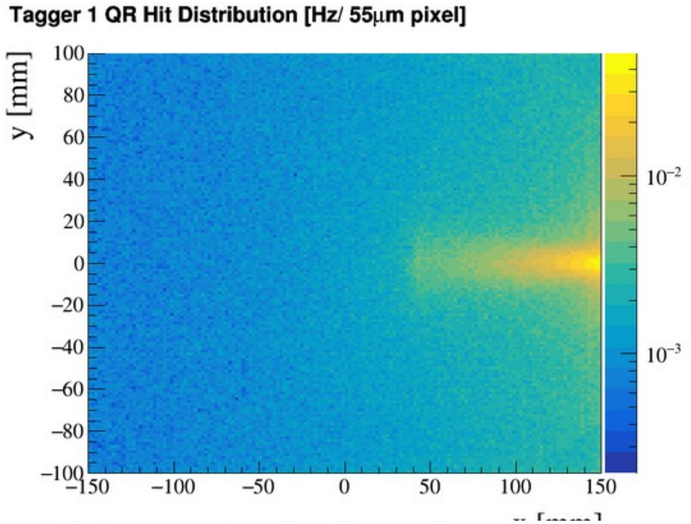
Timepix4 tracker rates from Geant4

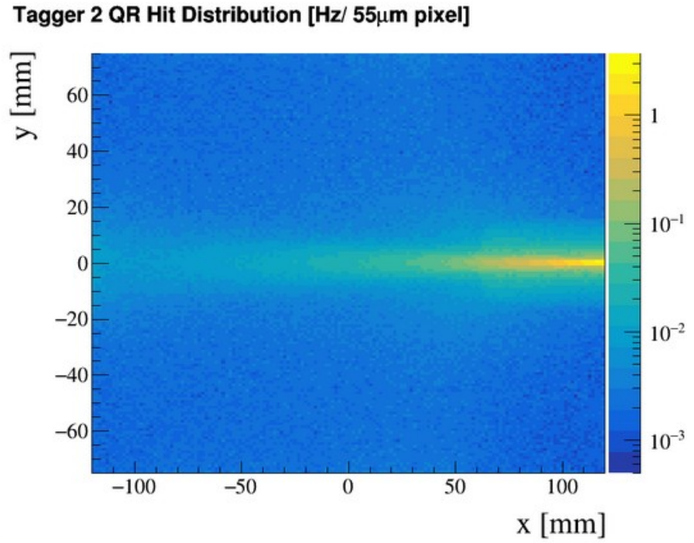
Timepix4 tracking layer design

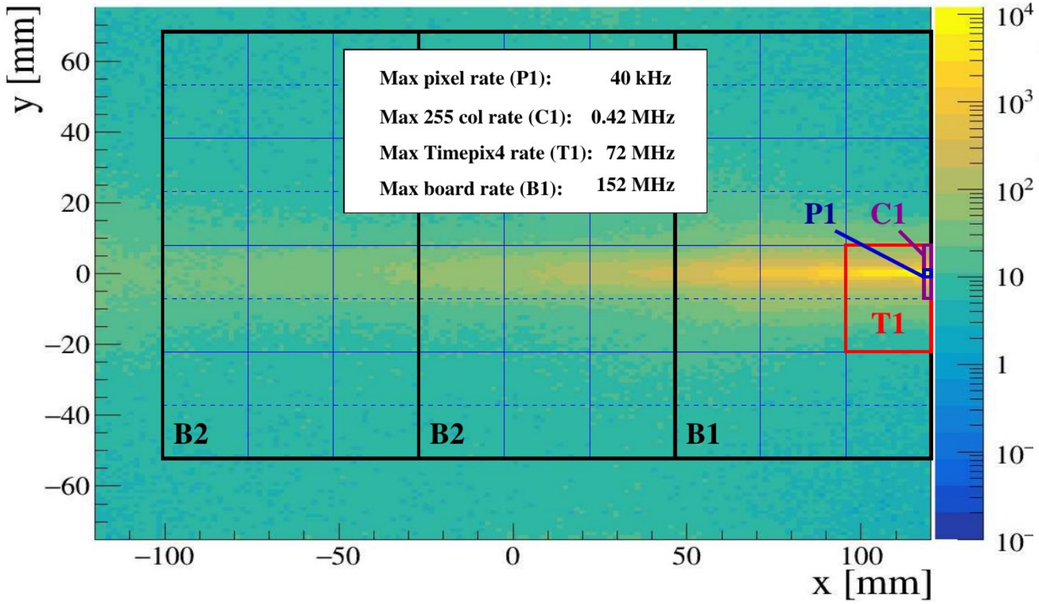
4 layers per tagger (2 taggers)
3 boards per layer
12 Timepix4 per board

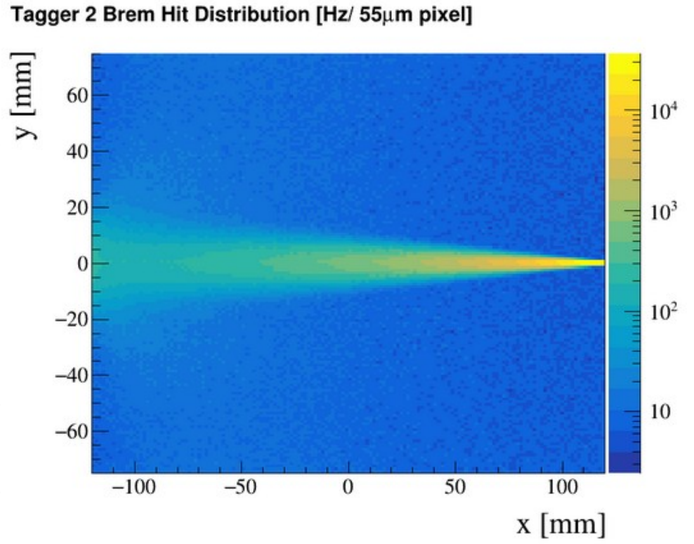
66M pixels
Max board bit rate: 115 Gb/s
Reduced DAQ rate: 20Gb/s











Timepix4 + SPIDR4 Design and prototype

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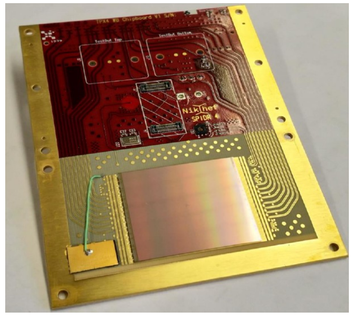
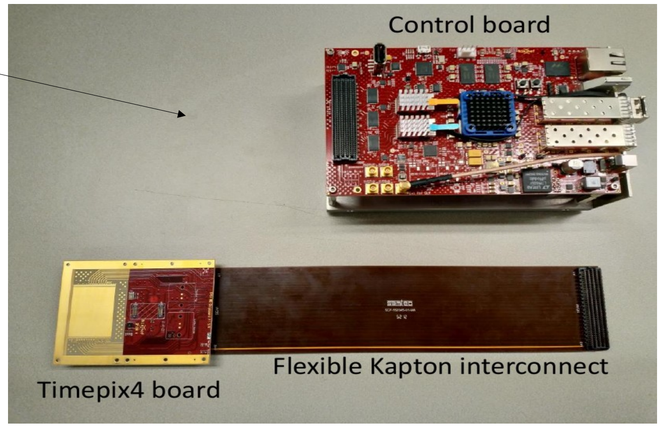
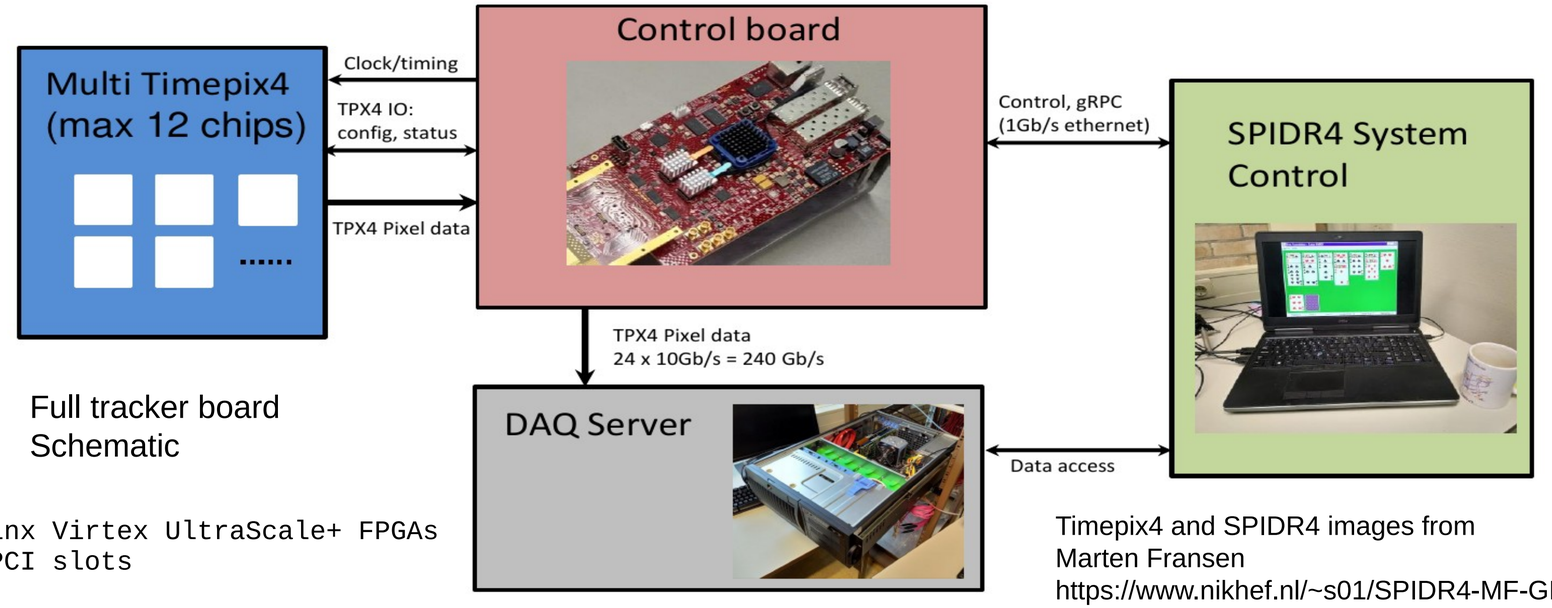
Prototype tracker based on:
2 x Timepix4 + SPIDR4
(Expected from Sept 2023)





SPIDR4: Multi chip, 2 x 10 Gb/s per TPX4 chip



Full tracker board
Schematic

Xilinx Virtex UltraScale+ FPGAs
In PCI slots

Timepix4 and SPIDR4 images from
Marten Fransen
https://www.nikhef.nl/~s01/SPIDR4-MF-GP-apr2020.pdf

Timepix4 + SPIDR4

Meeting local Glasgow Timepix Guru tomorrow.

Any questions?

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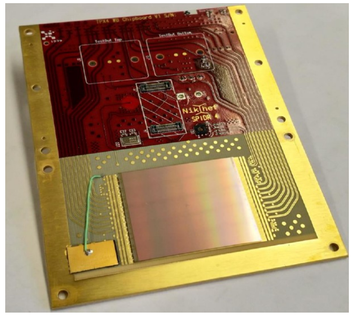

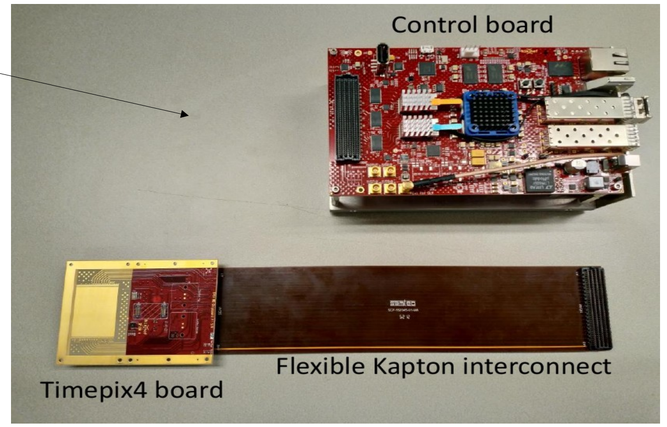

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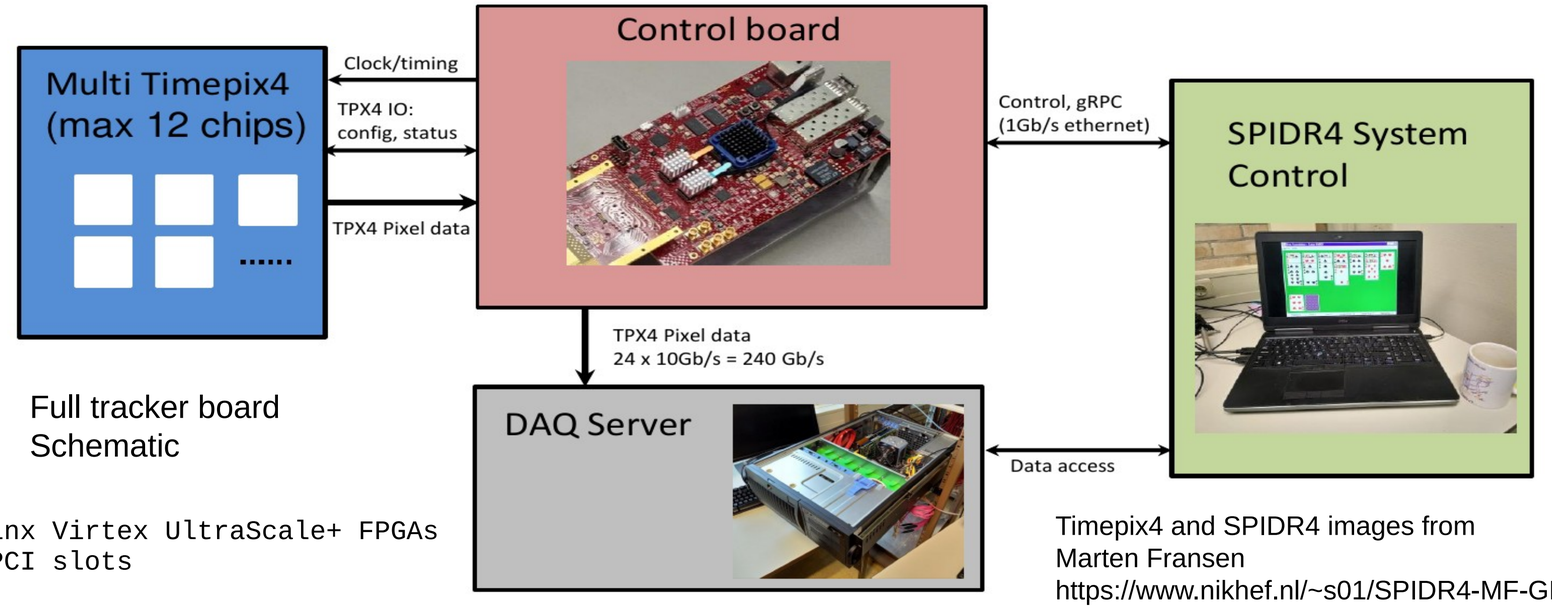

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