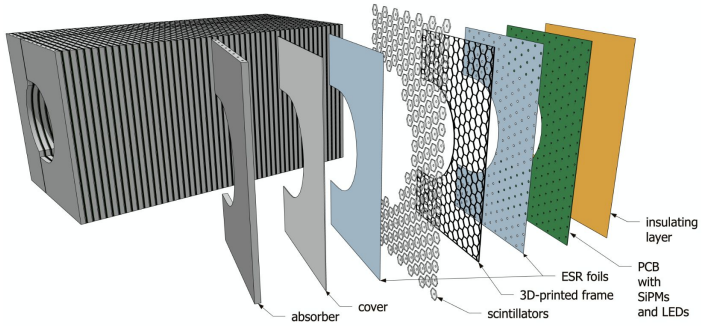
Update on layout of calorimeter insert



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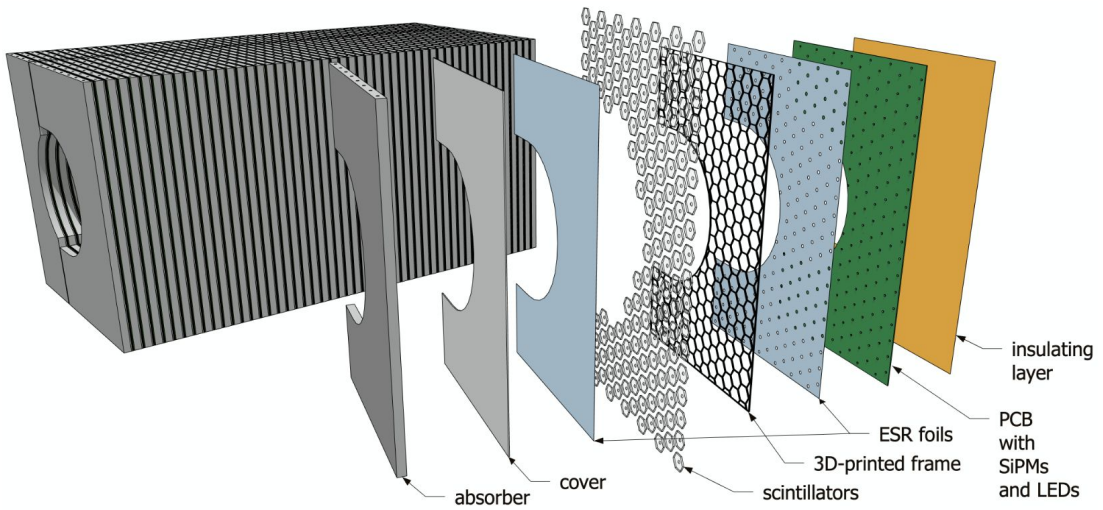
5/24/23

Introduction

- Calorimeter for particles in the 3<η<4 region, very close to beampipe
- Each layer contains a hole tailored to the the fit around the beam-pipe cone
  - Each of the 54 layers* is unique
  - Must be designed *algorithmically*



*plus 1 absorber-only layer

Outline of this talk

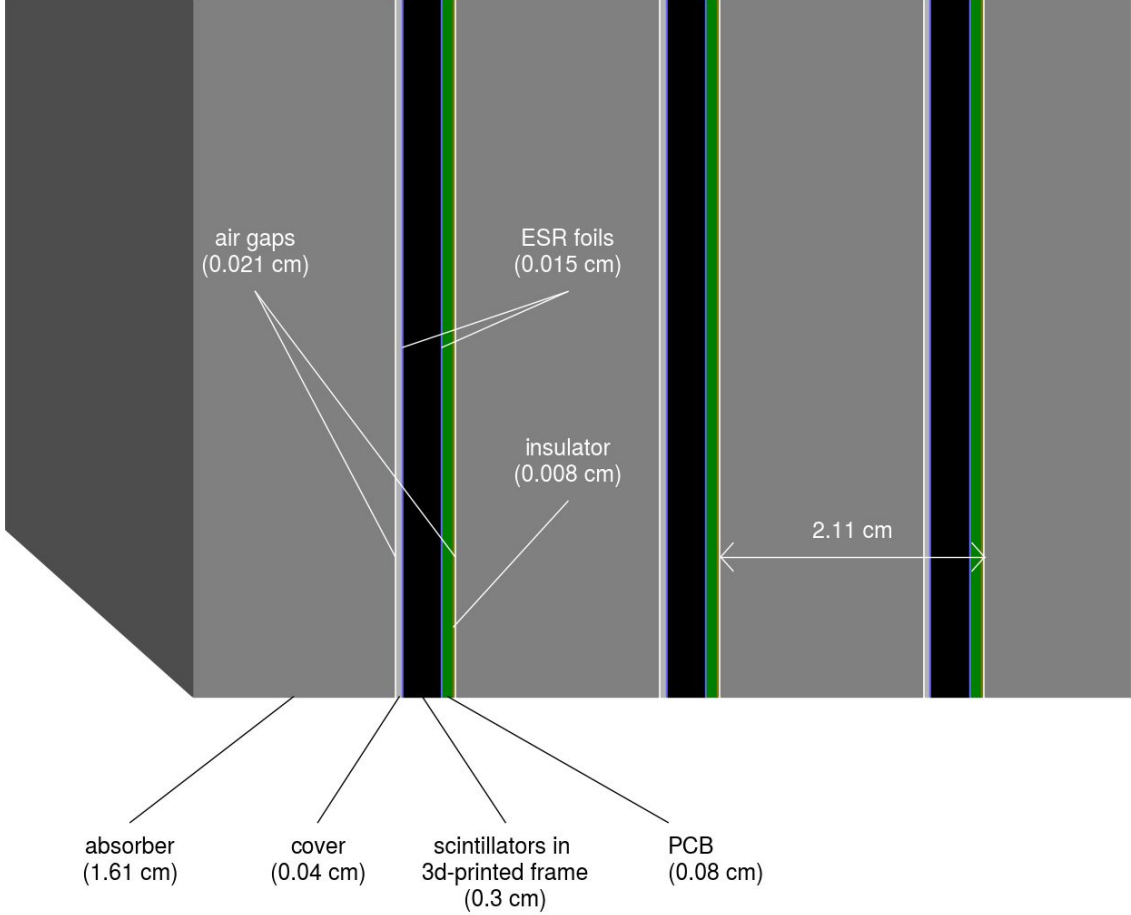
- We are trying to refine our estimate channel density, layout, etc to have an informed discussion with engineers in the future

- Making progress to concretize design aspects of the insert and check viability (given readout constraints, radiation fluence, etc)

- Report progress on STEP model for insert, which we hope could make integration with HCAL easier.

Step 1: Longitudinal structure

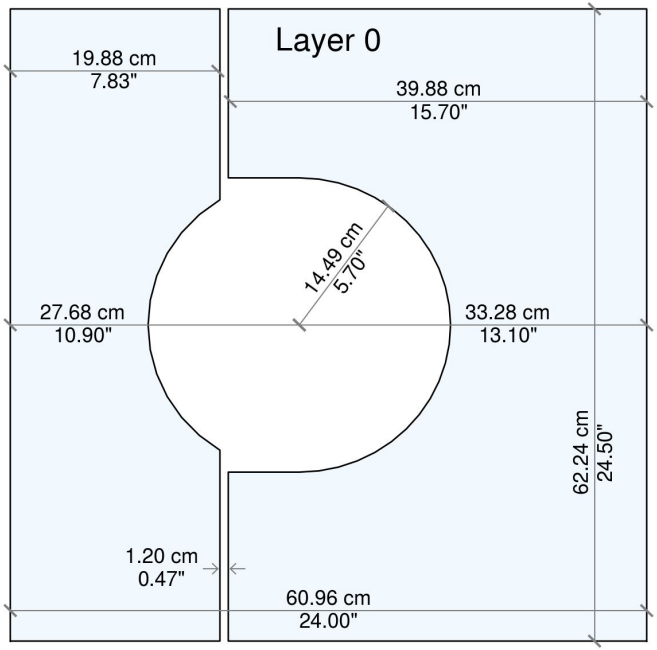
- Smaller layer thickness than in original design* (2.34→ 2.11 cm)
  - Thinner PCBs and covers
  - Also add insulators

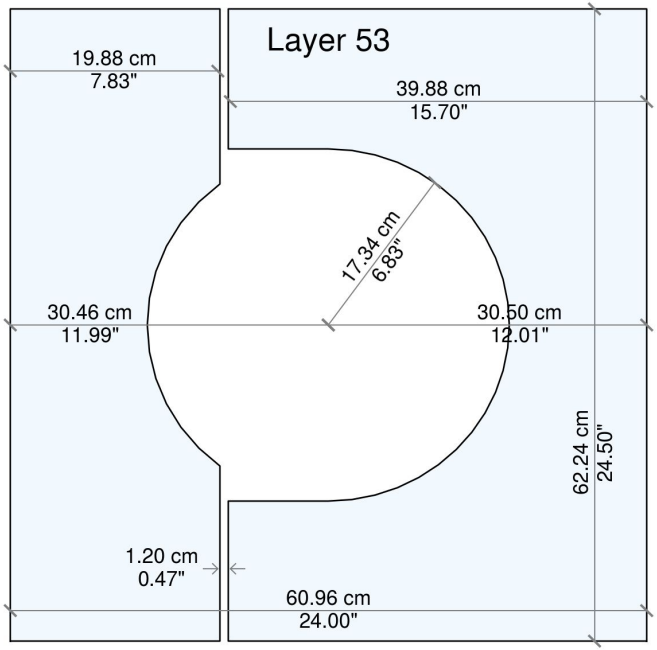


*https://doi.org/10.1016/j.nima.2022.167866

Step 2: Outlines of each layer

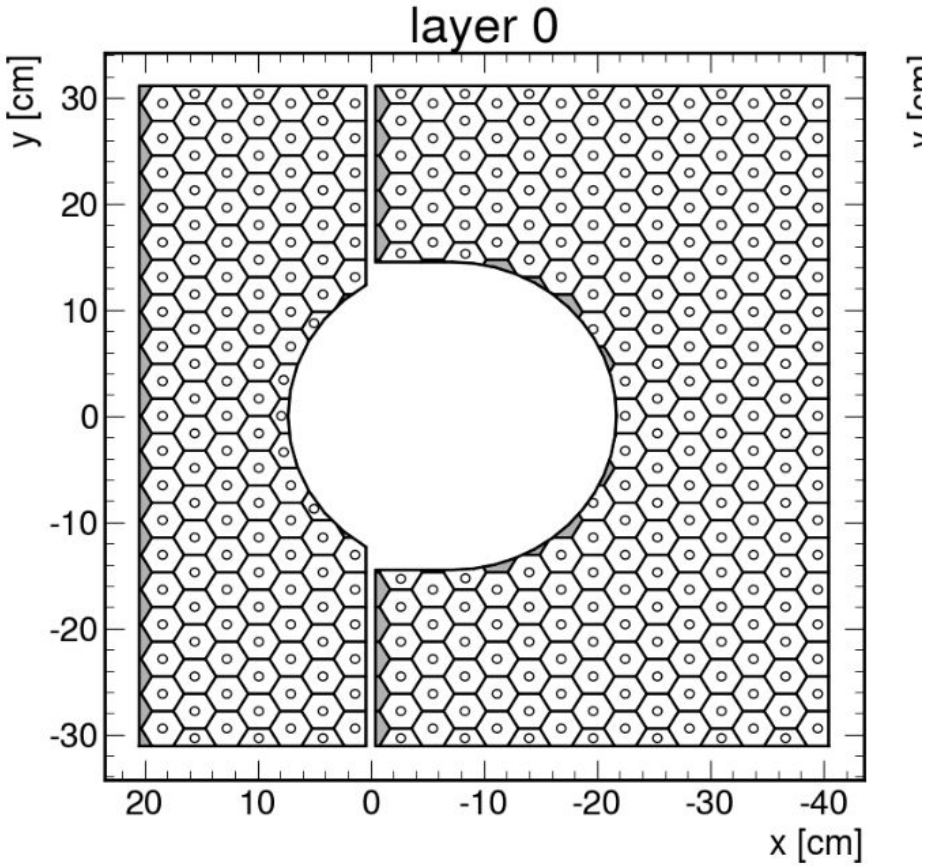
- Diagrams for transverse shape of each layer generated in python, keeps about 40 mm clearance to beampipe as per latest model
- Can give these to a machine shop to create absorbers and covers.





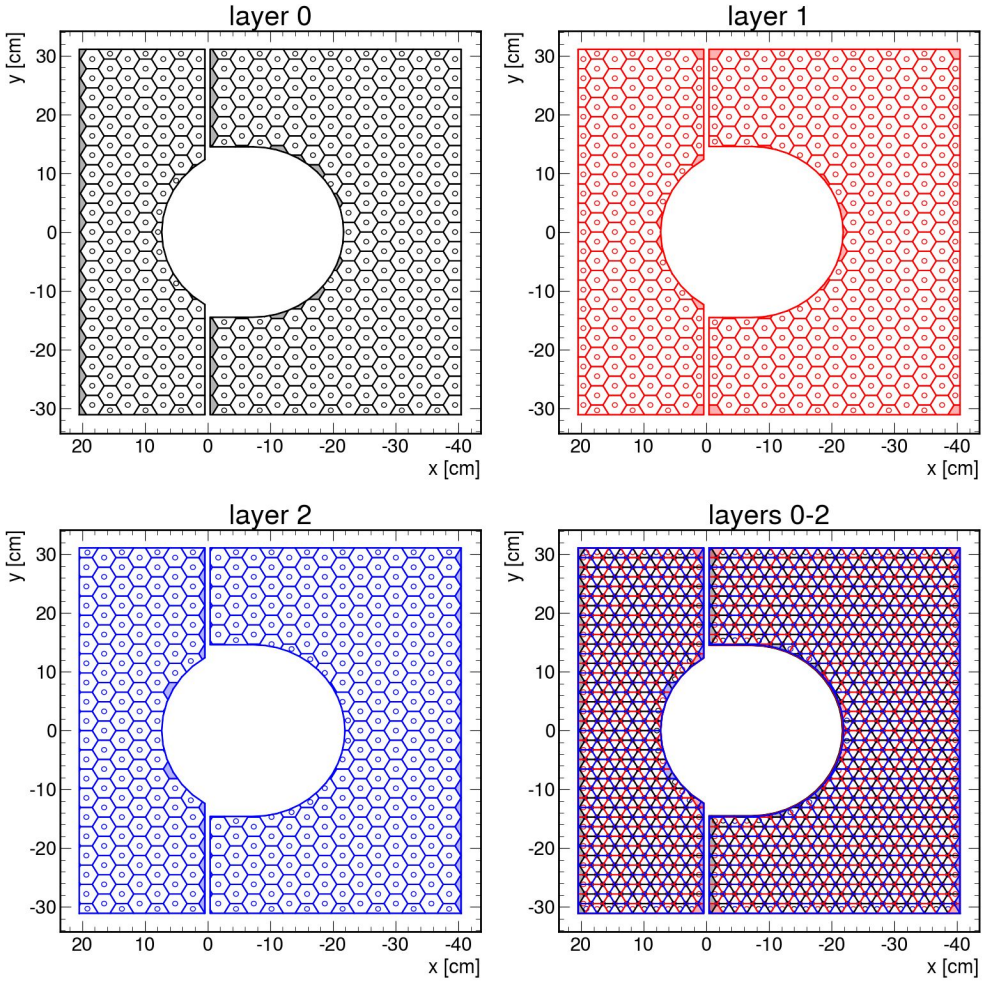
Step 3: Layout of scintillator tiles

- We wrote an algorithm to determine where to place cells, when to include partial cells on the edge, etc.



Step 3: layout of scintillator tiles (continued)

- Cell positions are staggered from layer to layer
  - Covers the deadspace near the edge
  - Also may improve the spacial resolution of the calorimeter



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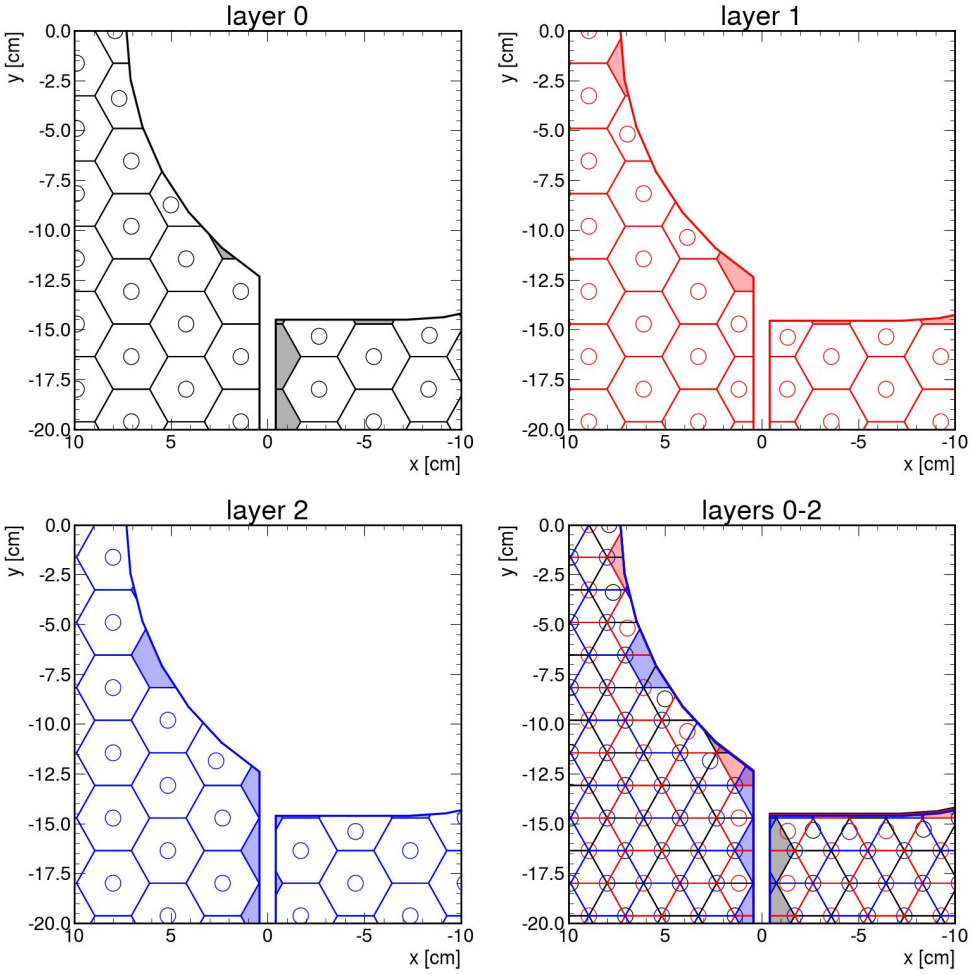
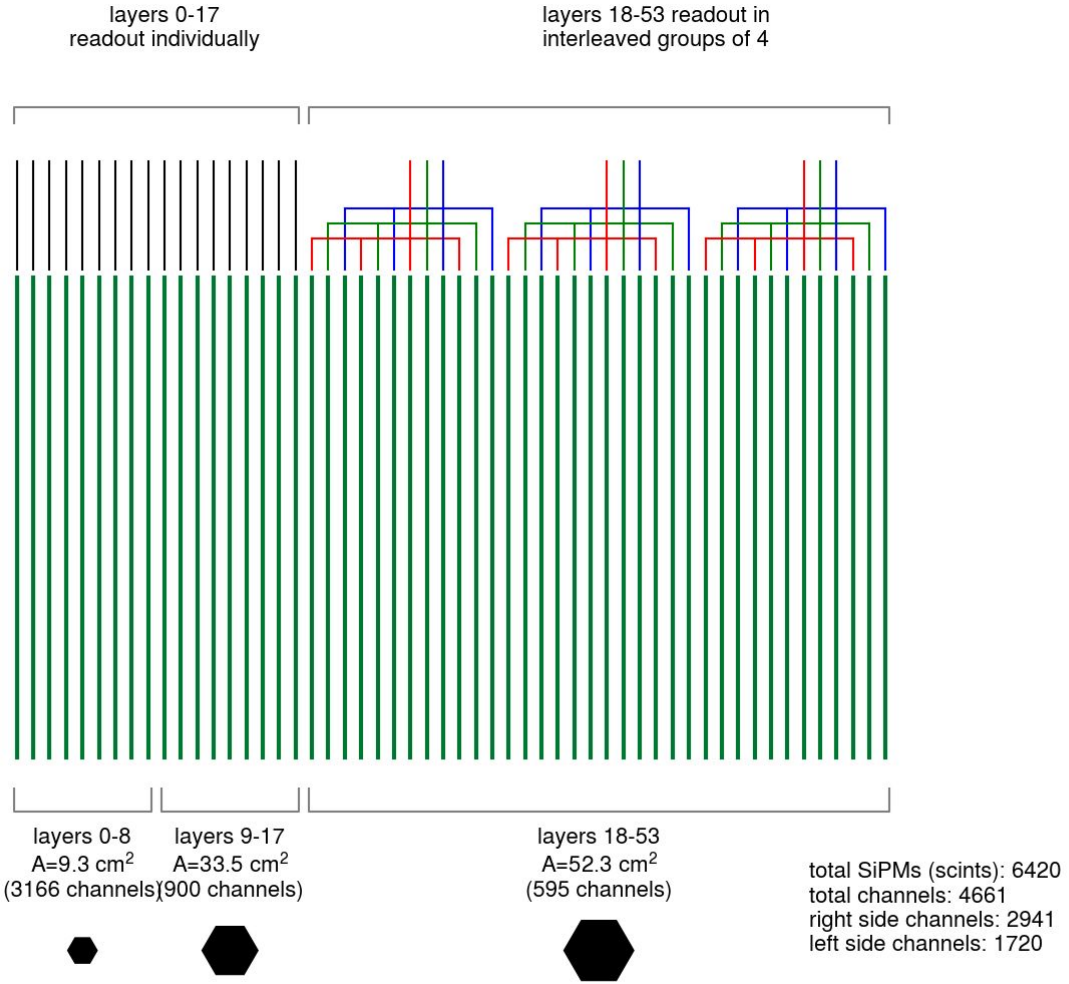


Layer-by-layer design

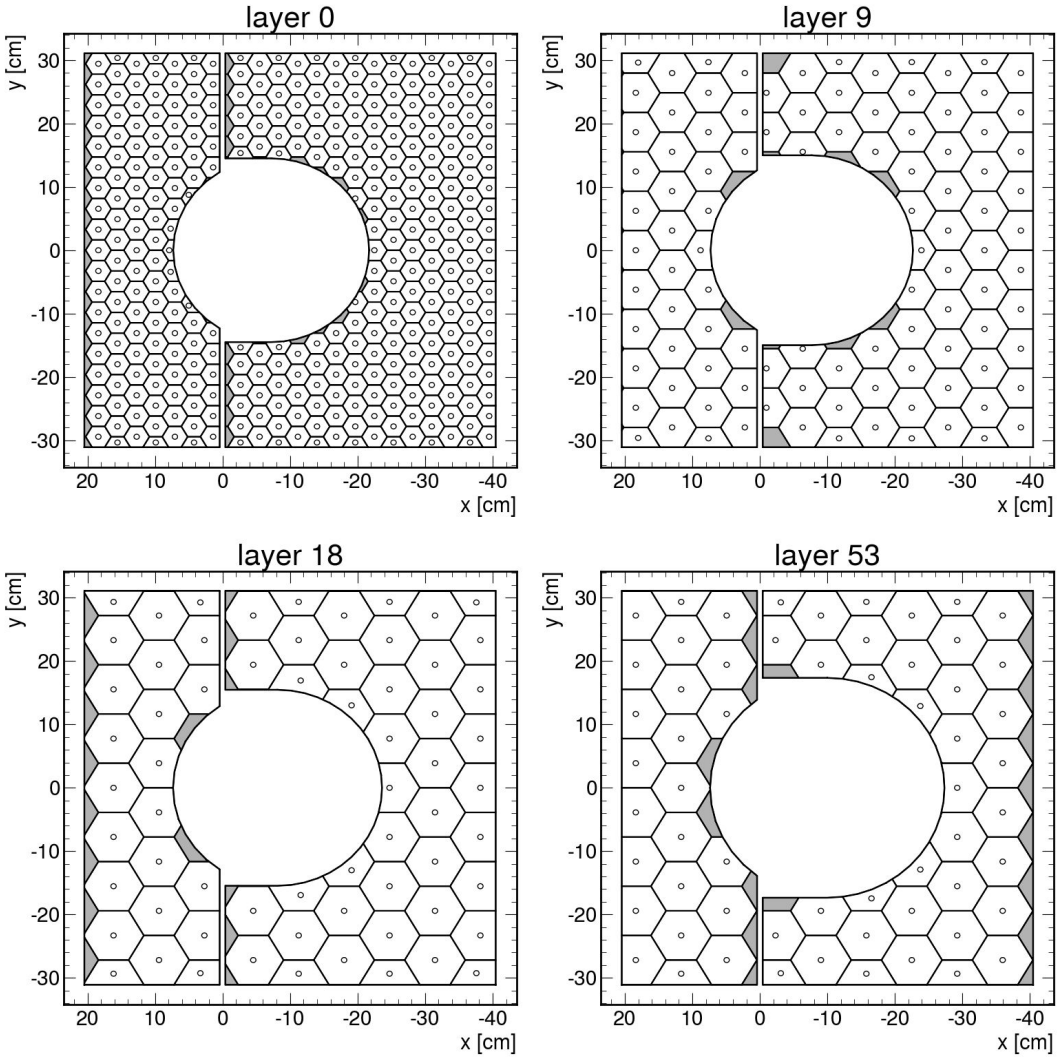
- 3 granularities
- Max SiPMs on any half-layer is 214
- Downstream layers readout in groups (to reduce channel count)
  - ~4.6k readout channels total (~6.4k SiPMs)



Hexagons

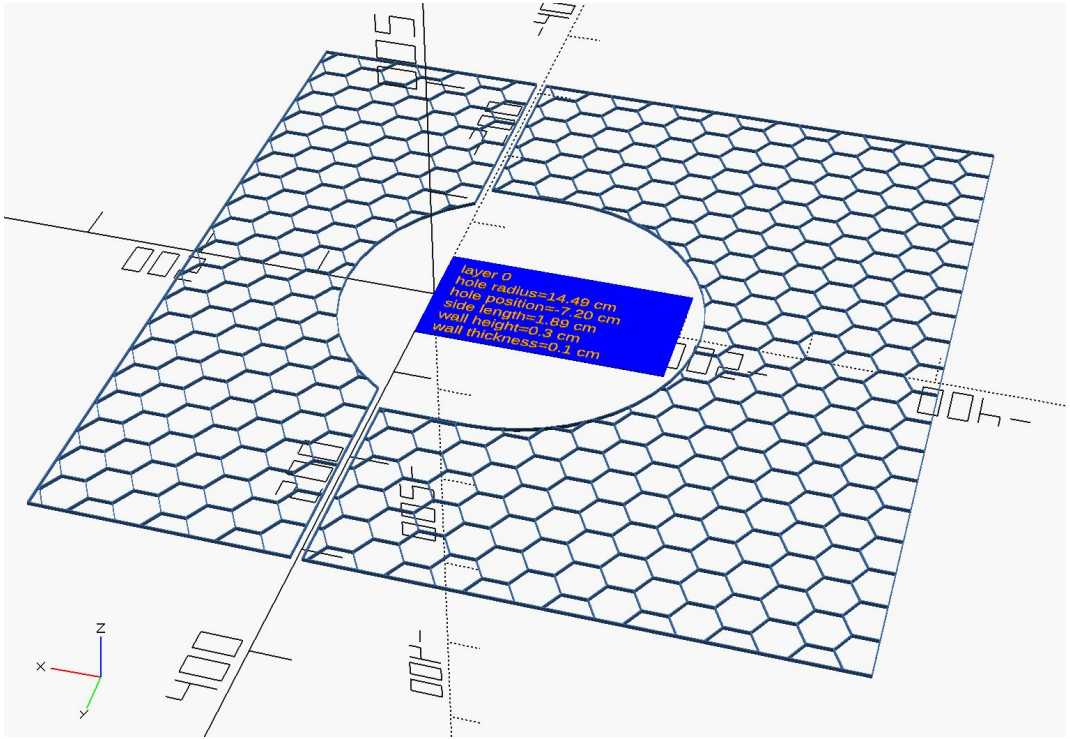
- Minimizes the max distance to the center for a given tesselating cell area
- Minimize dead area in tessellation for area that varies layer by layer
- Distance to center is what determines light yield and uniformity
  - Largest cells in HG-CALI have same maximum distance-to-center as CMS's HGCAL largest square scintillators (which are 5.5x5.5 cm^2), but ~30% more area
- In other words, for a given light yield, hexagons maximize area.

Some representative layers



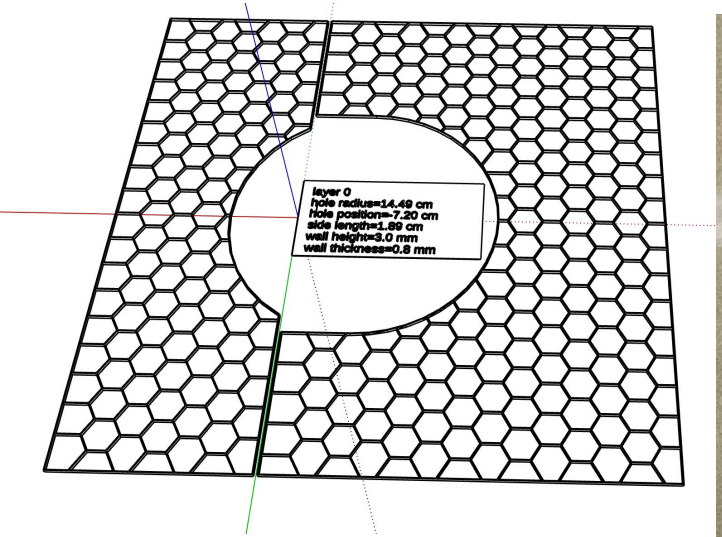
Step 4: Generate stl files for the scintillator-holding frame

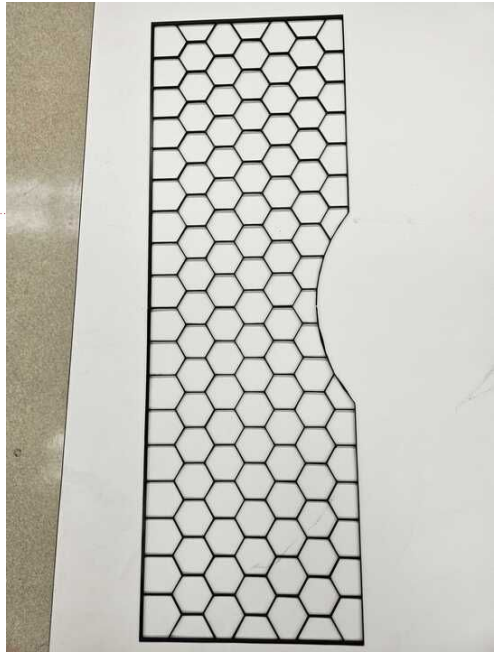
- Frames have the same transverse dimensions as the absorbers, covers and PCBs
- Python: write out positions of start and end of points of all cell boundaries
- OpenSCAD: turn these into 3D walls between cells in an STL file, which can be printed.

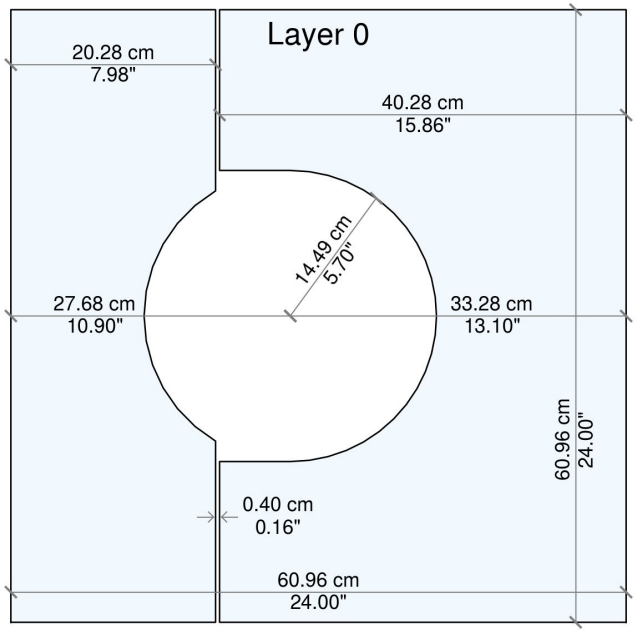


Parametric design of HG-CALI

Models for 3d printed frames and engineering diagrams for absorbers for each layer can be made quickly in a Jupyter notebook



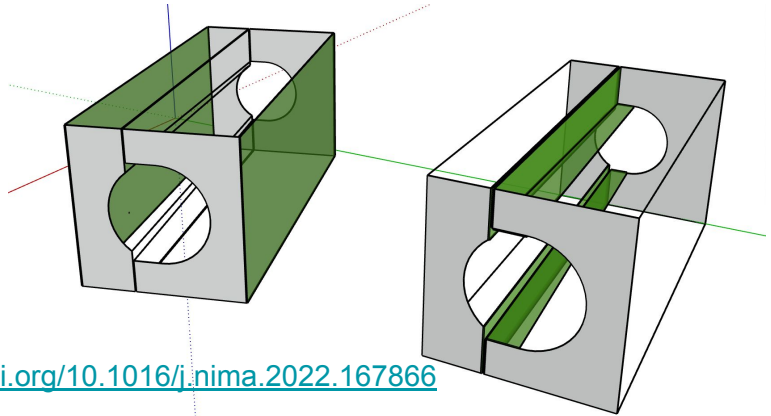


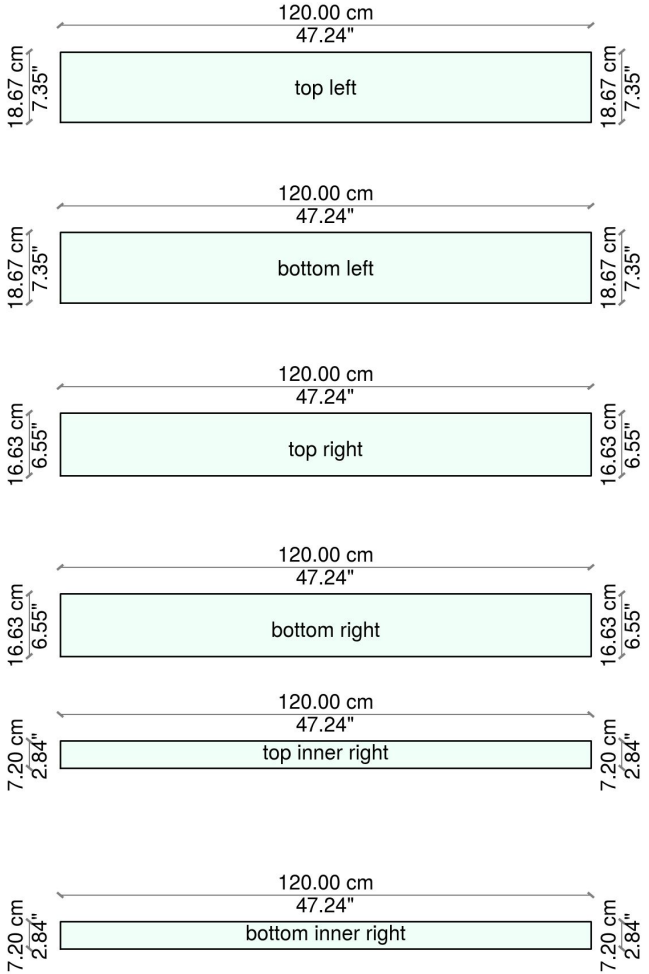


*Note: printed frame shown was from earlier version of design than current one.

Backplane design

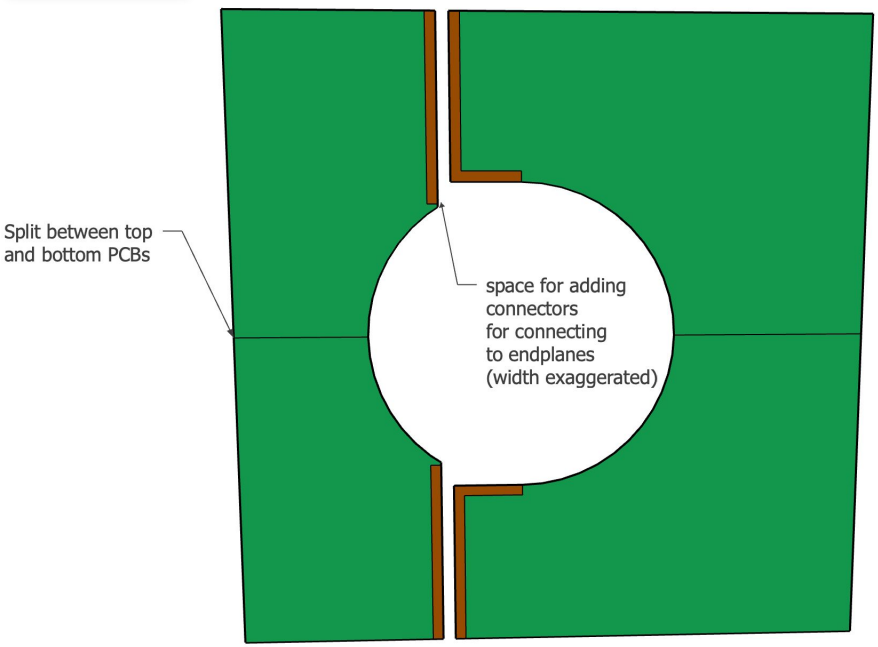
- Original design*
  - Had backplanes locked between HG-CALI and endcap HCal
  - Locked in place for ever
- Possible alternative (suggested by Friederike) uses inner surfaces
  - Pros: Backplane is accessible
  - Cons: less space, requires higher layer-count PCB





*https://doi.org/10.1016/j.nima.2022.167866

Possible layout of connectors to backplane*

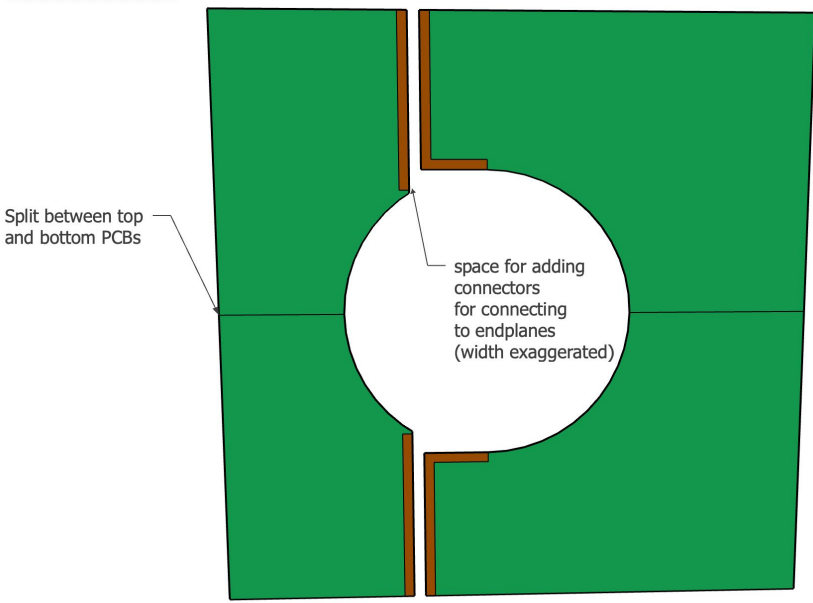


- Maximum of 214 SiPMs per side on any layer

*Note: we just are trying to estimate number of channels, channel density, layout, etc to have an informed discussion with engineers in the future

How much space should connectors take up?*

- An engineer informally suggested us to use 0.8 mm pitch connectors, and 2 leads per signal
  - Need at least (0.8 mm)^2*214*2/2=1.4 cm^2 for each of the right quadrants in the first layer.
  - ~16+17=35 cm available on edges.
    - 1.4 cm^2/26 cm~0.6 mm thick, about ¾ of a pitch.
    - About ¾ of the available space for connectors is needed.

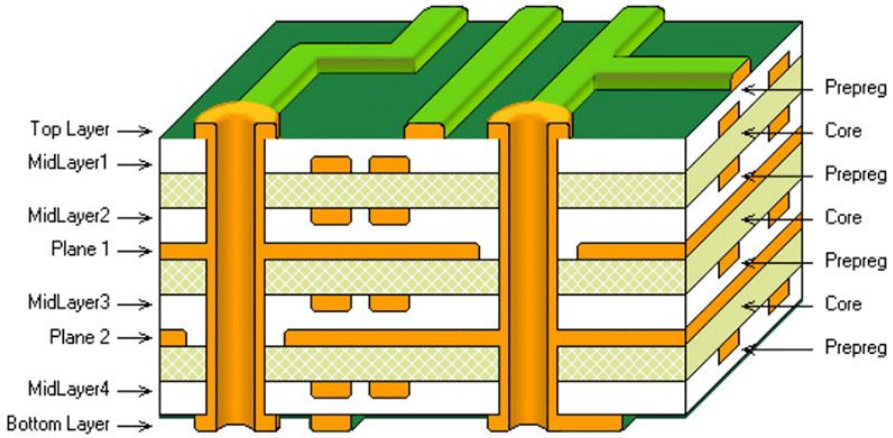


**Note: we just are trying to estimate number of channels, channel density, layout, etc to have an informed discussion with engineers in the future*

Backplanes: How many layers in PCB?

**Note: we just are trying to estimate number of channels, channel density, layout, etc to have an informed discussion with engineers in the future*

- An engineer informally suggested us “Differential pairs with 200 µm traces, 200 µm between them, with 500 µm between them → 1.1 mm per signal”
- 127 µm for each layer
  - Alternate ground planes with signal layers
- Original design:
  - (2912 channels)/(60 cm available for backplanes)/(1.1 mm per signal)* (2 to account for ground planes) =10.3
  - Probably would use 12 layer PCB for machining purposes
- New design:
  - Add narrowest part of each backplane surface on right side: 39.2 cm available
  - 16.3 → 18 layer PCB
    - ~2.3 mm thick if using 127 µm between layers
  - For left, same exercise yields 10.9 → can use 12 layer PCB

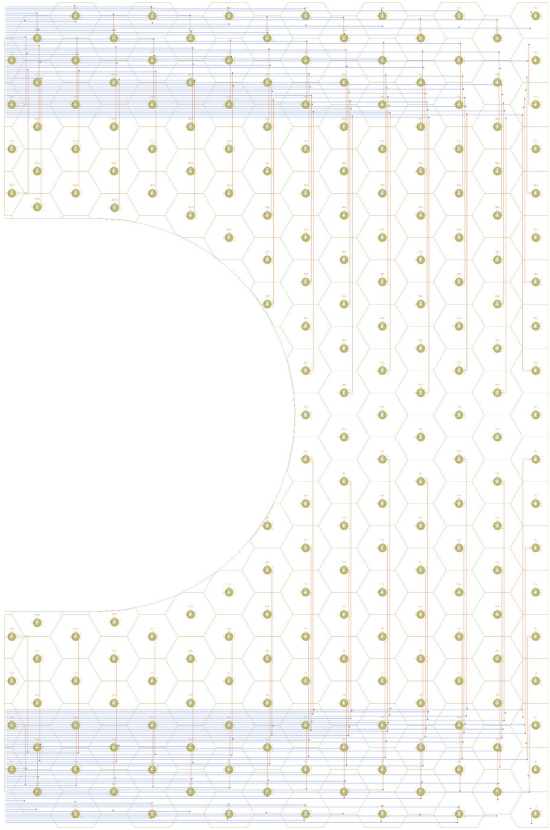


Step 4: PCB design*

*Note: we just are trying to estimate number of channels, channel density, layout, etc to have an informed discussion with engineers in the future

- Use same edge-cuts as frames, absorbers and covers
- Place pads for SiPM and LED (for calib.) under each dimple using positions from dataframe.
- Silkscreen shows row,col, and cell outlines
- Connectors to backplane TBD
    - Have shown how the SiPMs can be routed to an idealized connector with 2 rows of 0.8 mm using a python script I wrote

Connector goes here

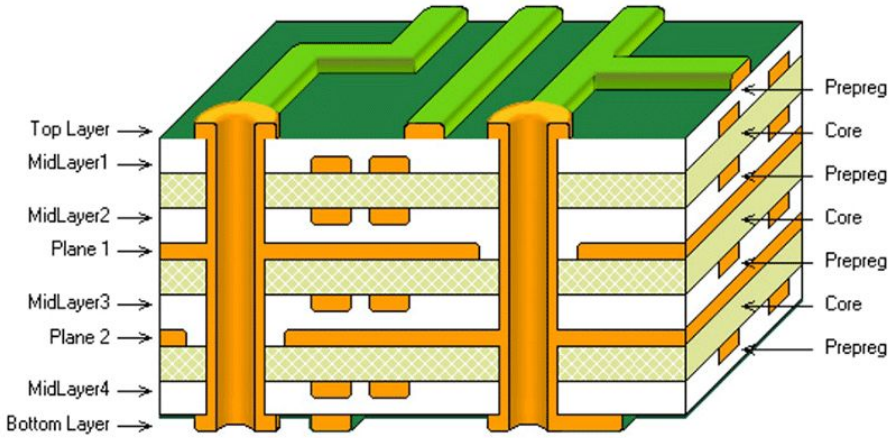


Connector goes here

Thickness and number of layers in SiPM-carrying PCBs

- 0.8 mm, 6-layer PCB should be sufficient:
  - Top layer should be flat so that ESR foil lays flat
    - May require blind or buried vias to accomplish this
    - Could be used as ground plane
  - Trace density largest near connector to backplane
    - Assuming 1.1 mm x 1 layer needed for each pair, with 0.8 mm single- or even a double-row connector, bottleneck is overcome
  - Some of the layers will mainly be used for bridging over traces in other layers

*Note: we just are trying to estimate number of channels, channel density, layout, etc to have an informed discussion with engineers in the future



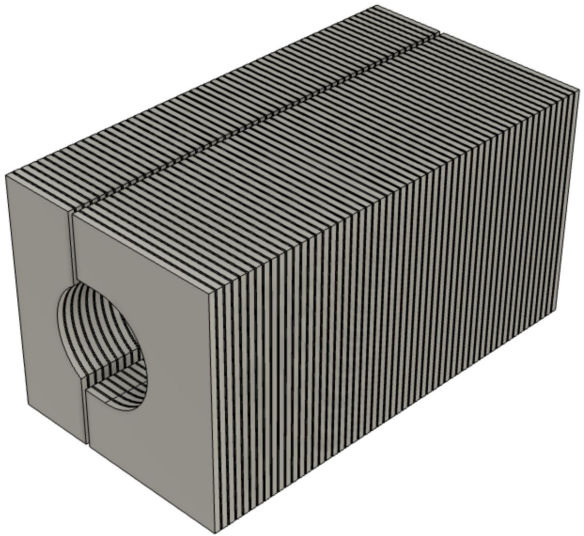
Status of STEP model*

Includes absorber geometry, PCB layout, foils and covers.

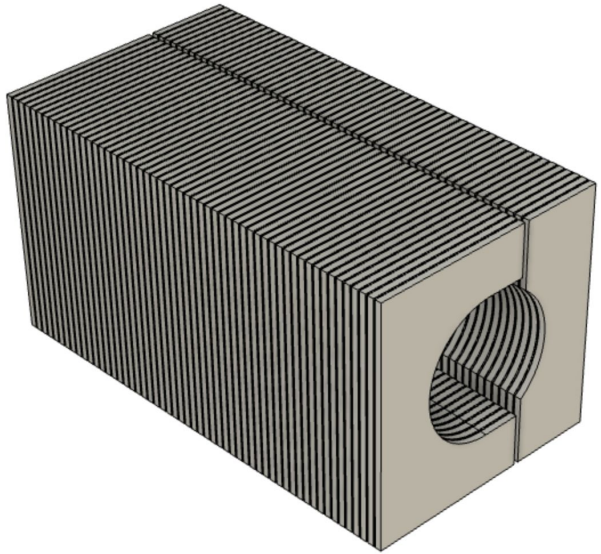
scintillators and 3d-printed frame to be added

*Note: we just are trying to estimate number of channels, channel density, layout, etc to have an informed discussion with engineers in the future

Front face



Back face



Summary and conclusions

- I have implemented algorithms for designing most of the components of HG-CALI, primarily working in Jupyter notebooks.
- Modifications to the design parameters can be implemented quickly and incorporated into the design if needed.
- Our initial estimates for channel density, PCBs etc seem OK, doable
- TODO:
  - TBD: connectors from SiPM-carrying PCB to backplanes
    - Space between left and right parts of detector
    - Need to subtract some space from layout for connectors
  - PCB design for backplanes