

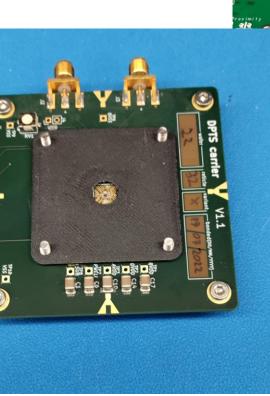


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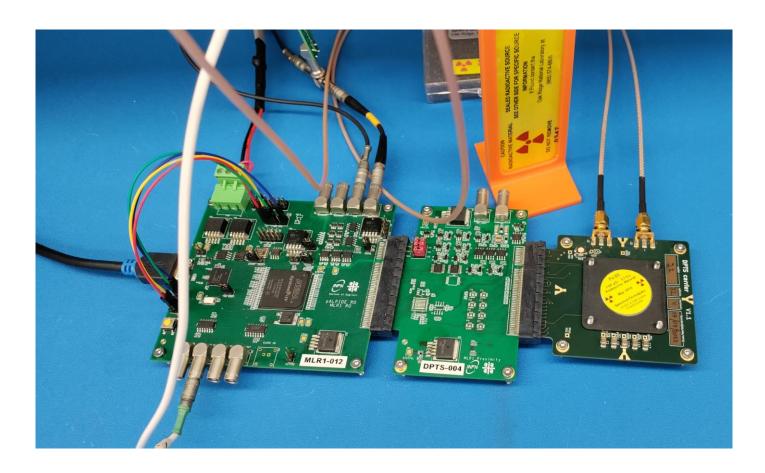


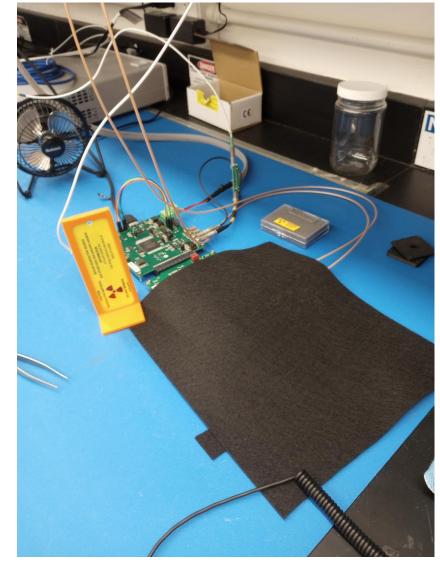
3-D printed a fixture for Fe-55 Data Taking





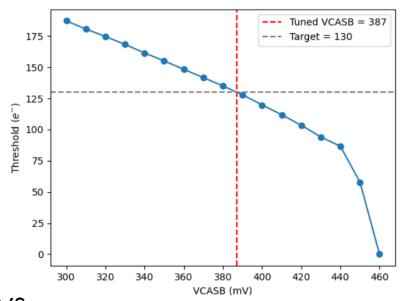
Fe-55 Data Taking Setup



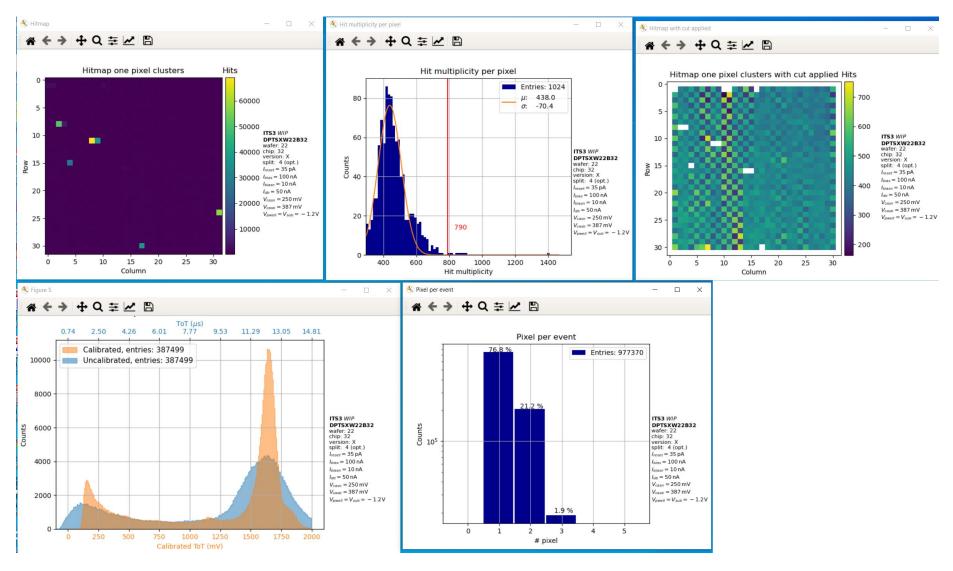


Fe-55 Data Taking

- Obtained a Fe-55 from ORNL source custodian
- Initially took 650,000 waveforms in about 2 days
- Successfully went through all of the calibration steps as instructed by M. Buckland
- Tuned VCASB to 130 e-
- Took an additional 400,000 event in another 2 days
- Spectrum looks reasonable, still need to continue analysis to fit the peaks so the results can be compared to other chips



Fe-55 results (~1M waveforms)





CML Digital Output Buffering Characterization

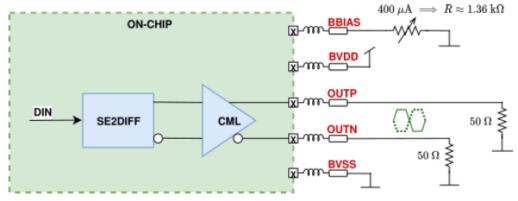


Figure 3: Digital Output Buffering



BVDD, BVSS – output CML buffer domain BBIAS – Digital output buffer bias

Recommended CML BVDD: < 1.32V

Outp, Outn termination resistance: 50 Ohm

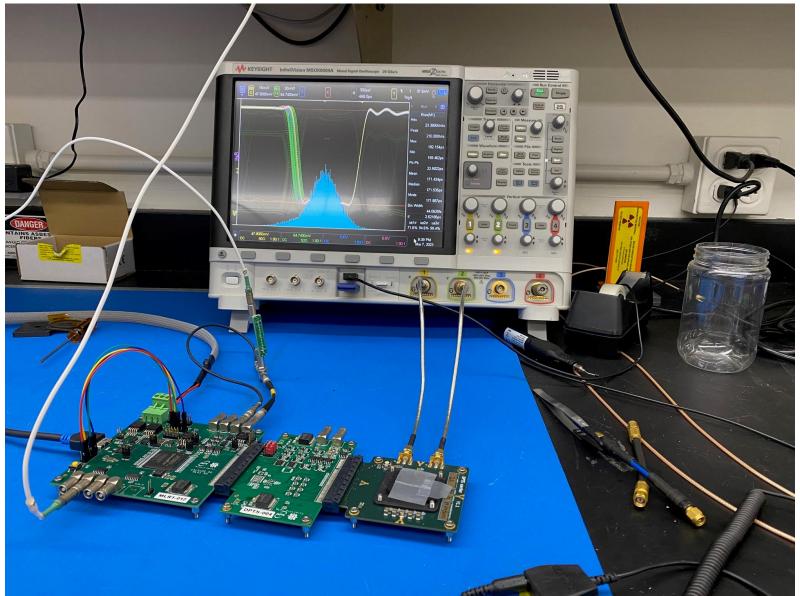
BBIAS current typical: 400 µA BBIAS current max : 450 µA

Adjusted typically to 400 μA via RV1 on carrier card to have a voltage drop across R5 of $1k\Omega$ of 400 mV (probed @ J4)

Expected Rise/Fall time (from datasheet):



Test Setup

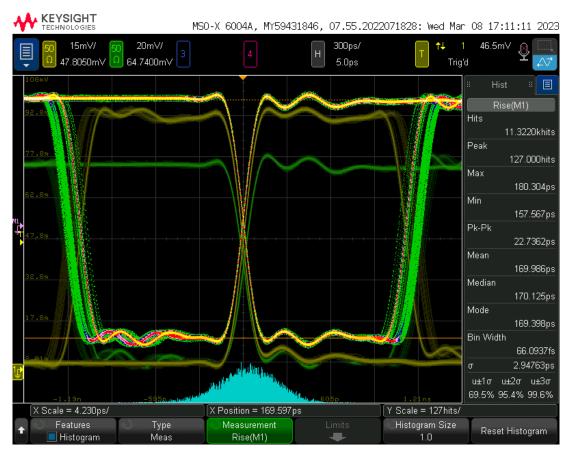


Some Remarks

- Use "standard" settings for various voltages:
 - VBB = -1.2 V, VCASB = VCASN = 300 mV, IRESET = 10 pA, IDB=100 nA, IBIAS = 100 nA, IBIASN = 10 nA
- Initially tried with longer cables, significant impedance load
- Short cables reduced rise/fall times (30pF / foot, i.e. 10pF)
- Fabricated a PCB to provide controlled impedance loading of the output and proper test pads for scope
 - Unfortunately, the scope bandwidth limits the rise/fall time



Scope Measurement





Rise Time Fall Time



Rise and Fall Time Measurements



High Statistics "Eye"



PCB for output probing

