Readout & DAQ
dRICH interim update

Pietro Antonioli, Davide Falchieri

INFN Bologna

Context of this update to DAQ group:

- Preparing for dRICH review (5th July), eRD submissions (7th July) and INFN budgeting (2024 + multi year) various refinement in progress
- This is an iterative process, not yet a firm plan. We want to get feedback/advice by DAQ group as usual
- Next iteration (if you are interested): 14th June 8:00 AM EDT → dRICH meeting

(plus some news we recently got from CERN we want to share)

Preparing 2024 RDO plans (in second semester 2023)

During 2024 we need to build a prototype RDO card (”close to final”) where we demonstrate:

- We can fit within space
- We start talking with ePIC DAQ (“FELIX based”)
- We are able to serve 2023 electronics (old ALCOR32/old FEB with FireFly connectors)
- We operate test beam 2024 (October) with optical link readout and RDO

The exercise must aim:

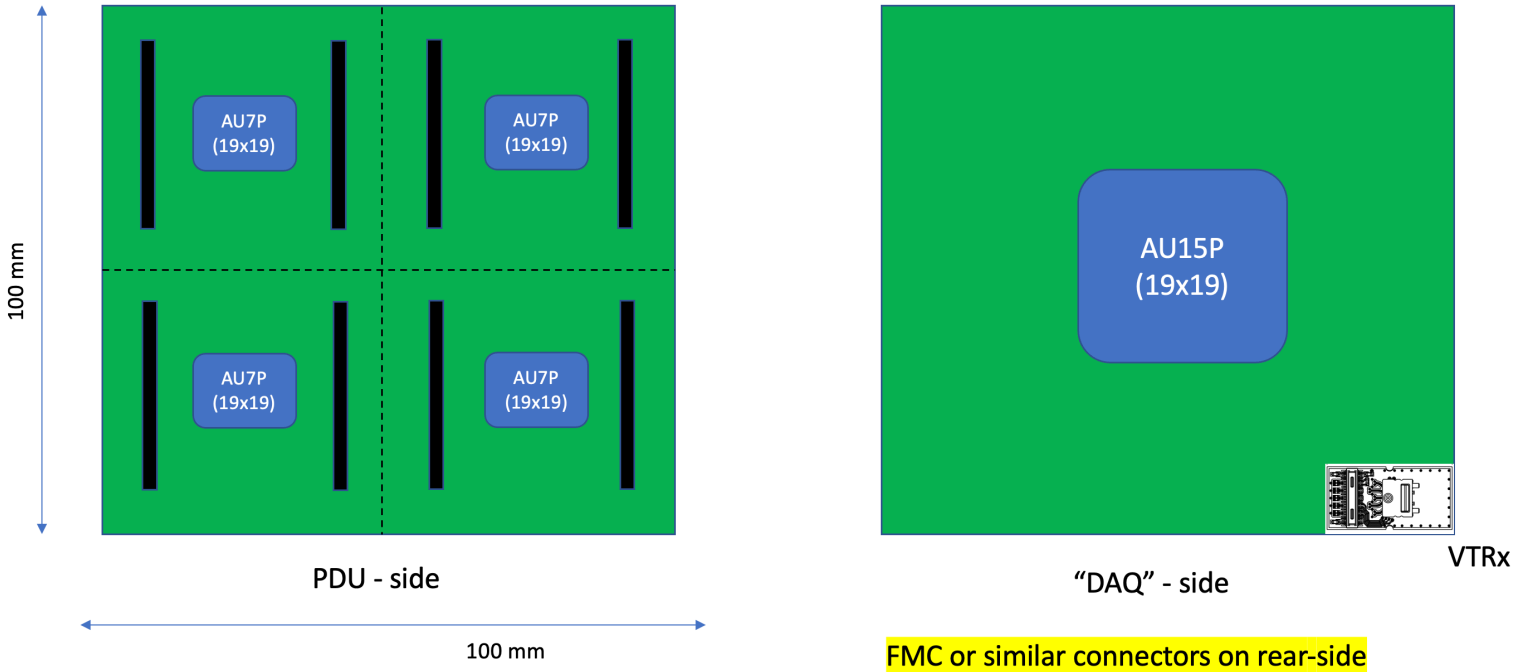
To fully define specs of RDO (possibly by December 2023)
To select FPGA candidate (and it might include some radiation test)
To define ancillary services on RDO, we will work out within dRICH electronics the divison of work (LV, watchdog, communication, …)

About throughput we recently had a chat with Elke. She made clear an interaction tagger will be available. This can really save us a lot of complications on data reduction (and help us to correctly select RDO/DAQ resources).

→ throughput will be modelled assuming an interaction tagger signal can reach dRICH DAM with max 2 us latency

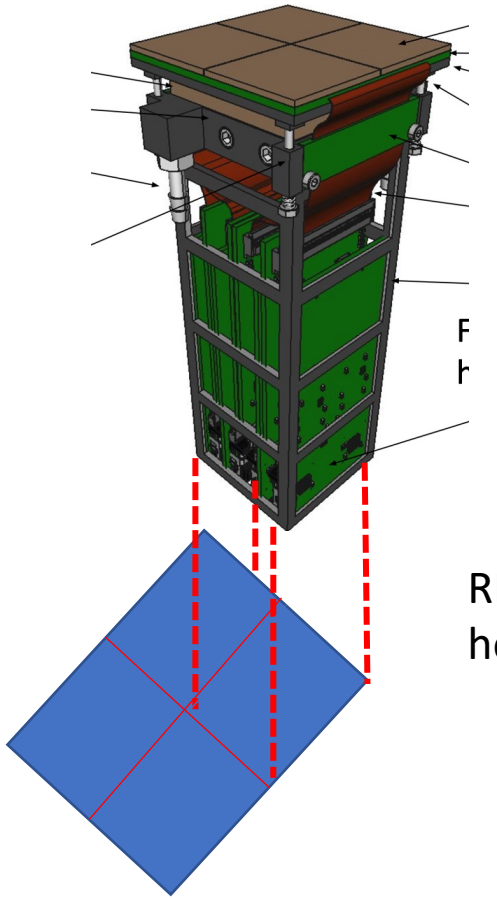
Where we were (few weeks ago)

RDO challenges: potential design (2b)



03/05/2023 dRICH meeting 18

RDO made with two cards:
- slave RDO (1 for 1 FPU) (4 piggy backs
- a master RDO (aggregating 4 slave RDO)

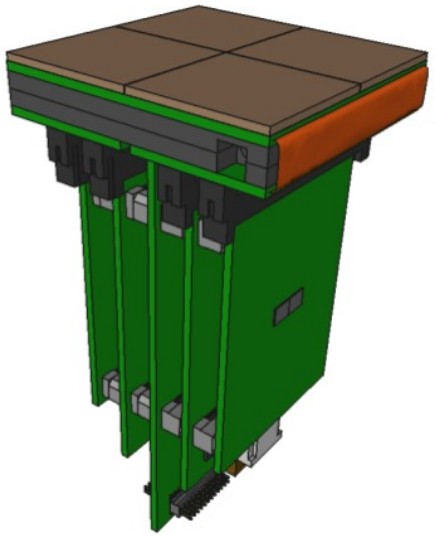


RDO "plugged" horizontaly

The need of two hierarchy of FPGAs descends from PIN I/O requirements

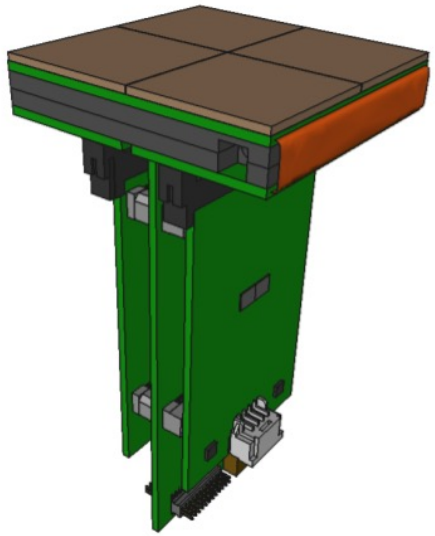
Where we are now (checking dimensions)

(A)



(each FEB hosts 1 Alcor64)

1 RDO + 4 FEBs



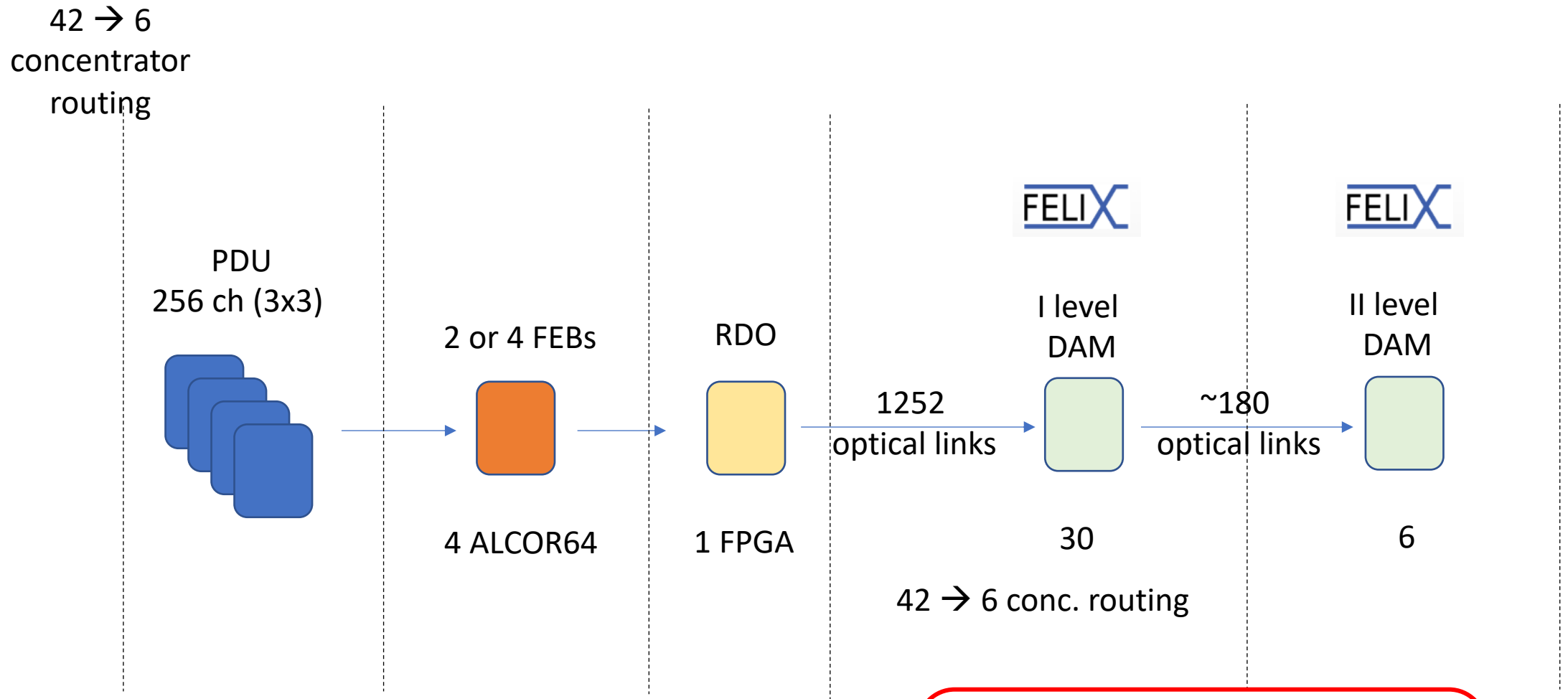
(B)

(each FEB hosts 2 Alcor64)

1 RDO and 2 FEBs

- RDO in the middle of FEB increases area! We desperately need area. In this way RDO is 4 x 9 cm
- Likely option (A) preferred (→ 1 FEB = 1 ALCOR64)
- The dRICH electronic - burger :

Where we are now (checking dimensions…)



600 k$

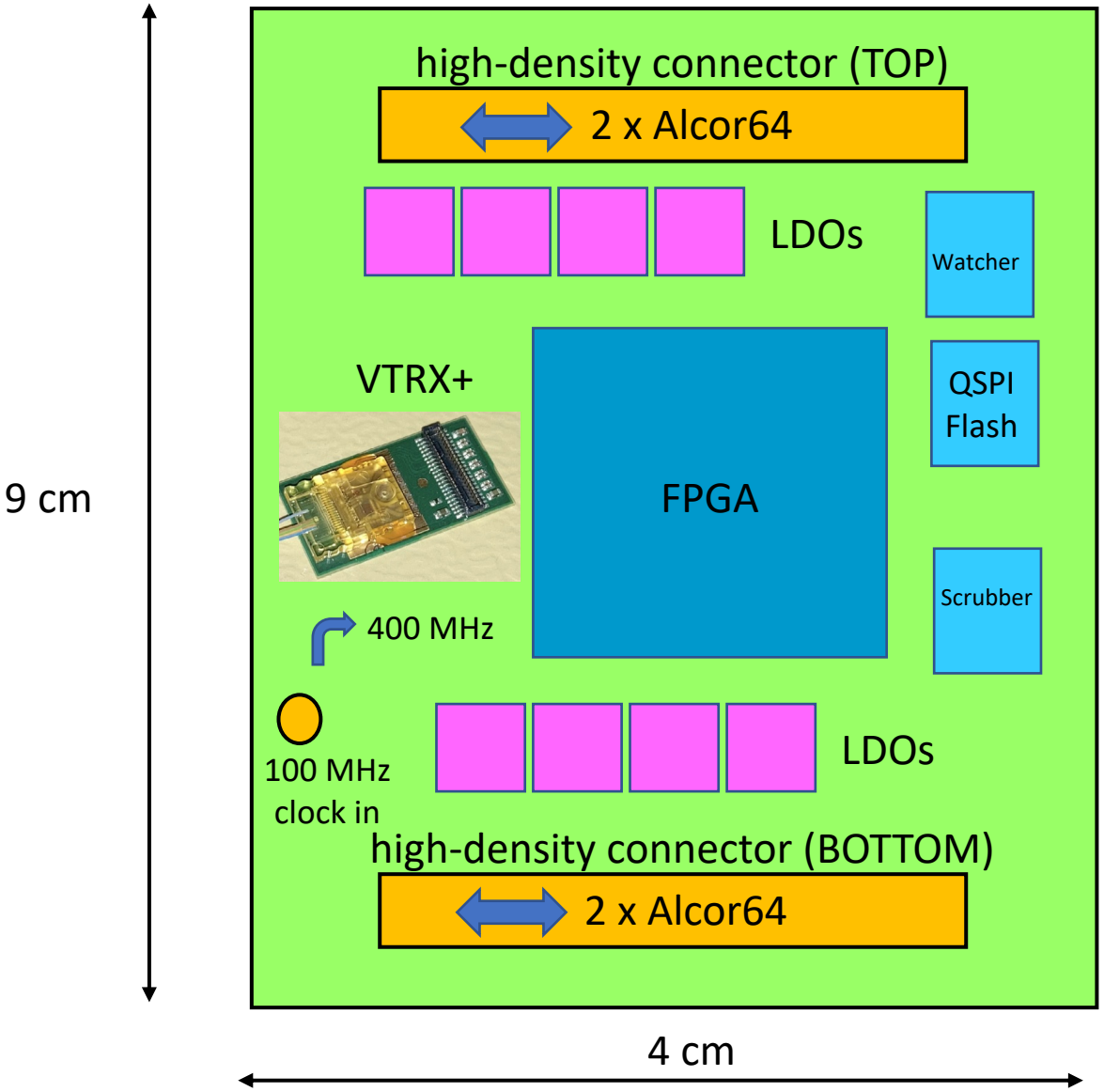
These numbers are not the “standard” one declared so far, wait 5th July for official dRICH statements

Why?

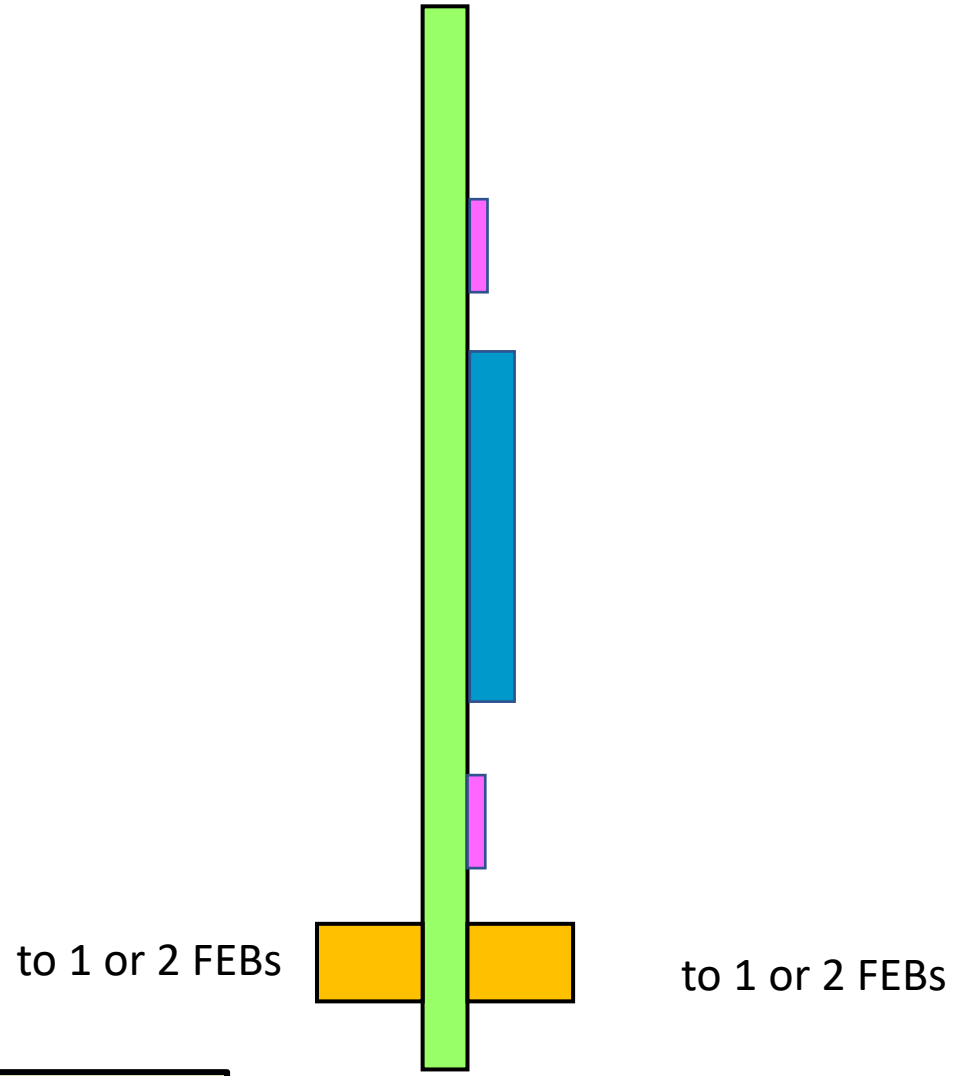
- We get rid of any hardware development for intermediate DAM (“more firmware, less hardware” approach)
- Space is a big challenge!
- Cost → to be done full assessment, but scenario with 312 links is not for free (and it entails, however 6-7 DAMs, 312 FPGA medium size, etc.) → Cost of fibres info would be useful for us in this phase to make properly this assessment
- PDU very modular
- Less power consumption inside readout box
- We add cables, materials inside readout box

What to put on such RDO?

front view



side view



not on scale !!!

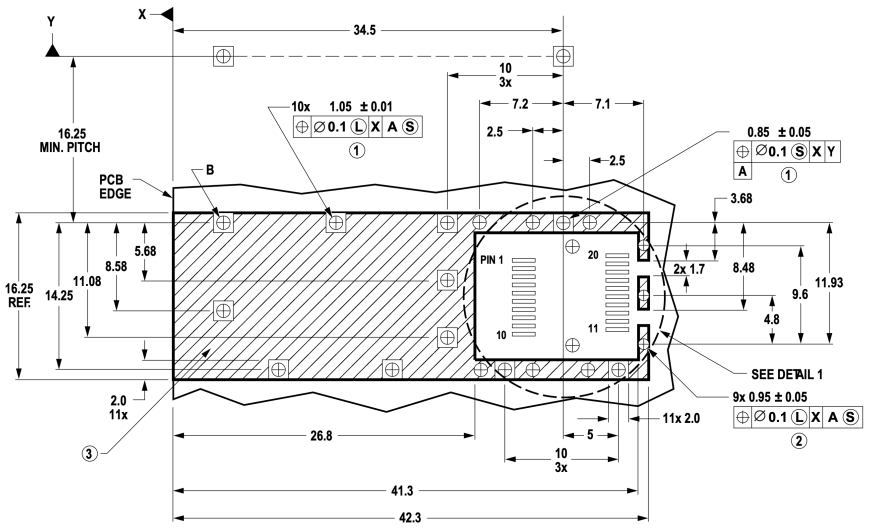
Specifications (to be worked out/discussed!)

A lot of work in progress toward defining specifications (LV, connectors, bus vs ALCOR64, services, etc.)

- **FPGA**: we are targeting Artix Ultrascale+ or PolarFire. There are pros/cons to be explored. Xilinx generally better on performance (including on link data out) and development tools. PolarFire likely better on rad tol. Not for today discussion. [Interesting news from Alex today!!!]
- Bologna will have soon a "development board" with PolarFire (ALICE/TRM2 project + ALICE3/SiPM readout)

- **OPTICAL TRANSCEIVER**:

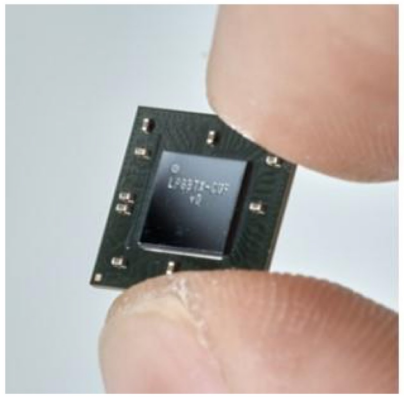
Commercial choice (just an example up to 14.025 Gb/s)

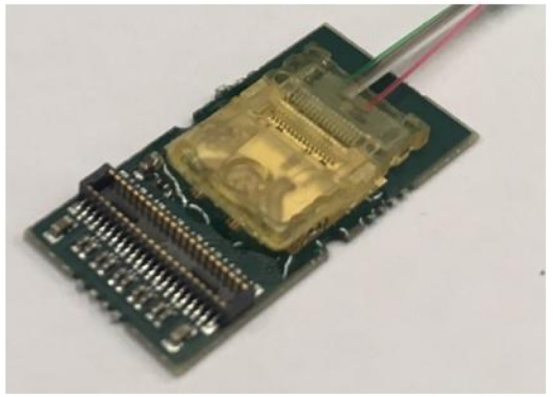


Example of commercial choice: 4.23 x 1.62 cm!

Optical transceiver: VTRX+

- **lpGBT and Versatile link +**
  - https://ep-ese.web.cern.ch/project/lpgbt-and-versatile-link
  - lpGBT
  - VTRX+
- **produced for LS3/Run4**
- **no iteration after that for mass production is planned (for now)**
  - performance assumed to be good for LS4/Run5
  - if this is not correct → we need to speak up now
  - future development effort goes to EP-RD WP6



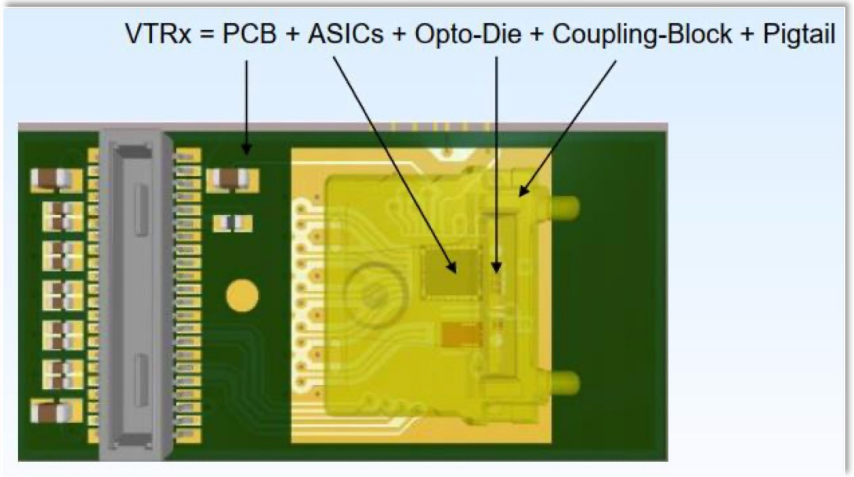


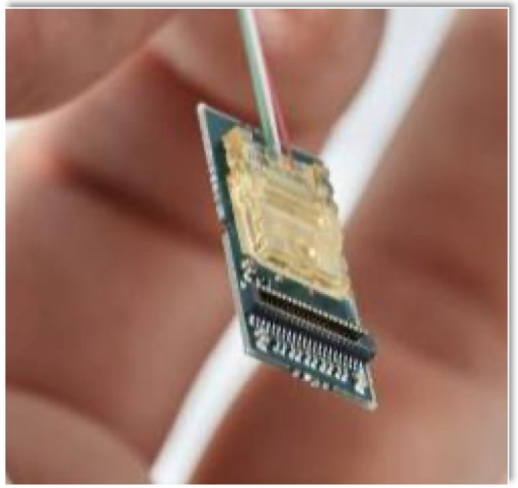
Slide from A. Kluge, ALICE Electronics coordinator

Note lpGBT not an option for EIC, but VTRX+ is a miniaturized opt. tranceiver (rad hard) that might be interesting

VTRx+ Front-end Module

- **Versatile**
  - Up to 4 Tx + 1 Rx, configurable by masking channels
- **Miniaturised**
  - 20 x 10 x 2.5 mm
- **Pluggable**
  - Electrical connector
- **Data-rate**
  - Tx: up to 4×10 Gb/s, Rx: 2.5 Gb/s
- **Environment**
  - Temperature: -35 to + 60 °C
  - Total Dose: 100 Mrad
  - Total Fluence: 1x10^{15} n/cm^2 and 1x10^{15} hadrons/cm^2
- **Status**
  - Pre-production ongoing
  - Solving problems with module assembly
  - Alignment of optical components
  - Ramping up to 2k modules/month in 2023





A. Kluge EP-ESE 10 May. 2023 6

Slide from A. Kluge, ALICE Electronics coordinator

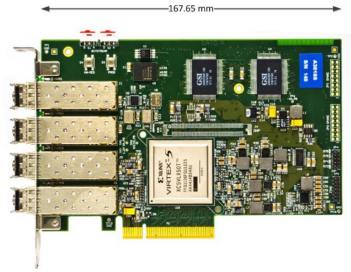
- **quantity and commitment to buy needs to be settled by end of 2023**

as components need to be purchased

Building a plan

dRICH World

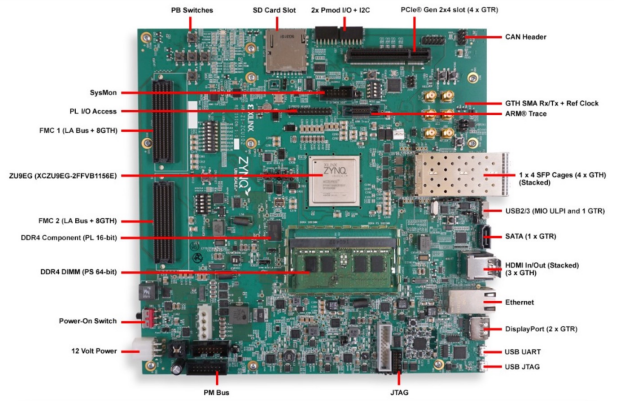
- define FEB-RDO specs!!! → by December 2023 at the latest worked out internally dRICH
- Production RDO + breakout-boards
- @test-beam 2024: read 8 PDU using CONET IPCORE and 2 PCIe CARD A3818 from CAEN (all hardware + know-how available from ALICE
- Some radiation tests of key component @TIFPA planned for 2024



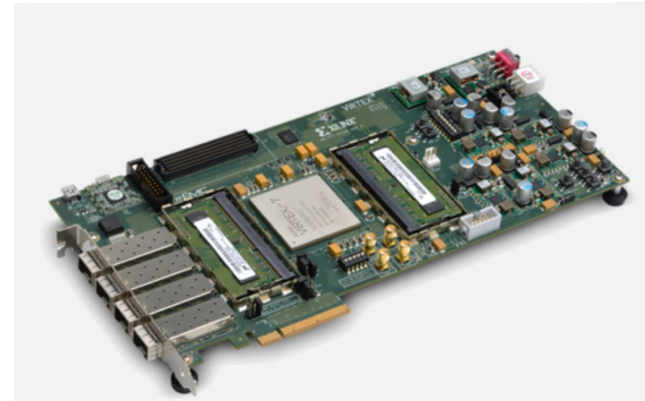
ePIC World

- Test/Development of ePIC DAQ link on a pair of Zynq ZCU102 (1 available, 1 from project)

  Davide/Pietro part of a small sub-DAQ WG to define specs of DAQ link
  These cards will be used to define specs. We might play already with RDO when existing (clock transmission etc).



- No FELIX available from ATLAS/BO: buy a VC709 as main “FELIX” development platform?
  → 9000 EU
  → ATLAS provide FW for VC709 operating it as a “mini-FELIX”



→ we need to collect more information about FELIX….

Backup

First FPGA candidate: Xilinx Artix Ultrascale+ family

	AU7P	AU10P	AU15P	AU20P	AU25P
System Logic Cells	81,900	96,250	170,100	238,437	308,437
CLB Flip-Flops	74,880	88,000	155,520	218,000	282,000
CLB LUTs	37,440	44,000	77,760	109,000	141,000
Max. Distributed RAM (Mb)	1.1	1.0	2.5	3.2	4.7
Block RAM Blocks	108	100	144	200	300
Block RAM (Mb)	3.8	3.5	5.1	7.0	10.5
UltraRAM Blocks	–	–	–	–	–
UltraRAM (Mb)	–	–	–	–	–
CMTs (1 MMCM and 2 PLLs)	2	3	3	3	4
Max. HP I/O(1)	104	156	156	156	208
Max. HD I/O(2)	144	72	72	72	96
DSP Slices	216	400	576	900	1,200
System Monitor	1	1	1	1	1
GTH Transceiver(3)	4	12	12	–	–

Package (1)(2)(3)	Package Dimensions (mm)	AU7P	AU10P	AU15P	AU20P	AU25P
		HD I/O, HP I/O, GTH, GTY				
UBVA292	10.5x8.5	72, 58, 4, 0				
UBVA368	11.5x9.5		24, 104, 8, 0	24, 104, 8, 0		
SBVB484	19x19		48, 156, 12, 0	48, 156, 12, 0		
SBVC484	19x19	144, 104, 4, 0				
SFVB784	23x23				72, 156, 0, 12	96, 208, 0, 12
FFVB676	27x27		72, 156, 12, 0	72, 156, 12, 0	72, 156, 0, 12	72, 208, 0, 12

Xilinx Artix Ultrascale+ family

VCCINT = 0.850 V
VCCAUX = 1.800 V
VCCO = 1.140 – 3.400 V for HD I/O banks
VCCO = 0.500 – 1.900 V for HP I/O banks

HP = High-performance I/O with support for I/O voltage from 1.0V to 1.8V.

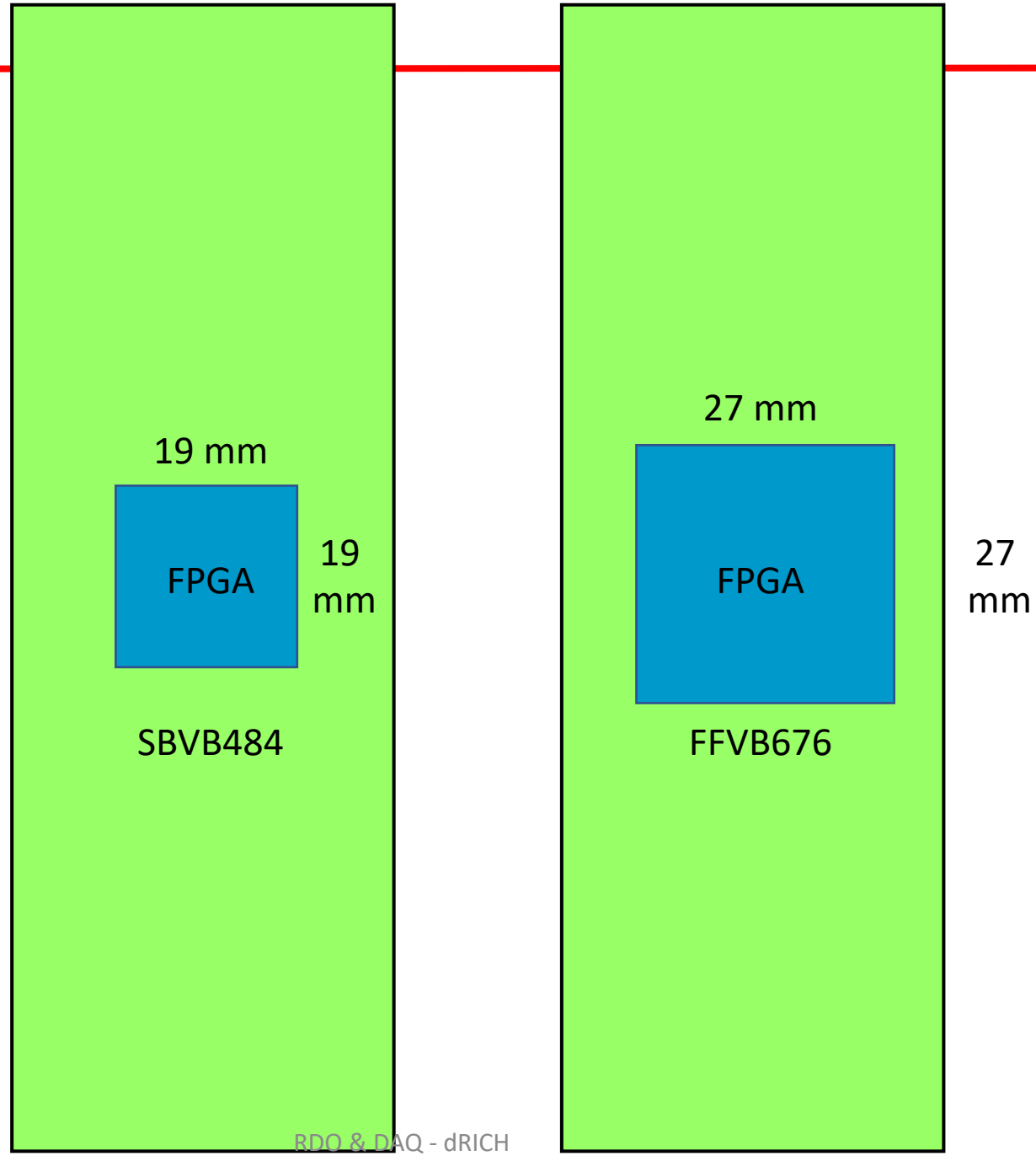
HD = High-density I/O with support for I/O voltage from 1.2V to 3.3V.

GTH and GTY transceiver line rates are package limited: SFVB784, SBVB484, UBVA368, and UBVA292 to 12.5Gb/s

LVDS DC specifications (**HP** I/O banks)

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO} [1]	Supply voltage		1.710	1.800	1.890	V
V_{ODIFF} [2]	Differential output voltage: $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	247	350	454	mV
V_{OCM} [2]	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF} [3]	Differential input voltage: $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High		100	350	600 [3]	mV
V_{ICM_DC} [4]	Input common-mode voltage (DC coupling)		0.300	1.200	1.425	V

On-scale drawings (scale factor = 1.5)



Choosing a Xilinx Artix Ultrascale+ requires both:

- a QSPI Flash
- a Microchip FPGA performing scrubbing

Second FPGA candidate: Microchip Polarfire family

	MPF050	MPF100	MPF200	MPF300	MPF500
Logic Elements (4LUT + DFF)	48K	109K	192K	300K	481K
Math Blocks (18 × 18 MACC)	150	336	588	924	1480
LSRAM Blocks (20 Kb)	160	352	616)	952	1520
uSRAM Blocks (64 × 12)	450	1008	1764	2772	4440
Total RAM (Mb)	3.6	7.6	13.3	20.6	33
uPROM (Kb)	216	297	297	459	513
User DLLs/PLLs	8	8 each	8 each	8 each	8 each
250 Mbps–12.7 Gbps Transceiver Lanes	4	8	16	16	24
PCIe® Gen 2 Endpoints/Root Ports	2	2	2	2	2
Total User I/O	176	296	364	512	584

Microchip Polarfire packages

VCCINT = 1.0 V

HSIO DC IO supply:
1.2V, 1.35V, 1.5V, 1.8V

GPIO DC IO supply: 1.2V, 1.5V, 1.8V, 2.5V, 3.3V

	MPF050	MPF100	MPF200	MPF300	MPF500
Type/Size/Pitch	Total User I/O (HSIO/GPIO) GPIO CDRs/XCVRs				
FCSG325 (11 × 11, 11 × 14.5 0.5 mm)	164 (84/80) 6/4	170 (84/86) 8/4	170 (84/86) 8/4		
FCSG536 (16 × 16, 0.5 mm)			300 (120/180) 15/4	300 (120/180) 15/4	
FCVG484 (19 × 19, 0.8 mm)	176 (96/92) 7/4	284 (120/164) 14/4	284 (120/164)14/4	284 (120/164) 14/4	
FCG484 (23 × 23, 1.0 mm)		244 (96/148) 13/8	244 (96/148) 13/8	244 (96/148) 13/8	
FCG784 (29 × 29, 1.0 mm)			364 (132/232) 20/16	388 (156/232) 20/16	388 (156/232) 20/16
FCG1152 (35 × 35, 1.0 mm)				512 (276/236) 24/16	584 (324/260) 24/24

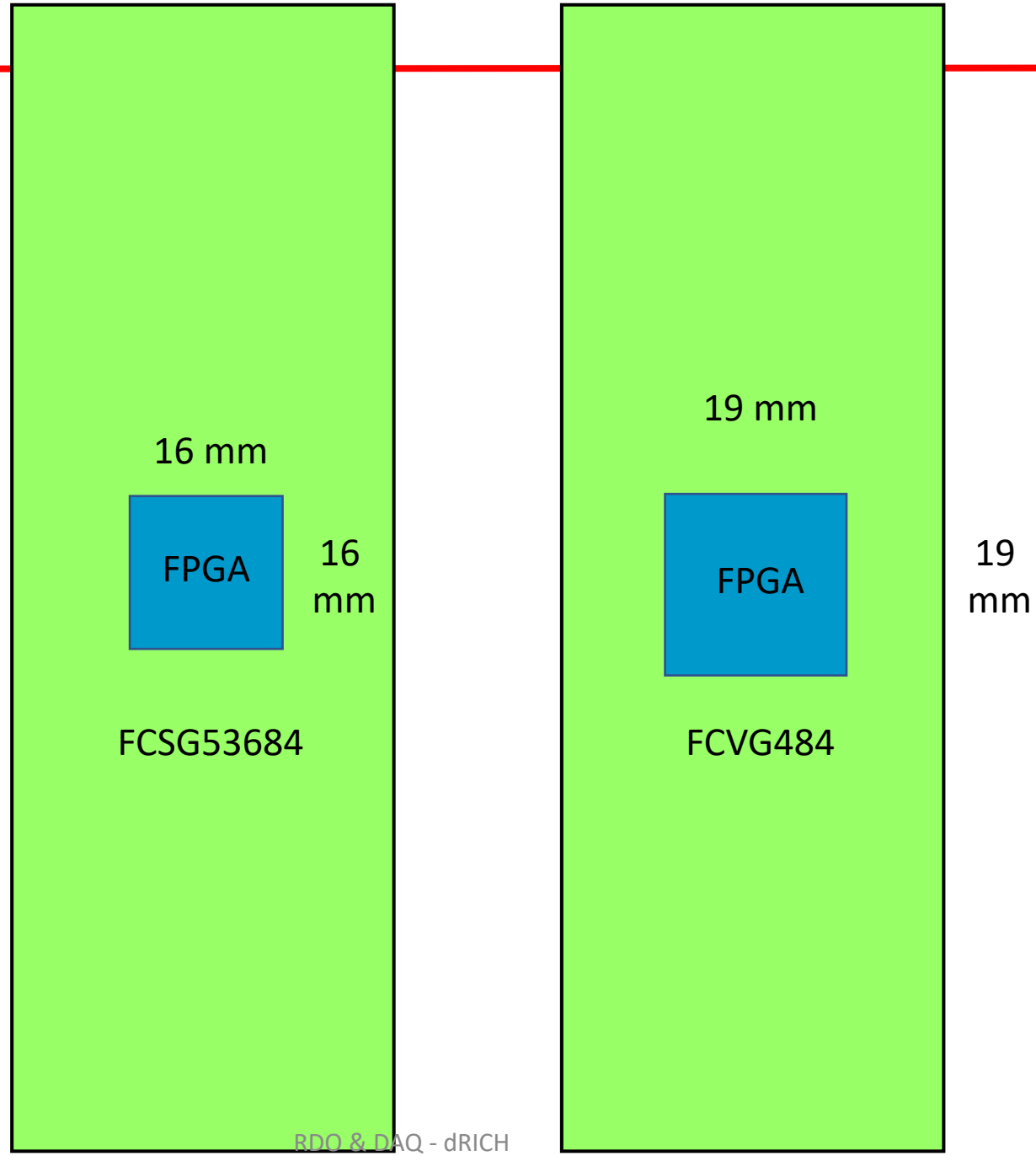
Differential DC input levels

I/O Standard	Bank Type	V_{ICM_RANGE} Libero Setting	V_{ICM} [1,3] Min (V)	V_{ICM} [1,3] Typ (V)	V_{ICM} [1,3] Max (V)	V_{ID} [2] Min (V)	V_{ID} Typ (V)	V_{ID} Max (V)
LVDS33	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS25 [7]	GPIO	Mid (default)	0.6	1.25	2.35	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18G[4]	GPIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6
LVDS18 [7]	HSIO	Mid (default)	0.6	1.25	1.65	0.1	0.35	0.6
		Low	0.05	0.4	0.8	0.1	0.35	0.6

Differential DC output levels

I/O Standard	Bank Type	V_{OCM} [1] Min (V)	V_{OCM} Typ (V)	V_{OCM} Max (V)	V_{OD} [2] Min (V)	V_{OD} [2] Typ (V)	V_{OD} [2] Max (V)
LVDS33	GPIO	1.125	1.2	1.375	0.25	0.35	0.45
LVDS25 [4]	GPIO	1.125	1.2	1.375	0.25	0.35	0.45
LVDS18G[4]	GPIO	1.125	1.2	1.375	0.25	0.35	0.45

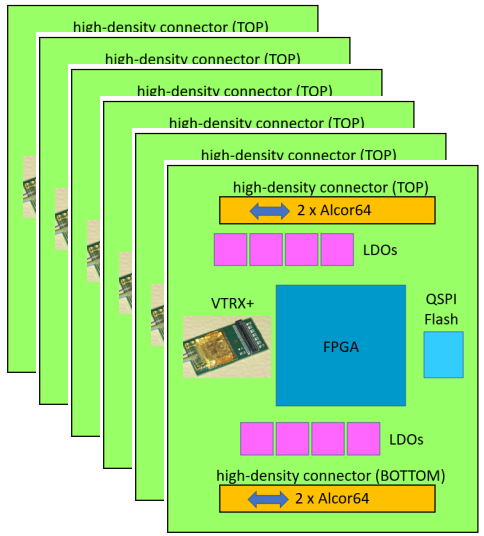
On-scale drawings (scale factor = 1.5)

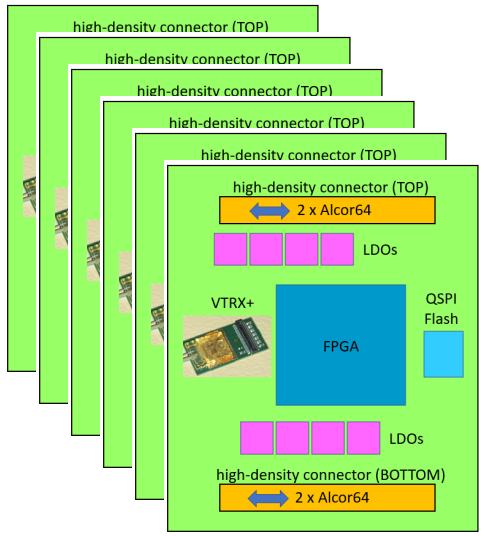


it would also allow to save on the QSPI Flash (not needed)

I level DAM: 42 to 6 concentrator/routing

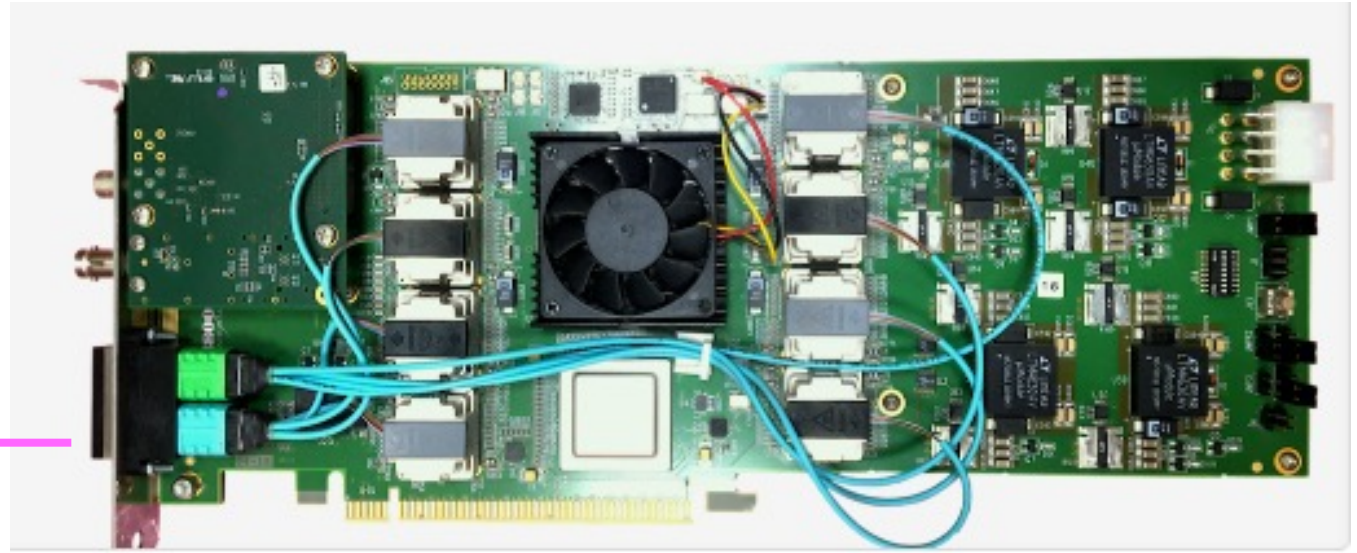
42 RDOs





42 optical links

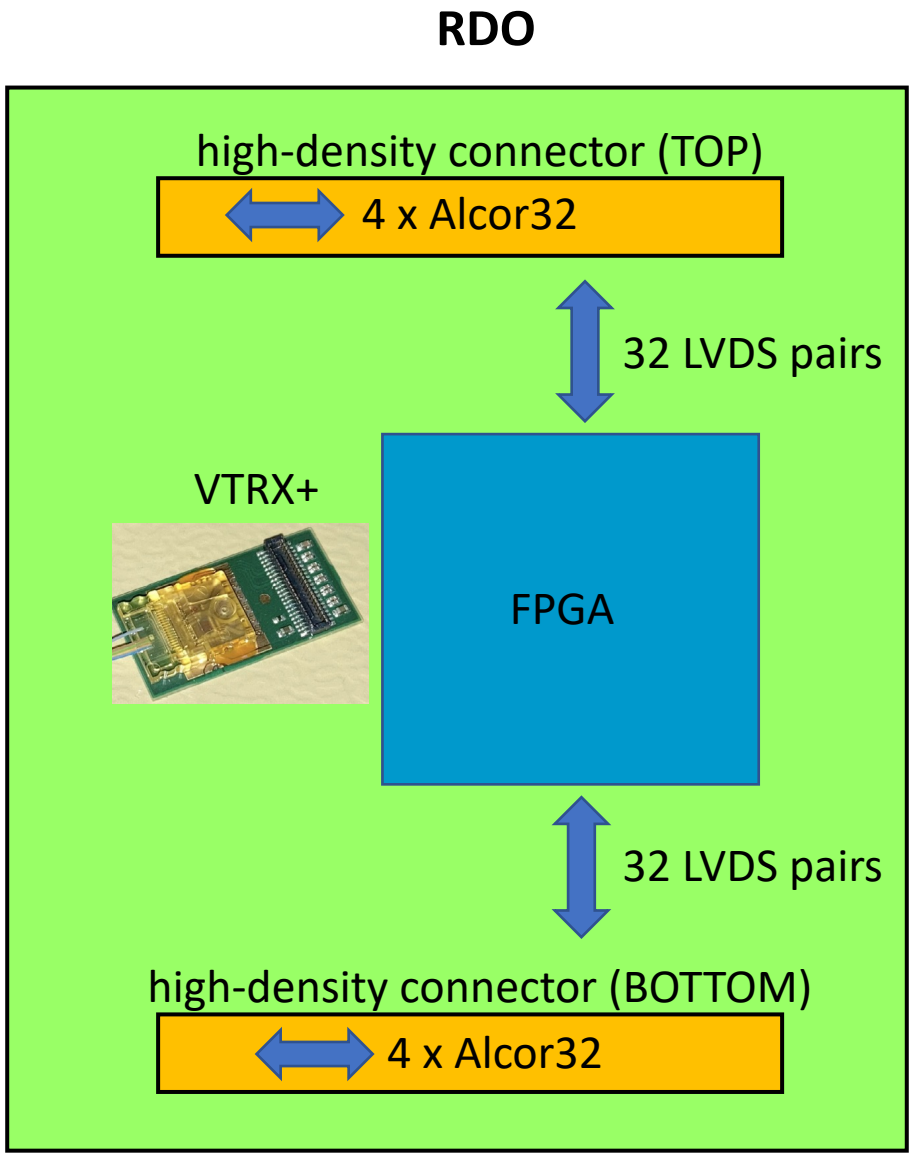
Felix board



6 optical links towards II level DAM

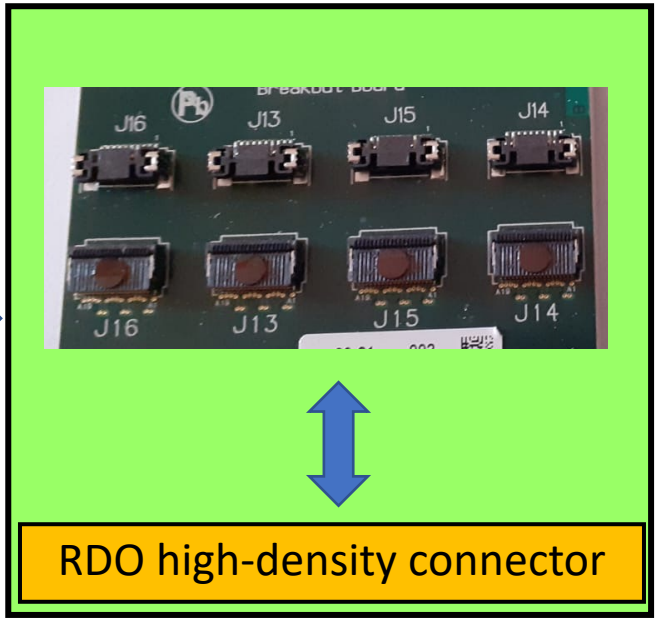
this solution requires modifications to the standard Felix firmware

Intermediate steps



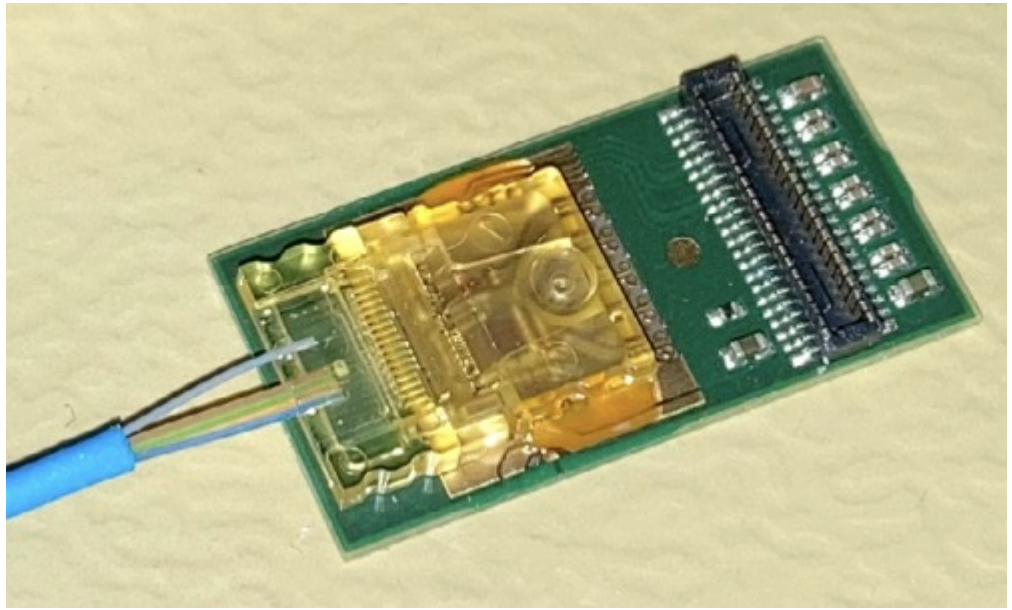
The plan is to use the RDO also to readout the Alcor32 chips: this requires the design of a new breakout board

old



new

VTRX+



VTRX+: 20 x 10 x 2.5 mm^3