ROC chips introduction

for EIC

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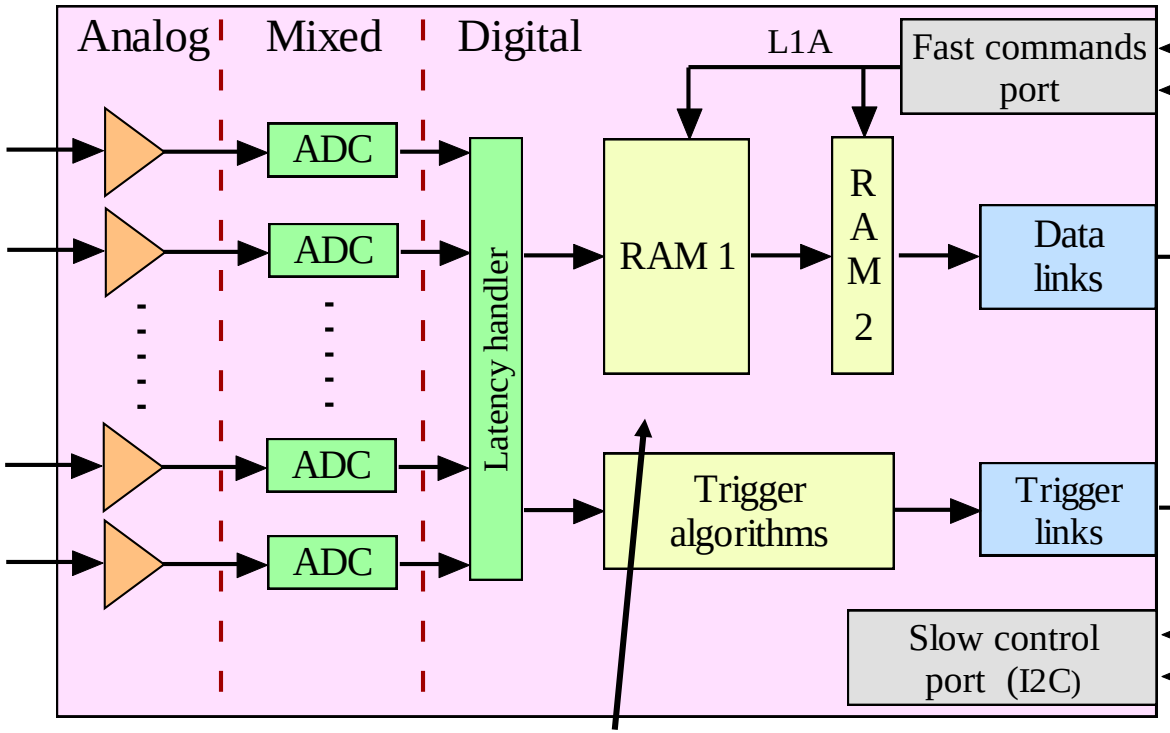
Organization for Micro-Electronics desiGn and Applications

ROC chips main structure

- HGCROC / H2GCROC (for SipM) and ALTIROC are LHC colored ASICs (external L1 trigger)
  - Below is an calorimetry structure (not pixel like ALTIROC or EICROC but interfaces are similar)



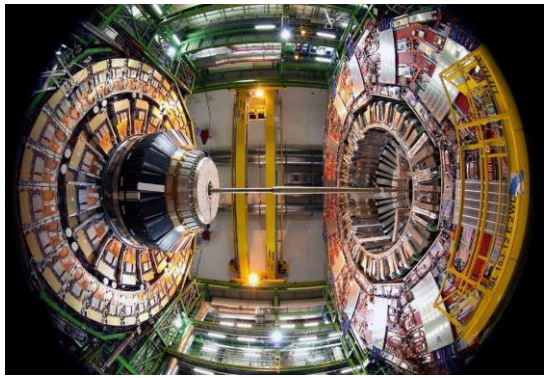
Dedicated fast command interface : calibration pulses, external trigger.

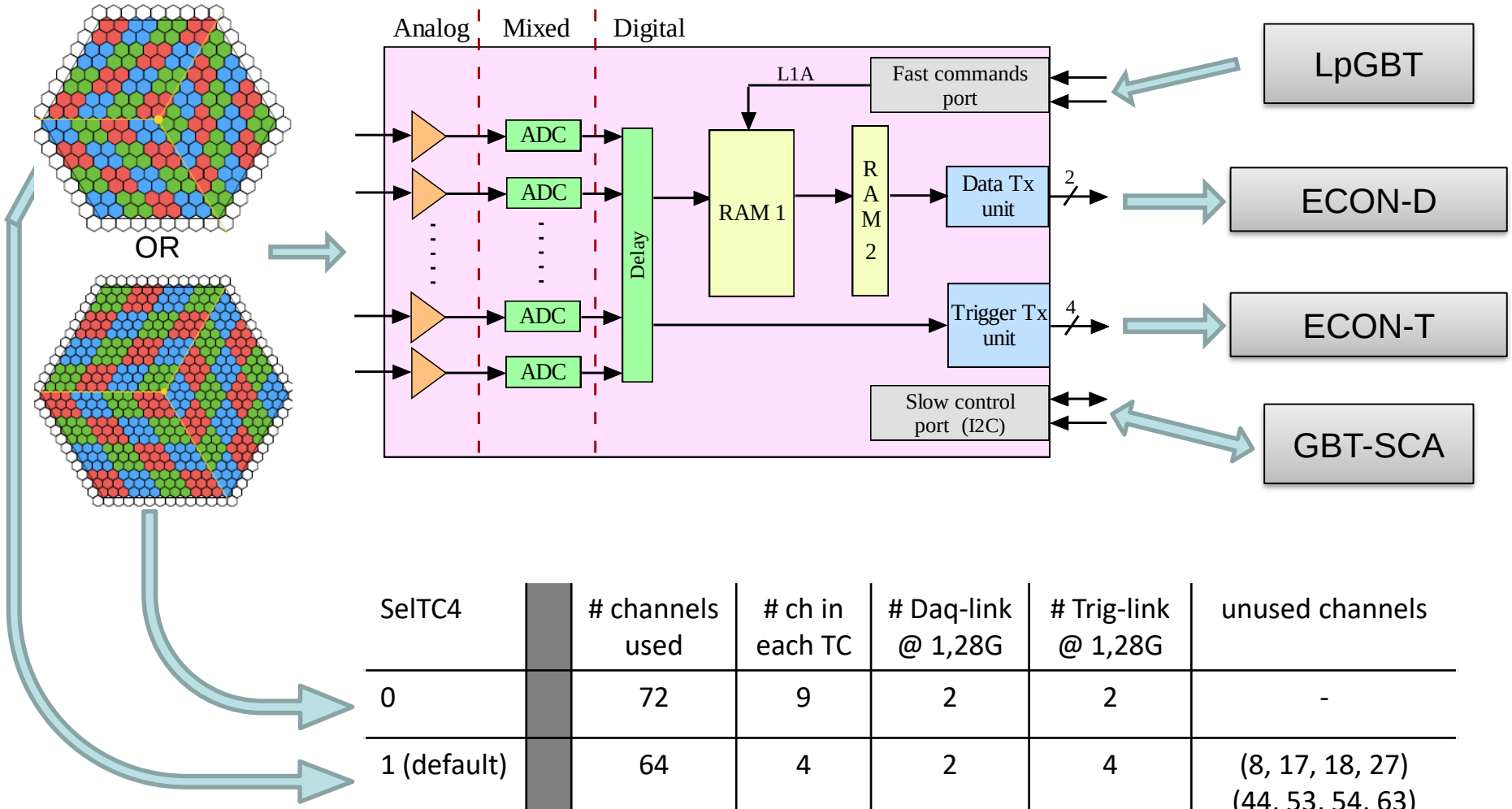
Data and trigger serial links with CLPS signaling (LpGBT @ 1,28 Gbps)

LHC-like structure :
Ram1 for data storage
Ram2 for L1 accepted events

I2C interface to load the ASIC parameters (slow control interface)

- **HGCROC integrates 72 channels to readout (+2 Calib, +4 CM):**
  - 192-ch sensor with a 64-ch configuration
  - 432-ch sensor with a 72-ch configuration





SelTC4		# channels used	# ch in each TC	# Daq-link @ 1,28G	# Trig-link @ 1,28G	unused channels
0		72	9	2	2	-
1 (default)		64	4	2	4	(8, 17, 18, 27) (44, 53, 54, 63)

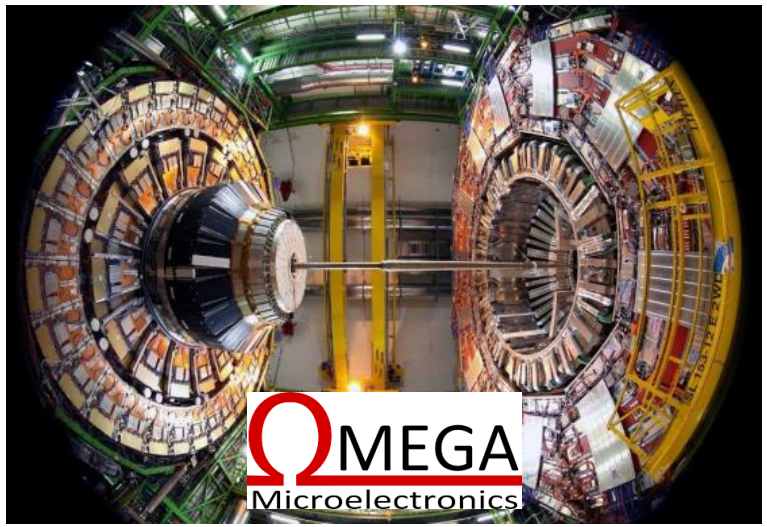
From HGCROC to HKROC (neutrino)

HGCROC for the endcap calorimeter – Phase II

6M of Silicon channels
(+ 240k of SiPM)

Radhard (200 Mrad)
Low Power (15 mW per chn)
Precise timing (25 ps)

Total of 150k ASICs needed
Pre-prod this year
Project started in **2017**



HKROC was developed in
6 months

Same ASIC structure (floorplan)
Same ADC and TDC
Same readout

New preamplifier
New digital processing

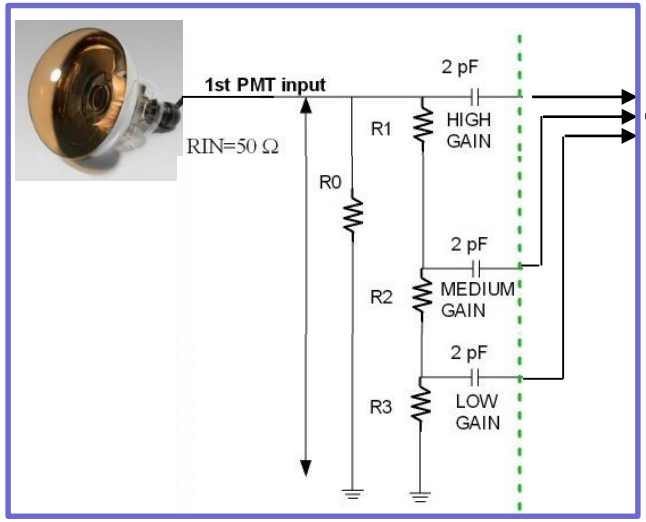
HEP trend => imaging calorimetry

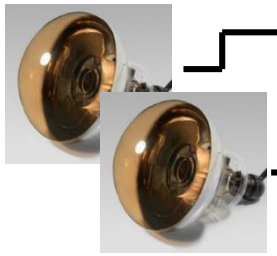
- ❑ High number of channels
- ❑ Charge and precise timing (<50 ps)
- ❑ Low power + System-On-Chip

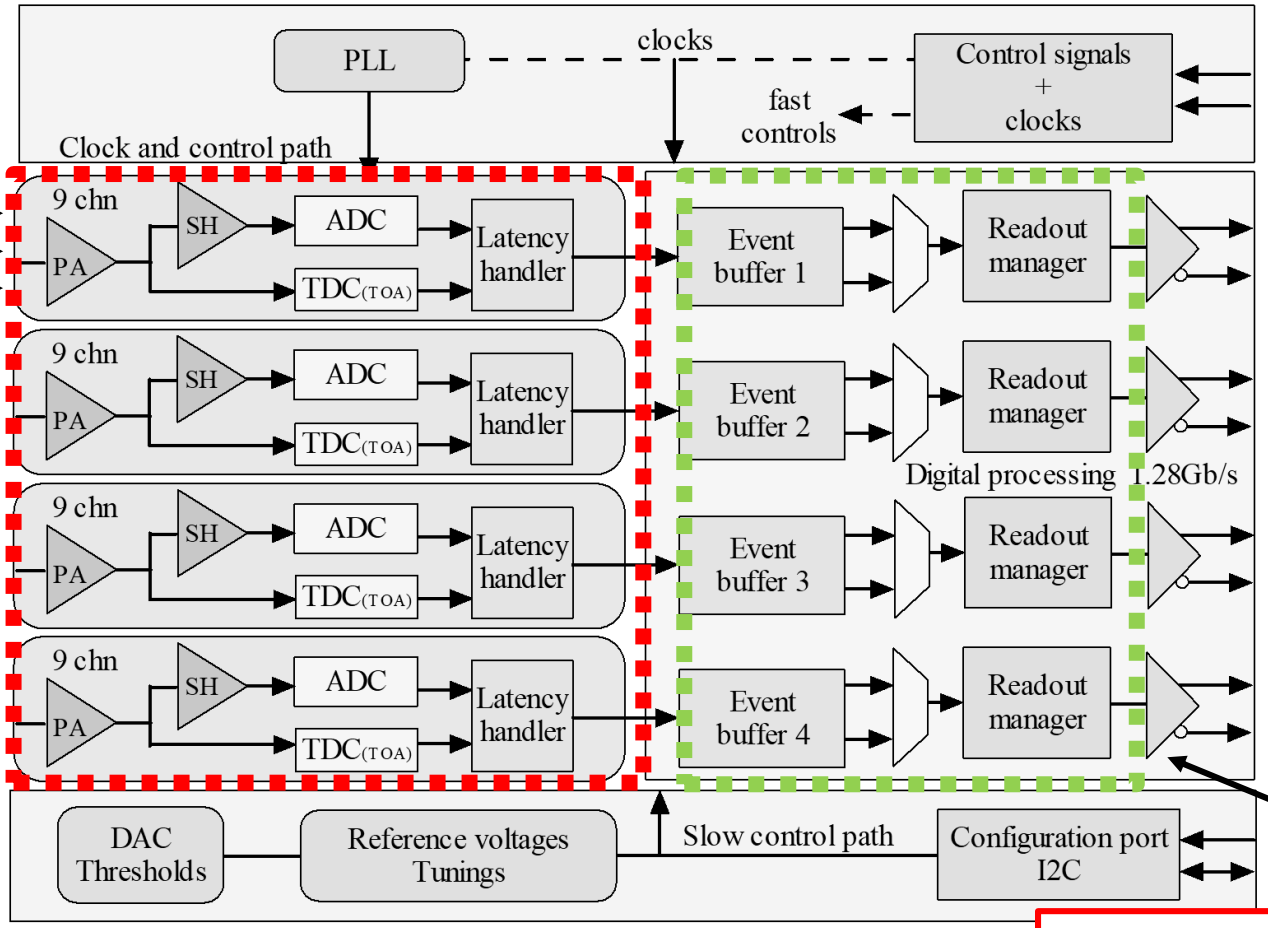
Based on HGCROC, HKROC-based electronics will provide a versatile, low-power and fully integrated solution for large neutrino experiments

From HGCROC to HKROC

- HKROC is 36 channels: 12 PMTs with High, Medium and Low gain
  - Charge (2500 pC) and time measurements (25 ps)







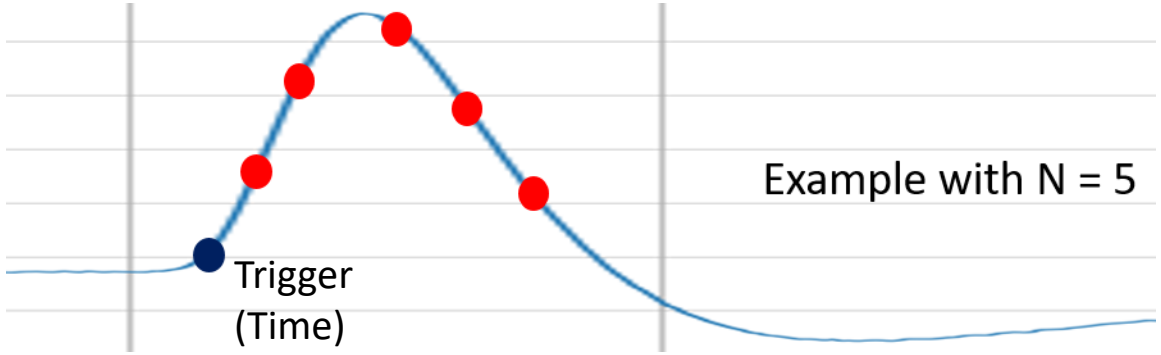
HGCROC front-end with almost no change

Experiment specific back-end

HKROC is a waveform digitizer with auto-trigger (half HGCROC)

HKROC: waveform digitizer with auto-trigger

- HKROC is waveform digitizer working @ 40 MHz
  - Number of charge sampling points from 1 to 7
  - Fast channel for precise timing (25 ps binning)
  - Charge reconstruction algorithm in FPGA



HKROC can accept consecutive events (separated by ~30 ns)

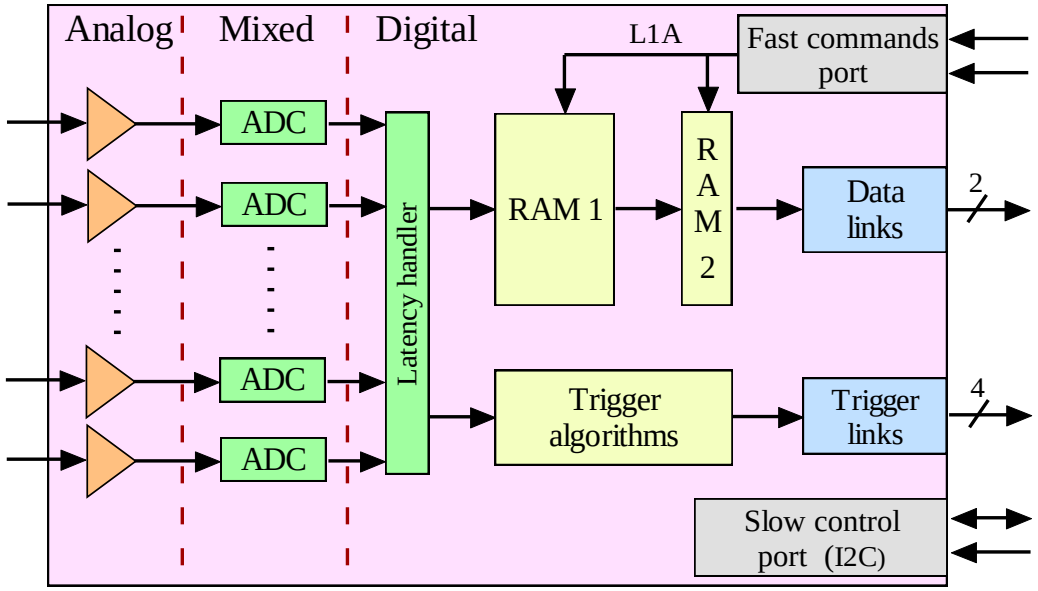
Internal HKROC memory writing is without dead time

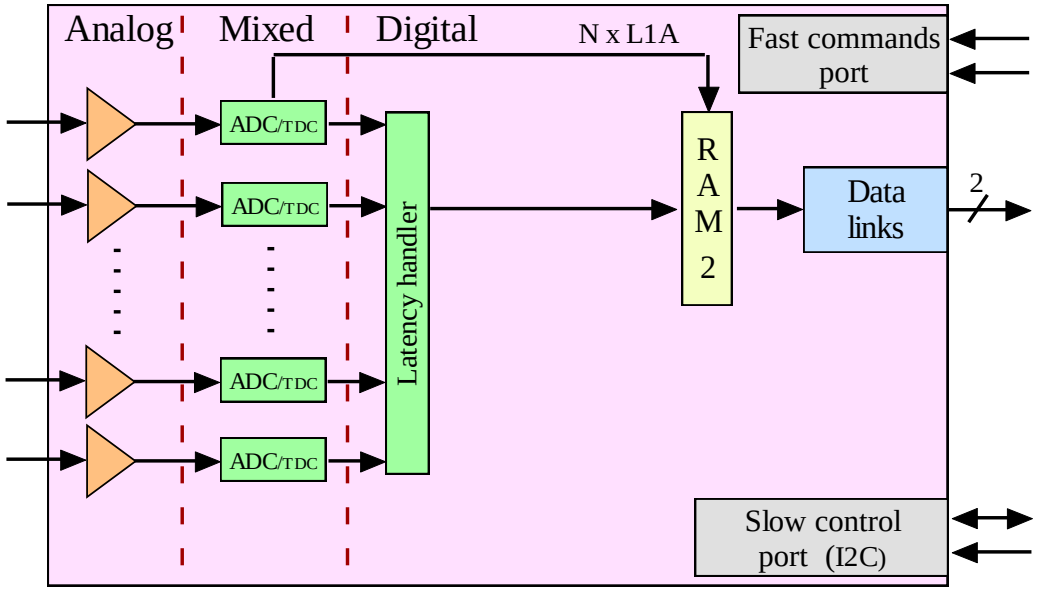
Readout speed is only limited by serial link bandwidth (average values above)

This auto-triggering scheme could be added to HGCROC-EIC
(same front-end, new back end)

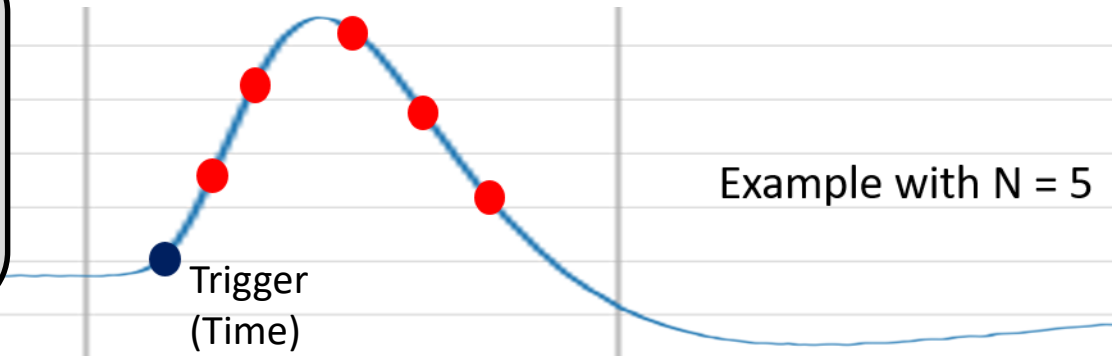
What HGCROC-EIC could look like

- HGCROC / H2GCROC (for SipM) with the integration of auto-triggering
  - Below is an calorimetry structure (not pixel like ALTIROC or EICROC but interfaces are similar)

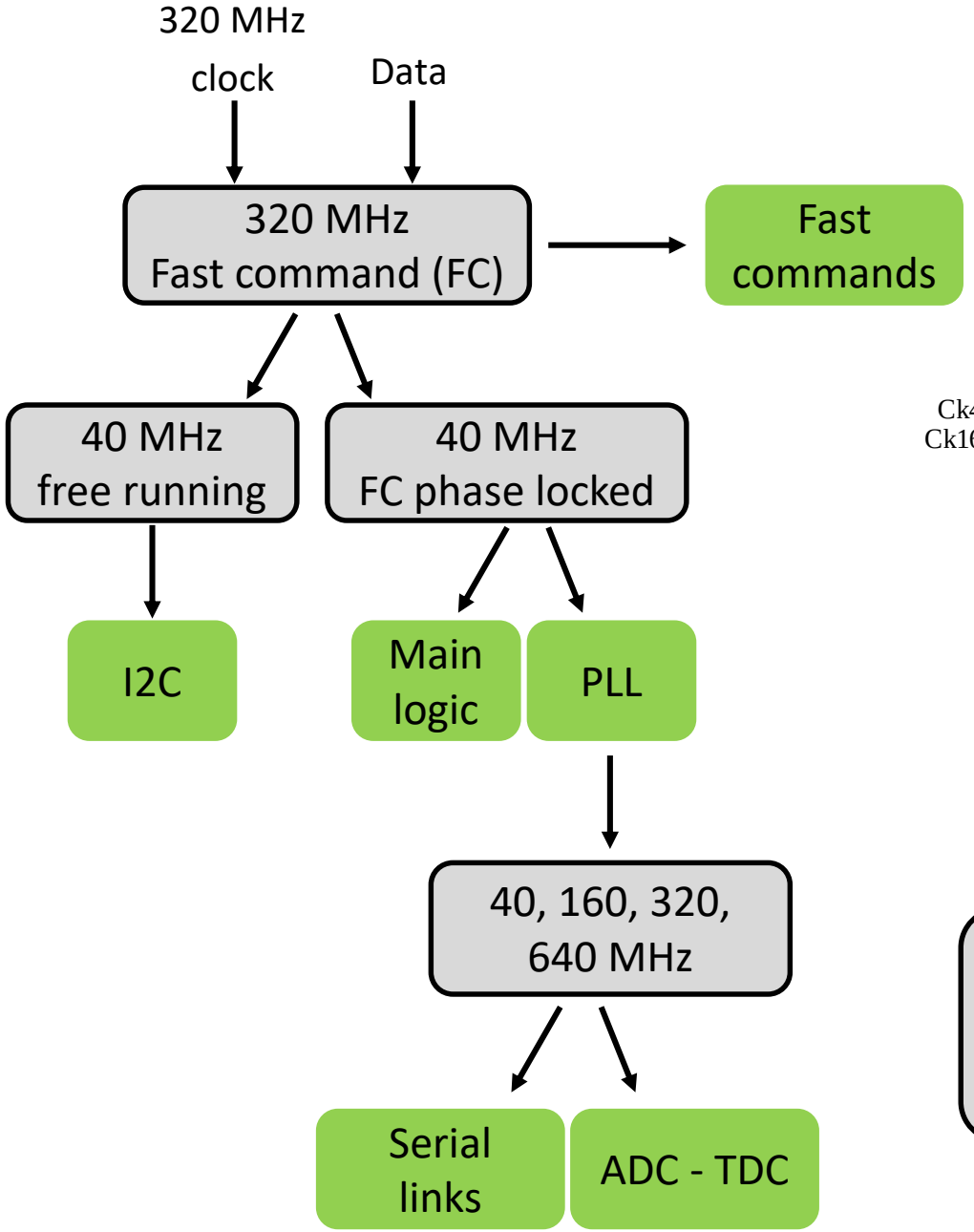


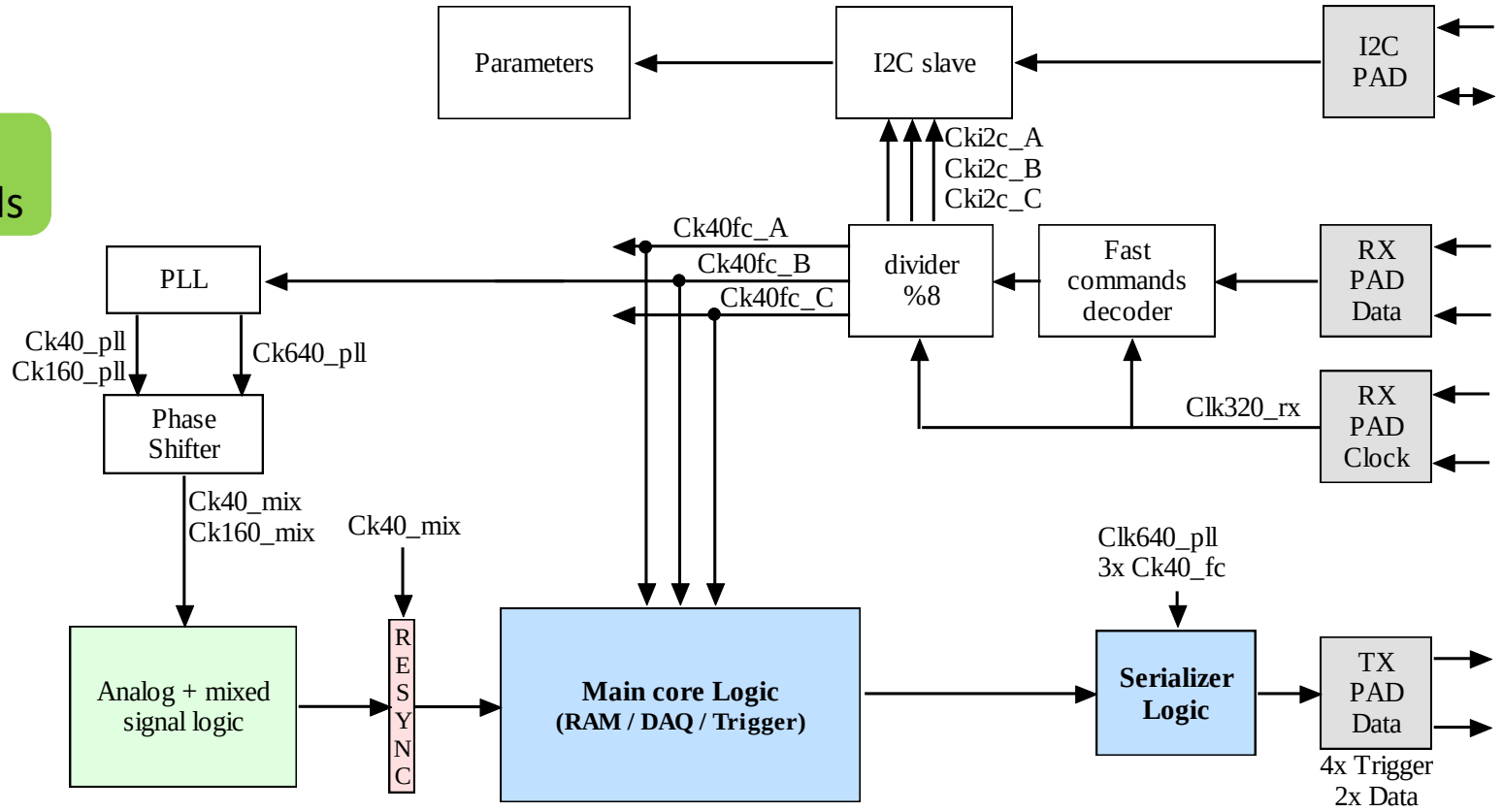


- Each event passing the threshold is readout
- Check Hit rate
- Auto-trigger with N “samples” (1 to 7)
  (Same as HKROC)



HGCROC/HKROC internal clocking scheme





Preferred clocking scheme (no change) - HGCROC-EIC

Propagate 320 MHz

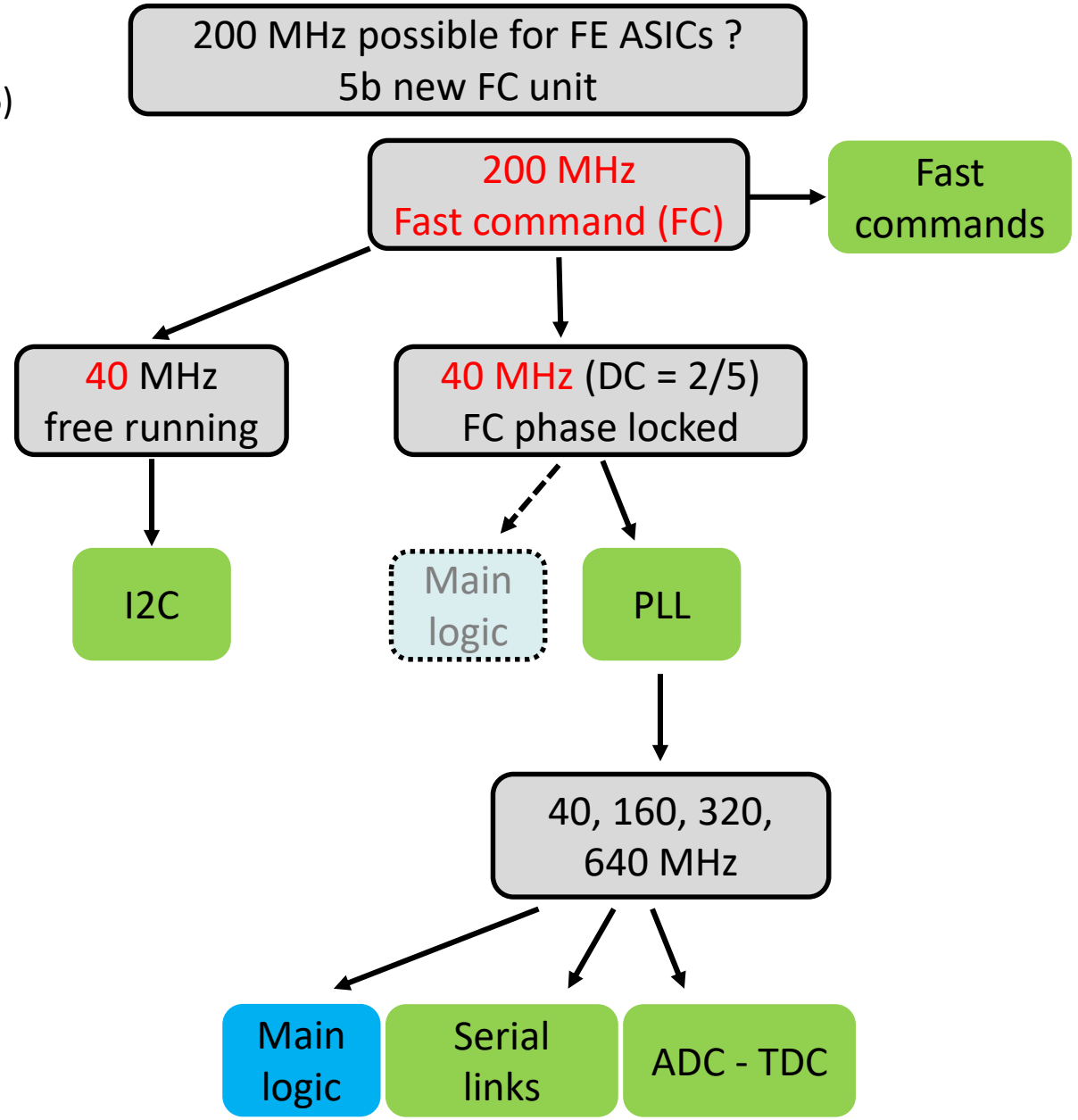
Same as HGCROC-HKROC-ALTIROC- (ECON)

From HGCROC/HKROC to EIC (alternatives with 200 M)

- Propagate a 200 MHz (twice EIC clock)
  - New fast command needed with less commands (32 instead of 256)
  - Able to recreate 40 M
  - Need to verify duty cycle impact but seems limited
  - Close from HGCROC – HKROC but only if needed

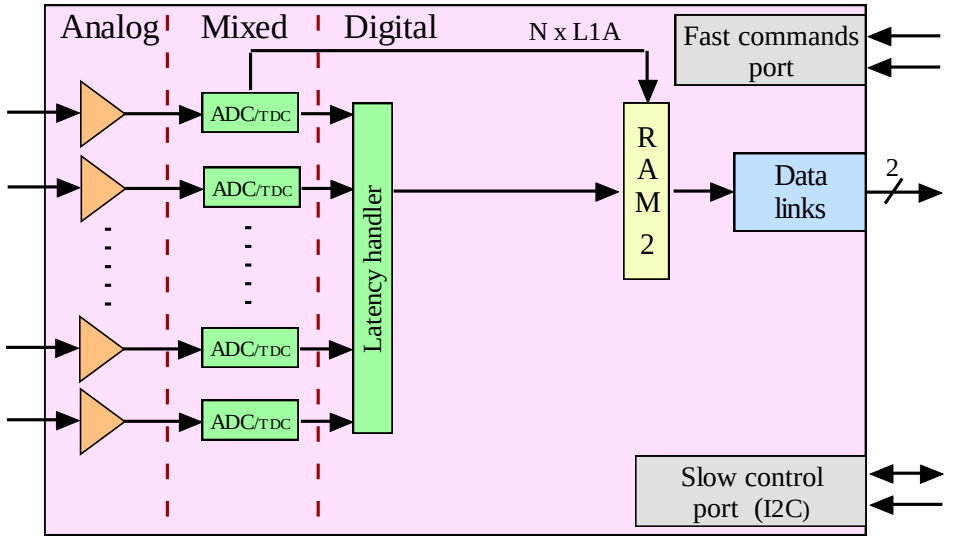
Fast commands	Description
Idle	Default, clock phase inside
External trigger	Pedestal measurement
Calibration Int	800 ns calib pulse
Calibration Ext	100 ns calib pulse
ChipSync	Fast digital reset
Link sync	idle pattern for 400 cycles
Counter reset	Init counters

Not 50 % duty cycle (pll input)



Conclusion

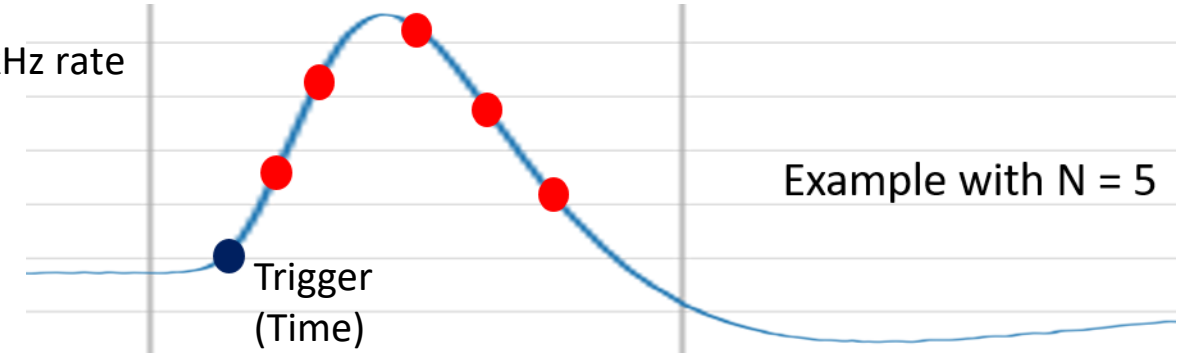
- HGCROC could be transformed to be auto-trigerred
  - Analog front-end + ADC/TDC remain the same



- ASIC internal clock should remain 40 MHz
  - Limited by ADC (and also the TDC)
  - Ideally keep the fast command unit (320 MHz + Data both differentials)

- Alternative with internal 40M clock coming with a 200 MHz

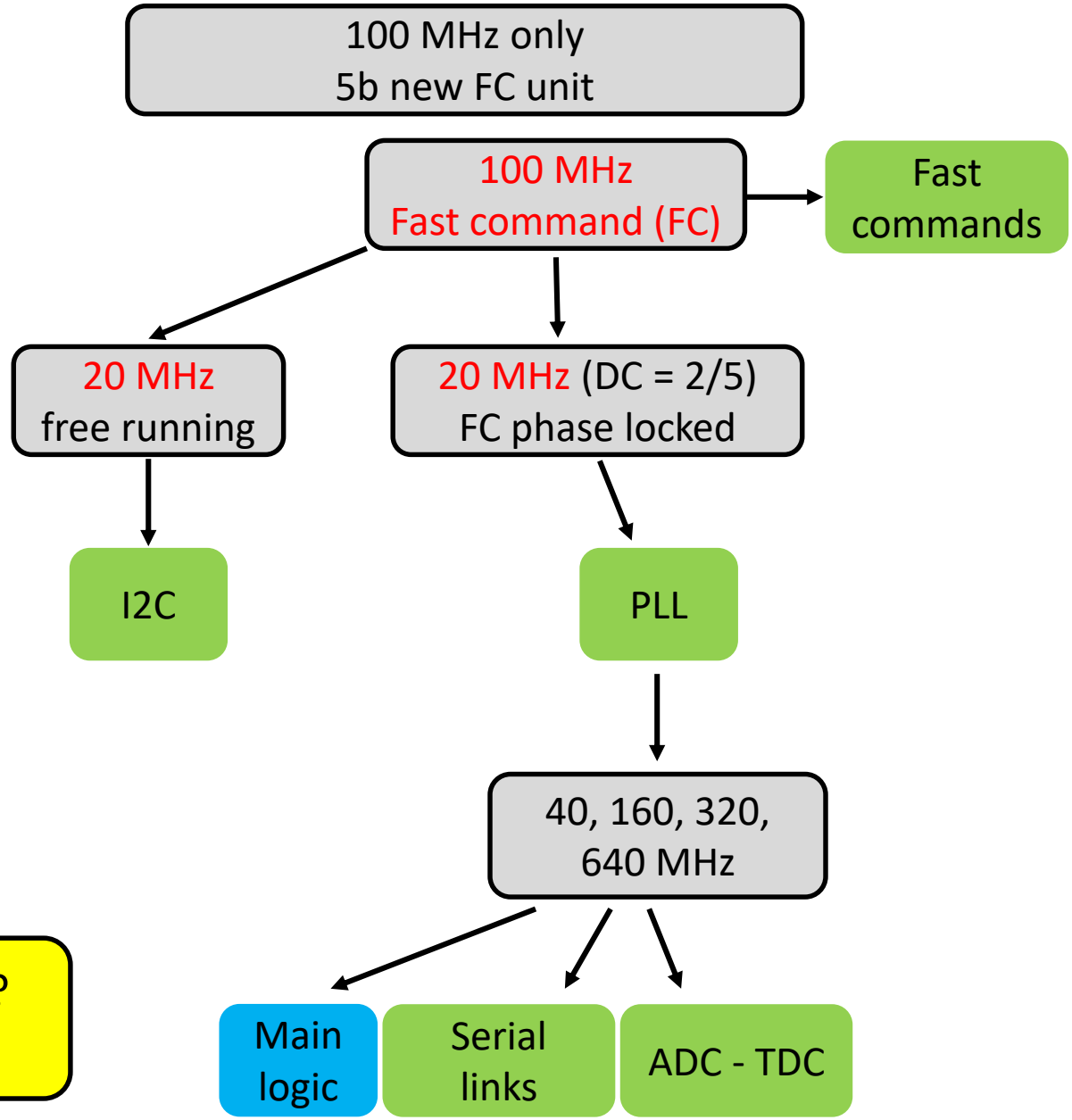
- Hit rate should be checked (1 signal above the threshold will output N (3 or 4) points
  - HKROC (N=3): 1 serial link @ 1,28Gps for 9 channels => max 100 kHz rate
  - Can be exercised with existing HGCROC and L1A



Backup

From HGCROC/HKROC to EIC (alternatives with 100 M)

- Propagate 100 MHz
  - Not able to recreate 40M
  - Not ideal



Command 256 -> 32 possibilities ?
Not 50 % duty cycle (pll input)

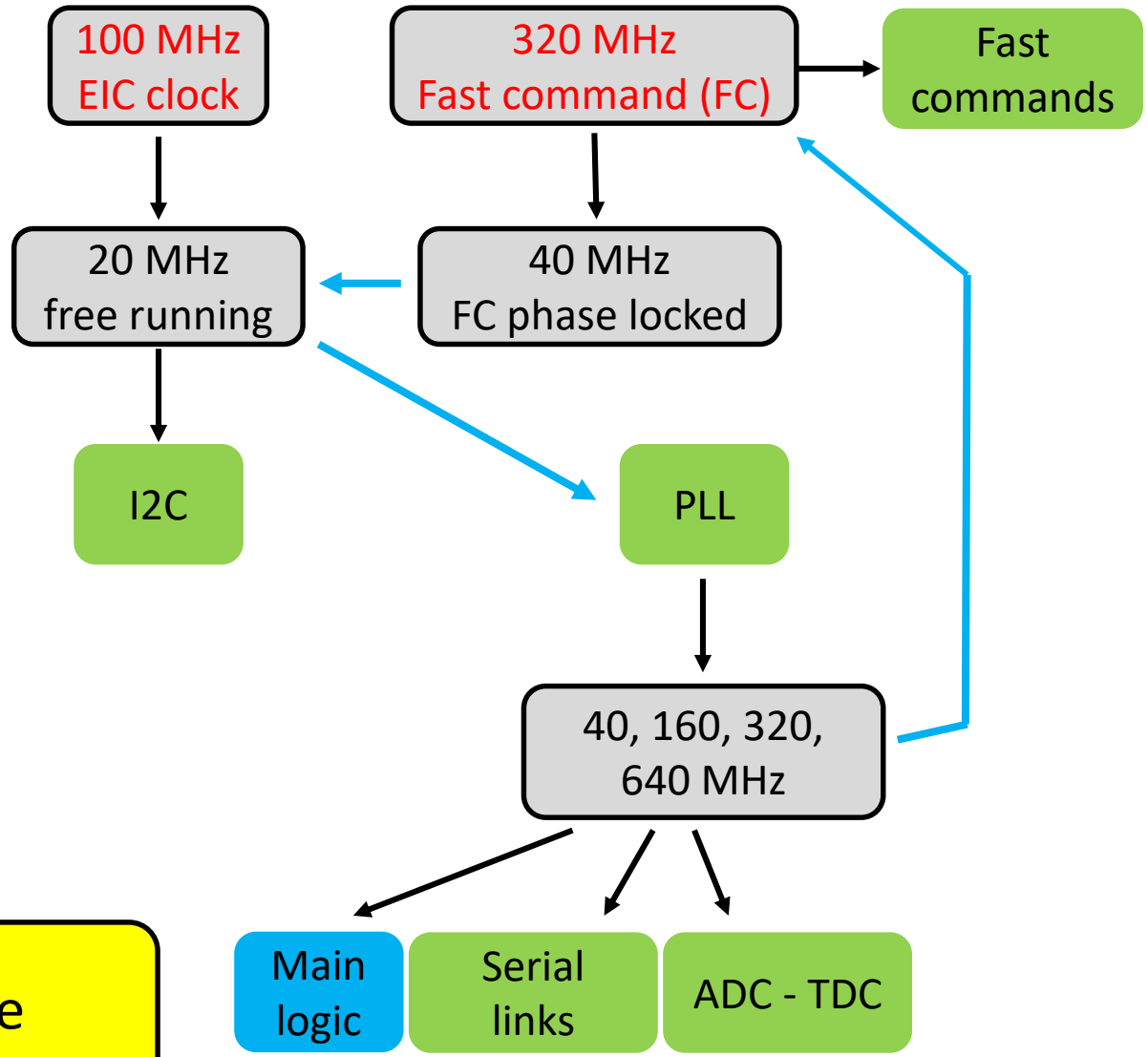
- Depending on the “hit rate”, we could move to an auto-triggered architecture (like HKROC)
  - I2C must remain independent of the PLL (to load the parameters during startup)
  - ADC is not able to go higher than 40 MHz ➔ need to remain the same

ADC max operating freq. is 40 M with all corners (tricky object)

I2C must be attached to a free running clock

Try to not change clock architecture

40 M phase is controlled



Clock loop ! Not usable

From HGCROC/HKROC to EIC (alternative with 40M)

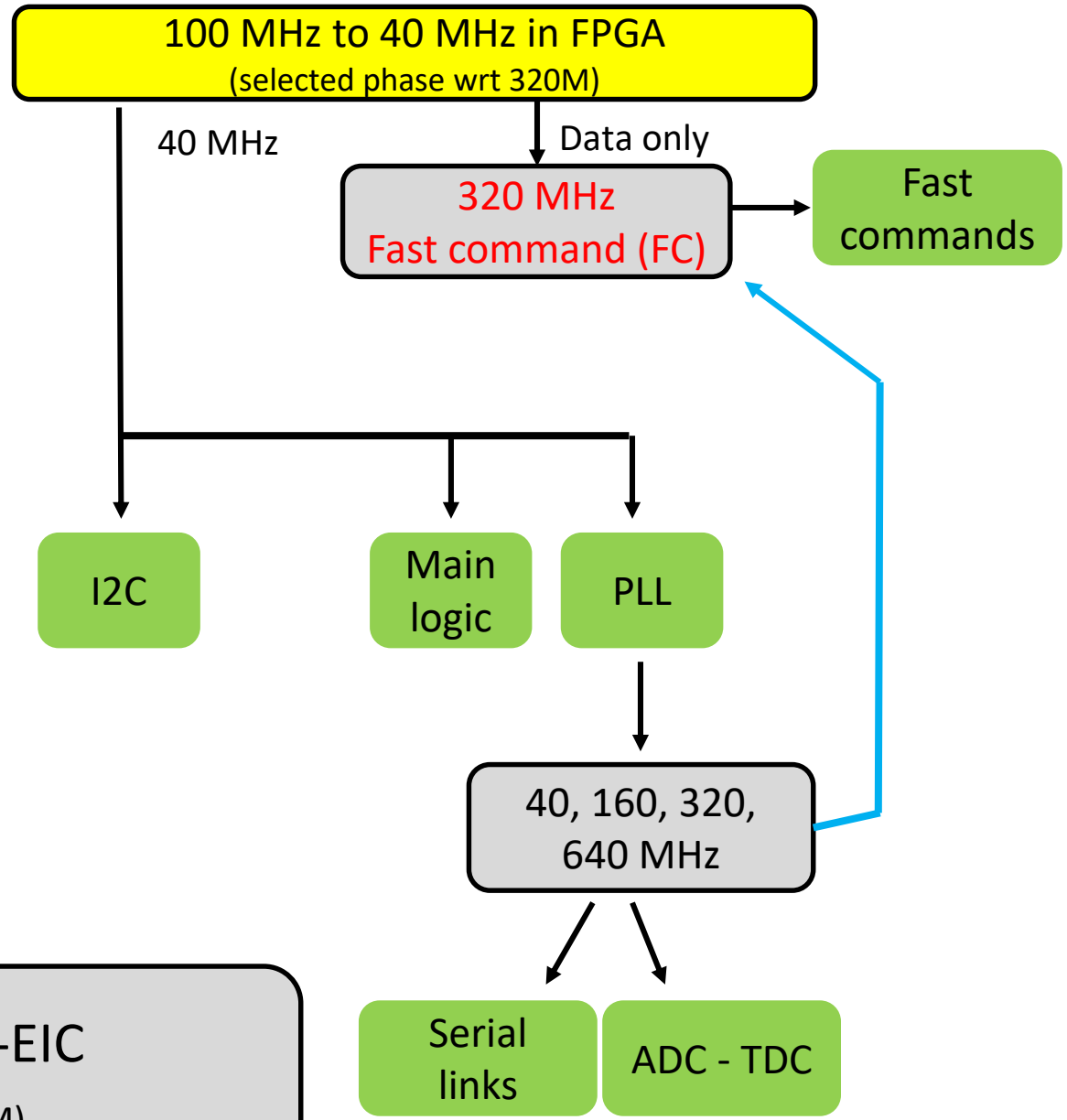
- Propagate 40 MHz instead of 320 Mhz
  - Need to wait the PLL to receive fast commands
  - Possible, not preferred due to the clock loop
  - Need to be aligned with the 40M of the ASIC

ADC max operating freq. is 40 M with all corners (tricky object)

I2C must be attached to a free running clock

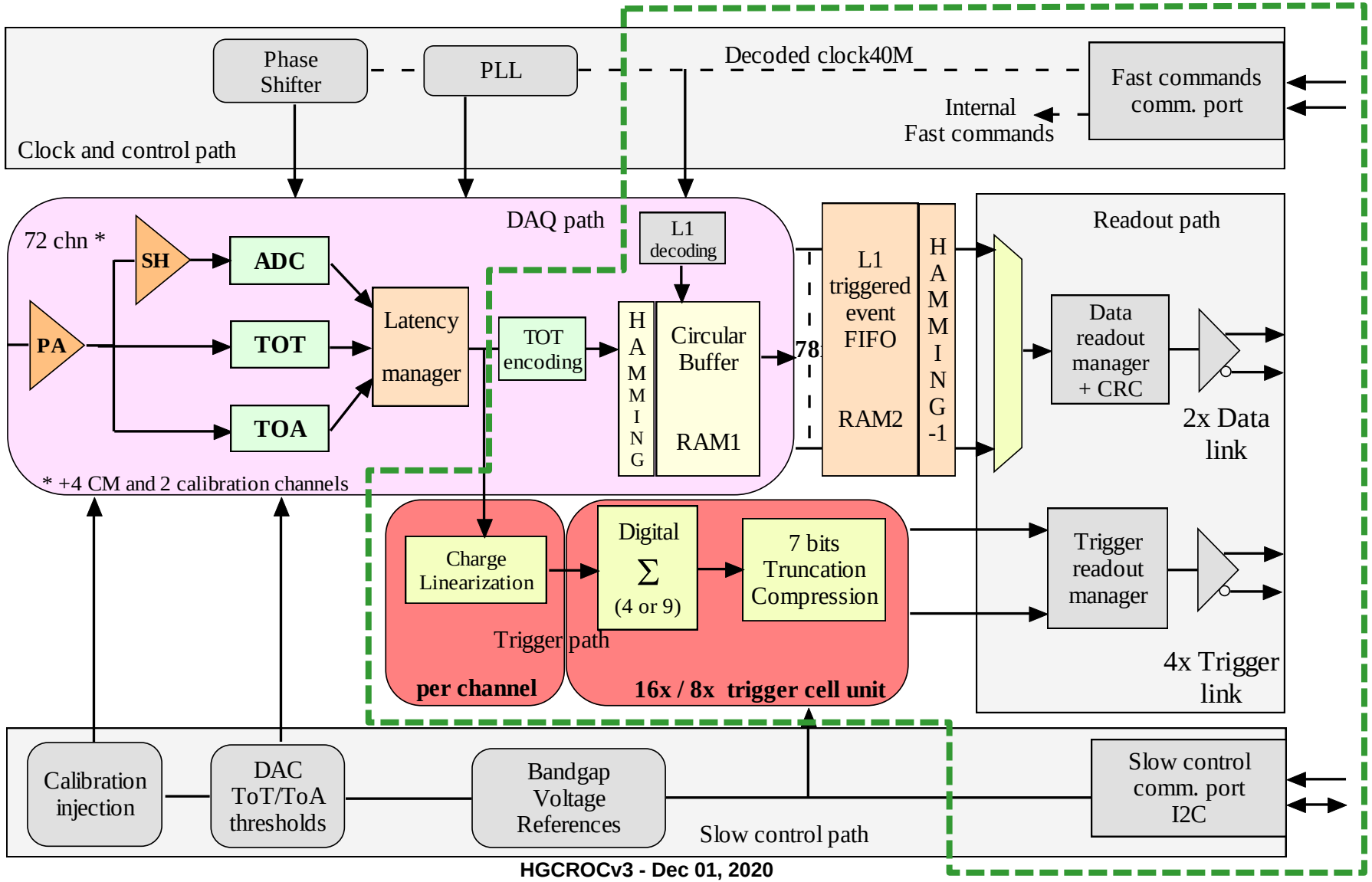
Try to not change clock architecture

40 M phase is controlled



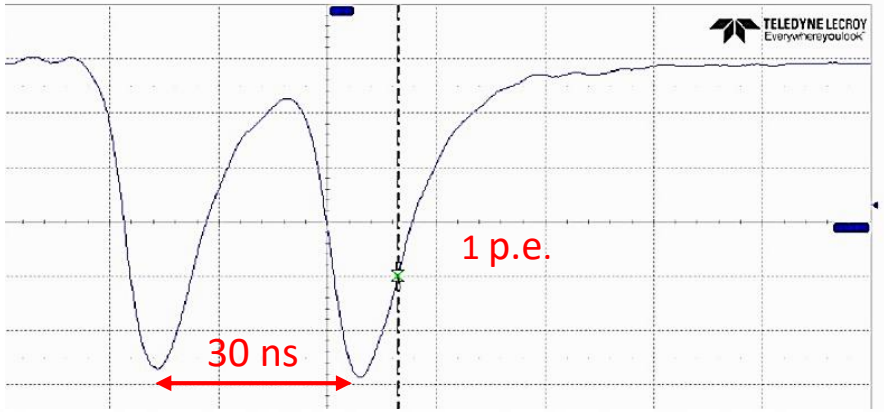
Possible clocking scheme - HGCROC-EIC
Propagate a 40 MHz (aligned with 320 M)

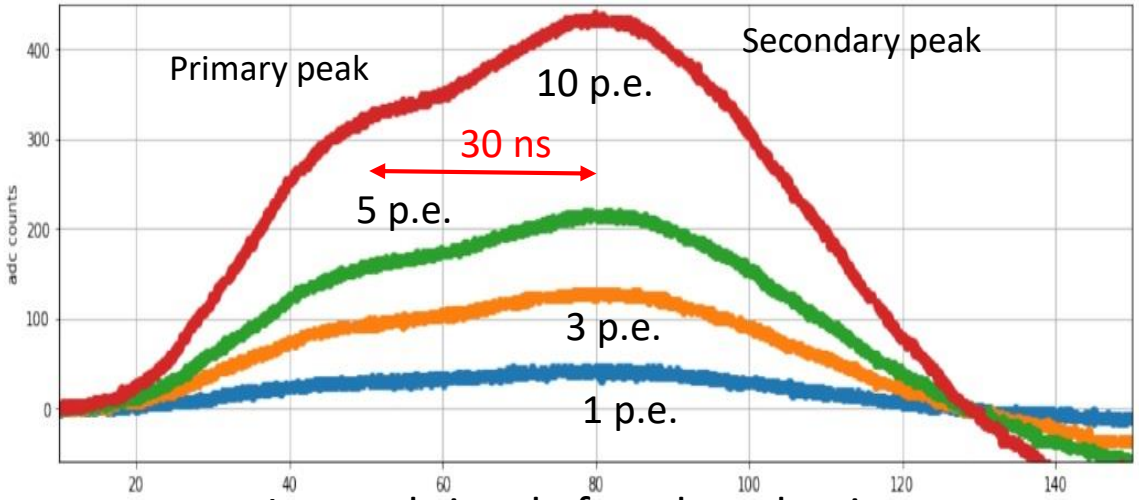
- Detail the functionality of this part
- Detail the design process used



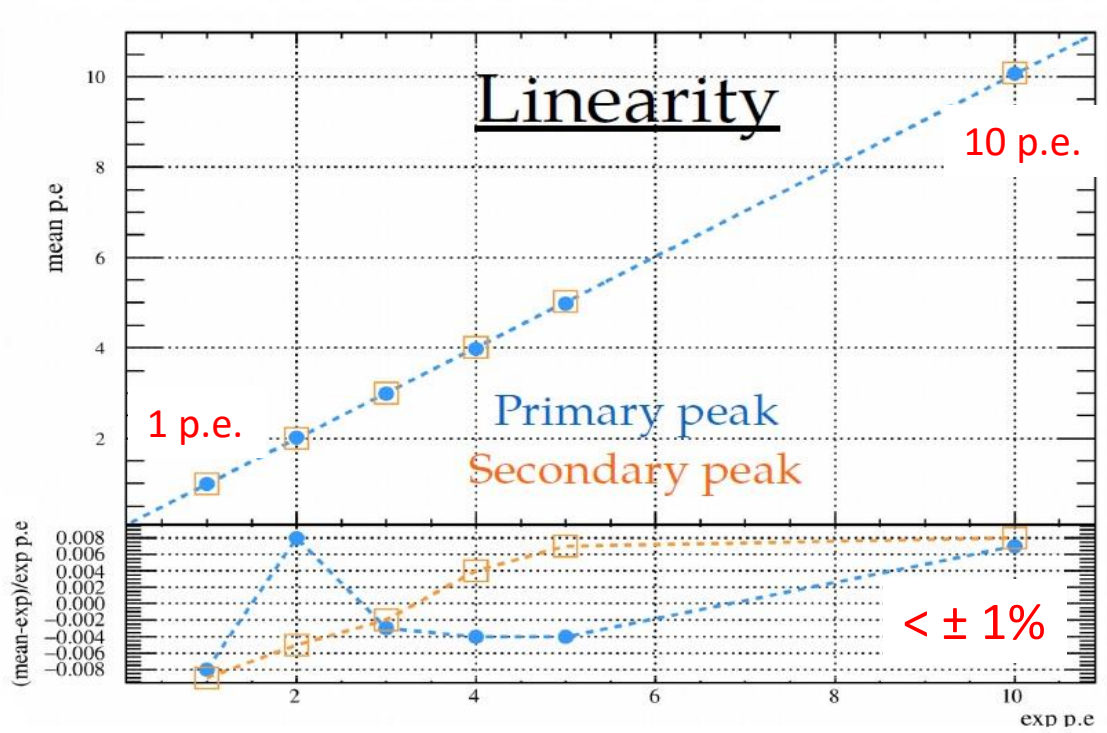
Main experimental results with HKROC0 - Pile-up

- Measurement with 2 events separated by ~30 ns (full chain: analog, digital and reconstruction)
  - Signals auto-triggered (internal prommagble threshold)





Internal signal after slow shaping



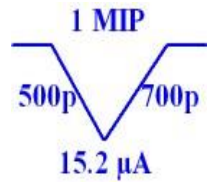
Charge reconstruction algorithm of the two peaks

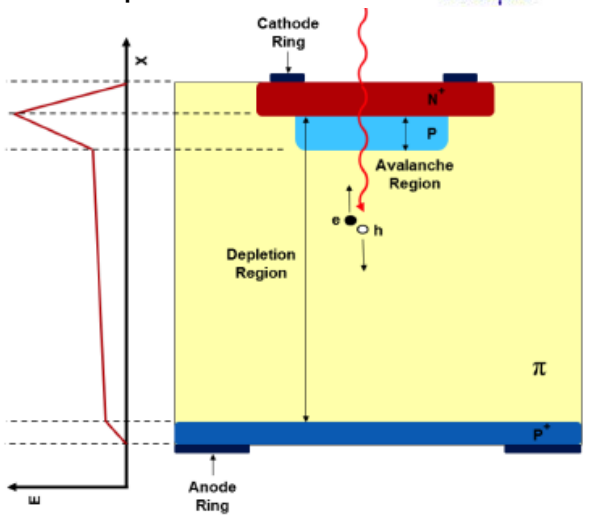
Good linearity of reconstructed pile-up events

We can reconstruct both peaks properly !

High Granularity Timing Detector in HL-LHC

LGAD sensor
1.3 x 1.3 mm^2
Thickness = 50 µm
Cd = 4 pF



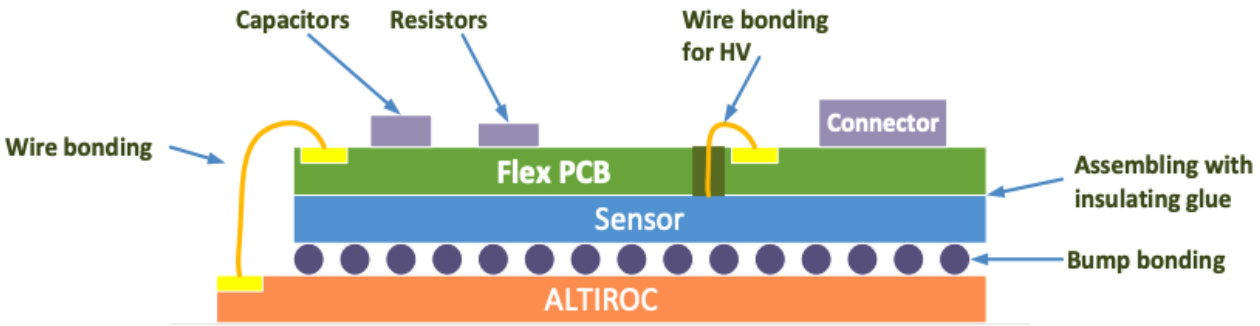


ASIC'S REQUIREMENTS

225 channels
Minimum charge : 2 fC
Charge dynamic : up to 100 fC
Noise : < 0.5 fC or 3 ke^-
Cross-talk : < 2 %
Timing precision : 35 ps for 10 fC
(per hit) 70 ps for 4 fC

Calibration LGAD-like injection :
Range : 0 – 100 fC
Rise time : 0.5-1.5 ns

Luminosity : Number of hits per bunch crossing for 2 time windows



Talk on the long Flexible Printed Circuits from Marisol Robles Manzano on Thursday, 9h20

TOA TDC
Resolution : 20 ps
Measurement window : 2.5 ns
Conversion time : < 25 ns

TOT TDC
Resolution : 120 ps
Dynamic range : 20 ns
Conversion time : < 25 ns

Radiation tolerance
TID : 2 MGy w/SF=2,25
NIEL : 2.5 10^{15} n_{eq}/cm^2 w/SF=1.5
SEE : 10^{15} n_{eq}/cm^2 w/SF=1.5
SEU rate : < 5 % per hour

ASIC power dissipation < 1.2 W
Per channel :
Analog very front-end : < 2 mW
TDC : 0,5 mW at 10 % occupancy
Digital : < 2 mW

ATLAS HGTD: ALTIROC ASIC

- **ALTIROC (**Atlas Lgad Timing Integrated ReadOut Chip)
  - Design under OMEGA responsibilty - Collaboration CERN Geneva, LPCF Clermont-Ferrand, IFAE Barcelona, SLAC Stanford, SMU Dallas
  - 20 ps timing silicon timing detector for jet identification and pileup rejection

  ⇒ Pixel ASIC for precise timing measurements
    - **Qmin/Cd ~ 500 µV** with **Cd ~4 pF** (1300 x 1300 µm2) and **Vth min= 2 fC** to be compared with other timing ASIC for which Qmin/C > 2 mV with Cd ~ 50 fF (50 x 50 µm^2) and Vth min = 0.1 – 0.2 fC

  ⇒ Mix of requirements specific to calorimetry and some of the requirements specific to pixel ASICs for trackers

  ⇒ Mix of Analog on Top design for the floorplan and analog performance + Digital on Top design for digital part (70% of the ASIC)

  - ALTIROC2 : first 225 channels full matrix LGAD readout chip with **1 GHz** preamplifier **4 pF** detector capacitance = **new territory in HEP**

- See details in https://indico.cern.ch/event/1127562/contributions/4904499/attachments/2511666/4317317/ALTIROC2_ATLAS_HGTD.pdf