Electronics and DAQ WG Meeting: 6/22/2023

- News / status update
- Continued RDO Discussion

News / Status

- Abstracts & Talks
  - Warsaw EICUG July 23-28 (combined EICUG & ePIC collab (27-30))
    - https://indico.cern.ch/event/1238718/timetable/#20230727
    - Convener will give DAQ talk remote on 27th (Me or Fernando)
    - Please register, even if remote
  - Hawaii APS/JPS (October 7-12)/(12-13)
    - Jo Schambach to give DAQ talk and is preparing abstract to submit

- S&C Streaming Readout WG (tentatively to meet next week, June 27th @ 1:30pm EST)
  - The indico will be announced here (with other S&C WGs): https://indico.bnl.gov/category/463/

- Services Requests
  - DAQ still needs to fill out services form (this is on Jeff, Fernando & Dave) but we are closer:
    - Racks:
      - Electronics on DAQ platform (38 + RDOs on platform: 15 Bias, 7 LV, 2 HV, 10 Digitizer, 4 network & fiber distribution)
      - DAQ Room (20 racks)
    - Fibers we have estimates from channels table
    - Cabling (unsure, Fernando may know better, but presumably can be estimated from electronics in racks)

- RDO physical specification & location determination (topic for continued discussion today)
  - Note for all: Please start using the mailing list for these discussions!

RDO: We need to specify the location of RDOs and their Physical Specifications!

- The RDO will be a "standard board" but we assume it might need variations
  - Optical transceiver
  - Size / shape
  - # of FEB connectors
  - If necessary, could be integrated in a FEB
  - Will need firmware implementation for specific ASICs
- Electronics and DAQ have agreed to specify features of the default standard RDO
  - Size of board (I am assuming something around 4x4 inches or less)
  - Type and number of connectors
  - Length of drive (depends on rate/cables/voltages)
  - Power need (3-4 Watts)
  - Maximum radiation level for proper functioning

Assuming:

- Artix/Artix-like FPGA
- 16-32 serial links / connectors for ASIC connections
- 3(4) fiber links possible, with 2 populated in most cases.
- The DAQ fiber protocol to be uniform for all detectors. Potentially using 2 schemes for timing distribution
- Any boards inside detector need to be pre-installed in their sub-detector and inserted with the detector and can be accessed only once/per year or so…
- Cost ~$500 / board
- Pay attention to "fiber pair" on DAQ table. This is number of RDOs

Points from last weeks discussion

- Need to go by detector, and focus first on barrel. (MAPS trackers, dRICH, pfRICH, TOF, eTOF, MPGDs, Astropix, DIRC, eCals, hCals)
- The "standard board with variations" has different meanings to different people and there are issues that need to be clarified
  - How will the collaboration between the eRD109 groups and the "standard DAQ protocol" by done?
  - The schedules for needing readout do not necessarily line up. eRD groups need some sort of readout now which implies putting effort in now, whereas DAQ efforts on RDO start after construction starts --- given this, how do we organize the designs to both get rid of redundant work and also get the uniform DAQ interface?
  - It's clear that the level of aggregation on the RDOs is far different for some detectors, which will define space needed so can we define this by detector?
  - The scheme's for connecting the FEBs to the RDOs is not at all uniform at the moment, so we need to document this detector by detector

Central Detectors

Detector	Concept	Plan for FEB Development	Plan for RDO development	# FEBs/RDO	# RDOs	Size	Location MAP?
MAPs Vertex	RDO near staves?						
MAPs Sagitta							
MAPs Disks							
dRICH	RDO between FEB						
pfRICH							
DIRC							
Barrel TOF	RDO near FEB						
Endcap TOF							
MPGDs							
Astropix eCAL	RDO near staves?						
Backward eCAL							
Barrel eCAL	LVDS cables						
Backward hCAL	Potential Repeaters						
Barrel hCAL	RDO on platform						
Forward hCAL							
Forward eCAL	RDO near FEB?						

EPIC Detector Scale and Technology Summary:

Detector System	Channels	Fiber pair	Data Volume	DAM Boards	Readout Technology	Notes
Si Tracking: 3 vertex layers, 2 sagitta layers, 5 backward disks, 5 forward disks	7 m^2 36B pixels 5,200 MAPS sensors	400	25Gb/sec	10	MAPS: Several flavors: curved its-3 sensors for vertex Its-2 staves / w its-3 improvements	Fiber count limited by Artix Transcievers
MPGD tracking: 3 layers	100k	15	<10Gb/sec	1	64 channel SALSA ASIC	Assume 512 Channel (8 ASIC)/FEB + 16 FEB/RDO
Calorimeters: Forward: LFHCAL ECAL W/SciFi Barrel: HCAL HCAL insert* ECAL (Imaging) SciFi/PB ASTROPIX ECAL (SciGlass) Backward: NHCAL ECAL (PWO)	 64k 19k 8k 8k 8k 88M pixels 8k 16.2k 3k	 80 75 32 32 32 24 32 18 12	15Gb/sec	10	SiPM using HGCROC &/or FPGA bases boards with FLASH ADC	ECAL will be SciGlass OR Imaging Assume HGCROC 56 ch * 16 ASIC/RDO = 896 ch/fiber Assume FLASH FEB 16 ch * 16 FEB/RDO = 256 ch/fiber HCAL assume HGCROC ECAL assume FLASH for fiber calculations *HCAL inset not yet part of baseline
Far Forward: B0: 3 MAPS layers 1 or 2 AC-LGAD layer 2 Roman Pots 2 Off Momentum ZDC: Crystal Calorimeter 32 Silicon pad layer 4 silicon pixel layers 2 boxes scintillator	 3x20cmx20cm (300M pixel) 300k or 600k 1M (4 x 135k layers each) 650k (4 x 80k layers each) 400 11520 160k 72	 6 30 64 42 10 10 10 2	<1Gb/sec	5	 MAPS AC-LGAG / EICROC AC-LGAD / EICROC AC-LGAD / EICROC APD HGCROC as per ALICE FoCal-E	 600^cm layers (1 or 2 layers) 13 x 26cm layers 9.6 x 22.4cm layers There are alternatives for AC-LGAD using MAPS and low channel count DC-LGAD timing layers
Far Backward: Low Q Tagger 1 Low Q Tagger 2 Lumi PS Cal (2 calorimeters) Lumi PS tracker Photon Detector	 1.3M 480k 1425/75 80M	 80 32 16 18	100Gb/sec (<1 Gb/sec to tape)	4 1 1	 AC-LGAD / EICROC AC-LGAD / EICROC SiPM / PMT	 40cmx40cmx500um 30cmx20cmx500um Possible tracking layers
PID-TOF	3M-50M	240-500	6Gb/sec	12	EICROC / AC-LGAD	Channel / Fiber counts depend on sensor geometry. Considering pitches of: .5mm x 1cm, .5mm x .3cm, .5mm x .5mm
PID-Cherenkov: dRICH pfRICH (or) mRICH DIRC	 300k 70k 70k 74k	 200 17 17 288	 1830Gb/s (<20Gbps to tape) 15Gbps 11Gb/sec	 20 1 1 6	 SiPM / ALCOR LAPPD LAPPD HDSoC64 (HRPPD/MCP-PMT)	 Worse case after radiation. Includes 30% timing window. Requires further data volume reduction (software trigger, or AI/ML) 12 boxes x 24 sensor x 4 asic x 64 ch

Calorimeter Connector Concept