AstroPix v4

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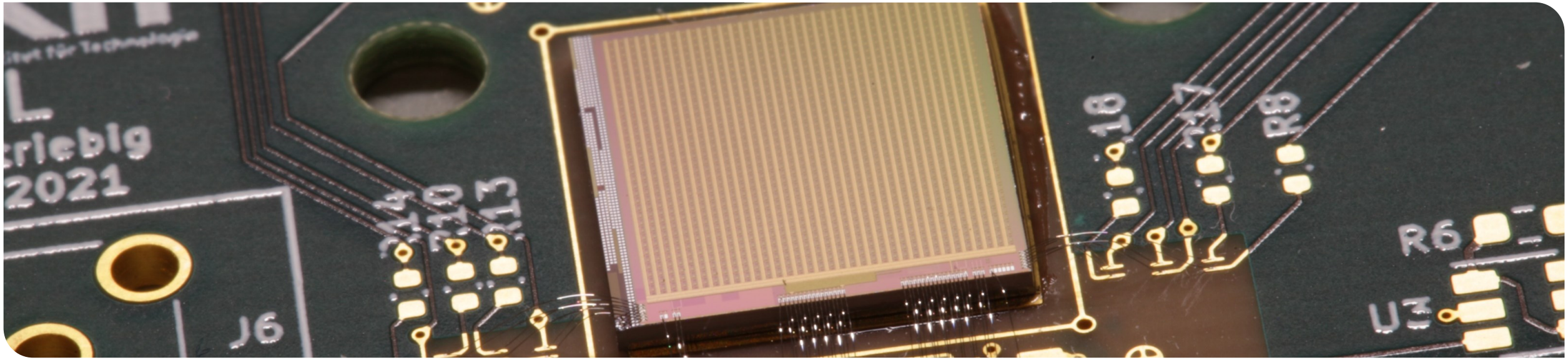
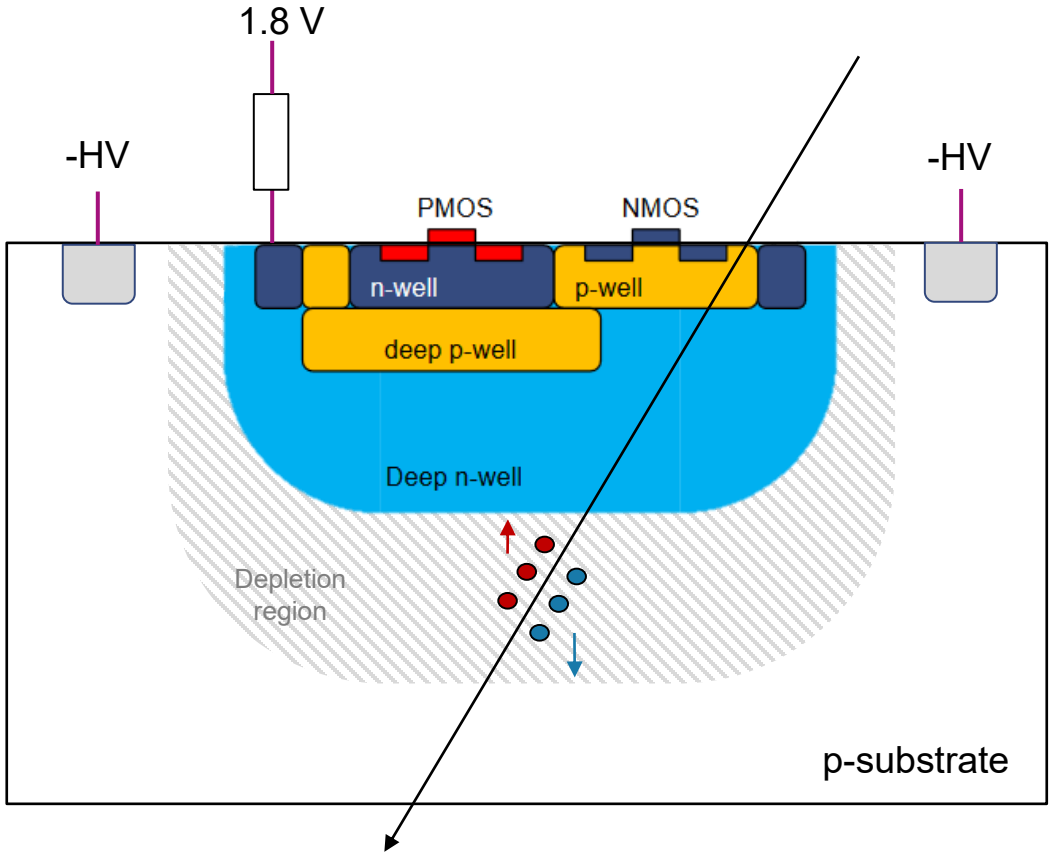


Introduction – HV-CMOS

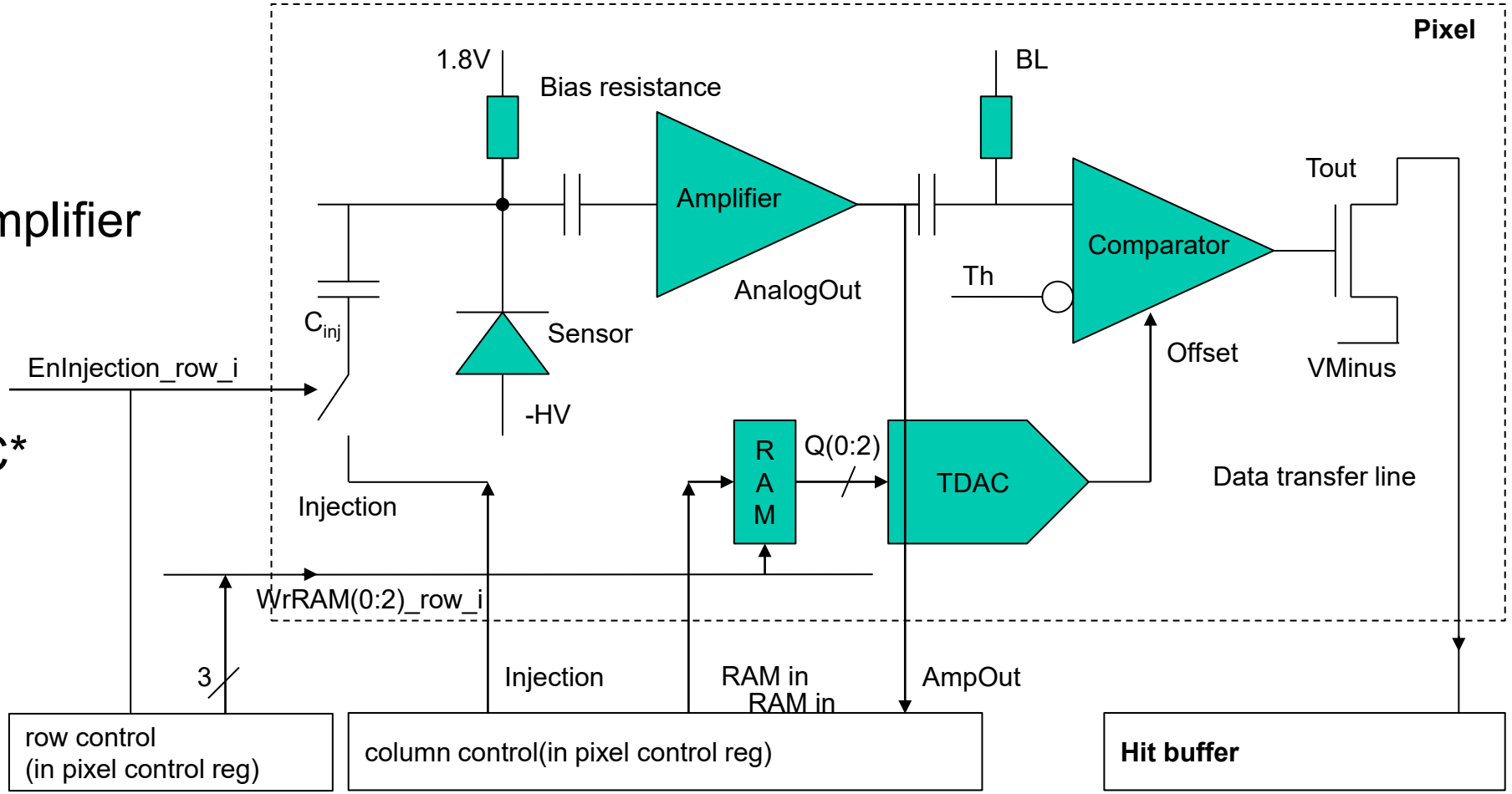
- Charged particles or photons generate electron-hole pairs in depletion region of the sensing diode formed by deep n-well and p-substrate
- Separated by strong electric field
- Electrons drift to charge-collecting deep n-well
- Deep n-well contains shallow wells for electronics
- **High-Voltage CMOS Active Pixel Sensor (HVMAPS)**



AstroPix4: Analogue Part

Pixel contains:

- Sensor diode
- Charge Sensitive Amplifier (CSA)
- Comparator
- Threshold tune DAC*
- RAM for tune bits*



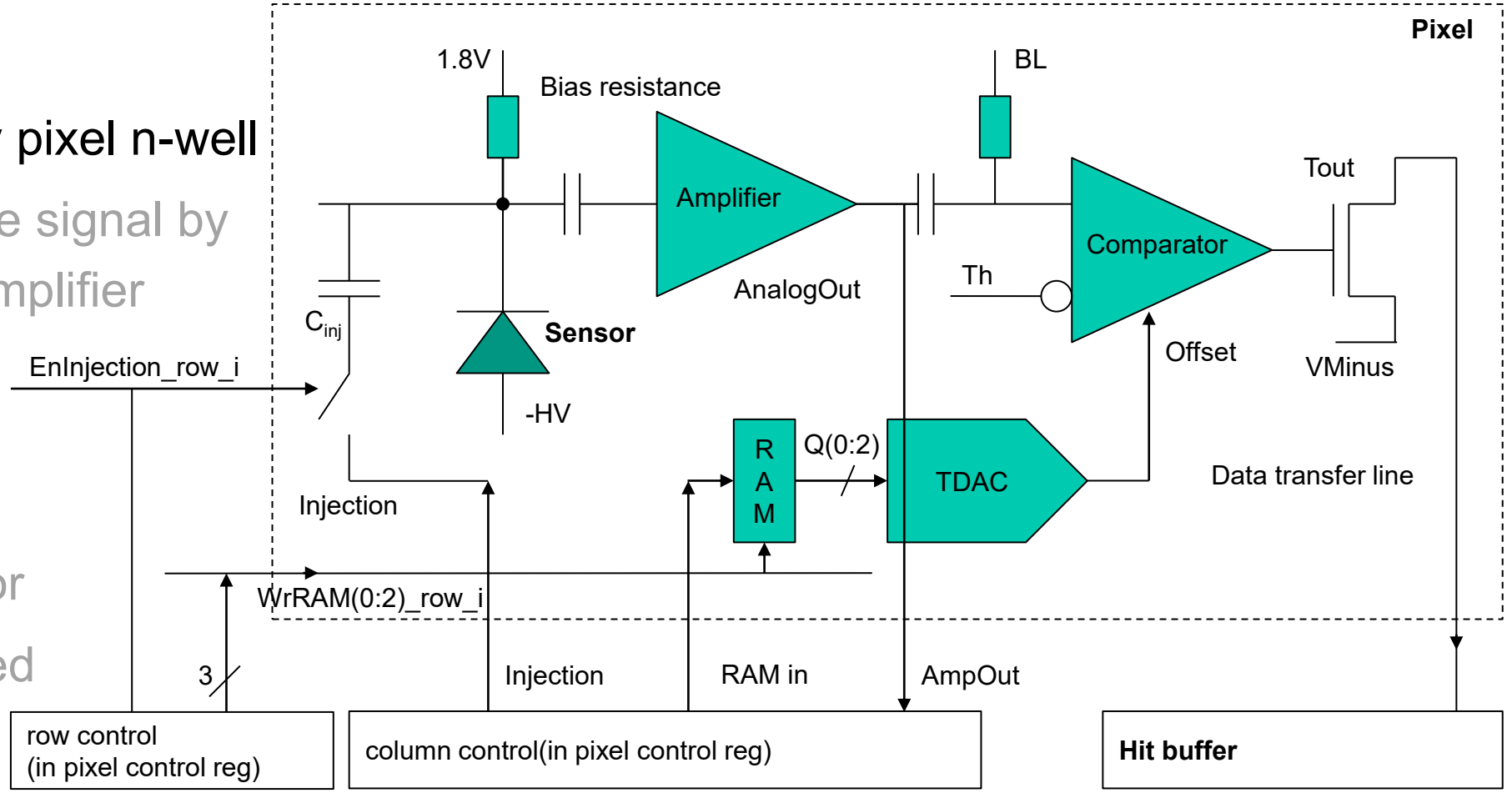
*placed in the periphery

Source: Ivan Perić

AstroPix4 : Analogue Part

Working principle:

1. Charge collected by pixel n-well
2. Converted to voltage signal by Charge Sensitive Amplifier
3. Analog voltage pulse shaped and converted to digital signal by comparator
4. Hit information stored in hit buffer



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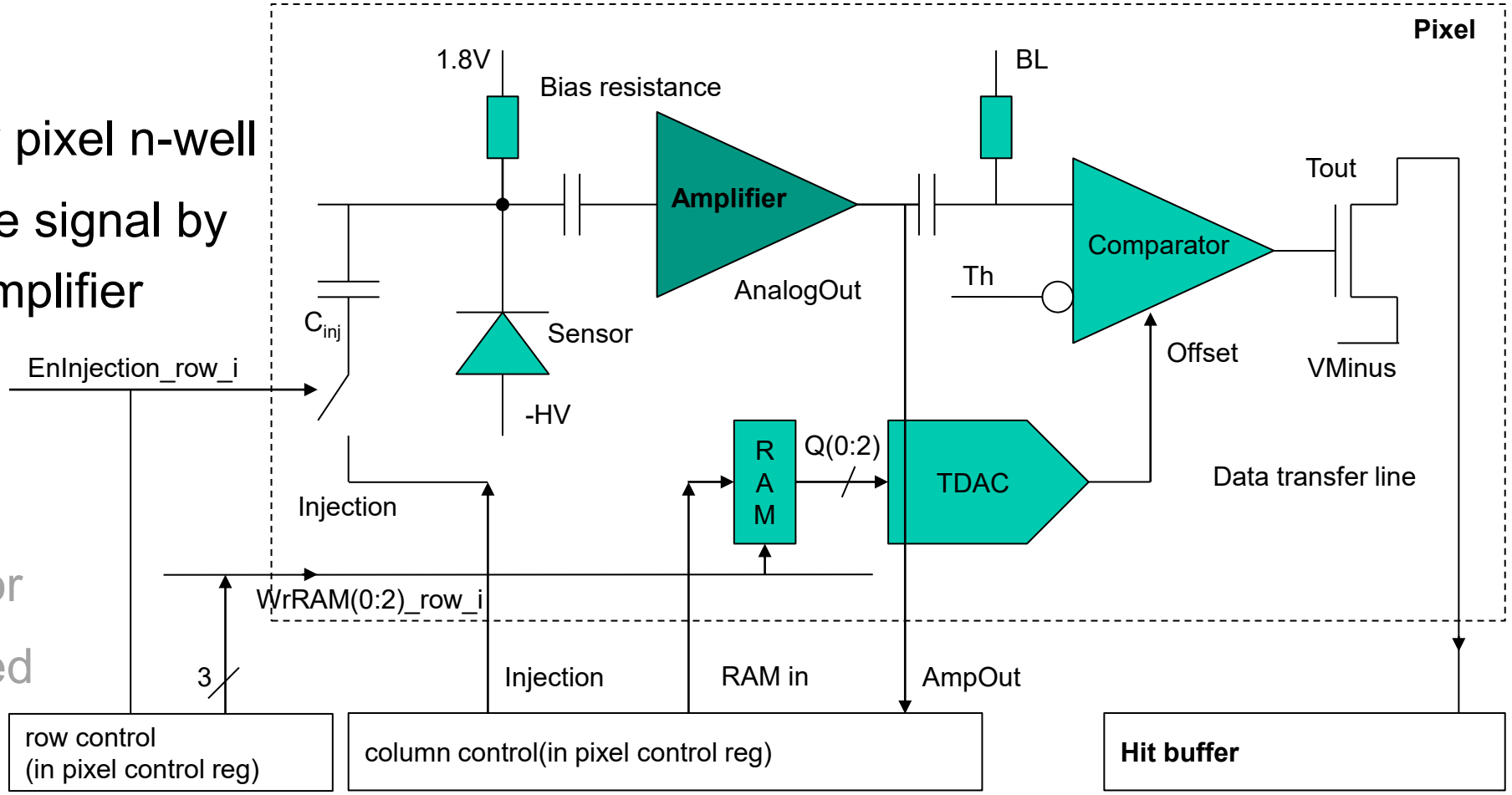

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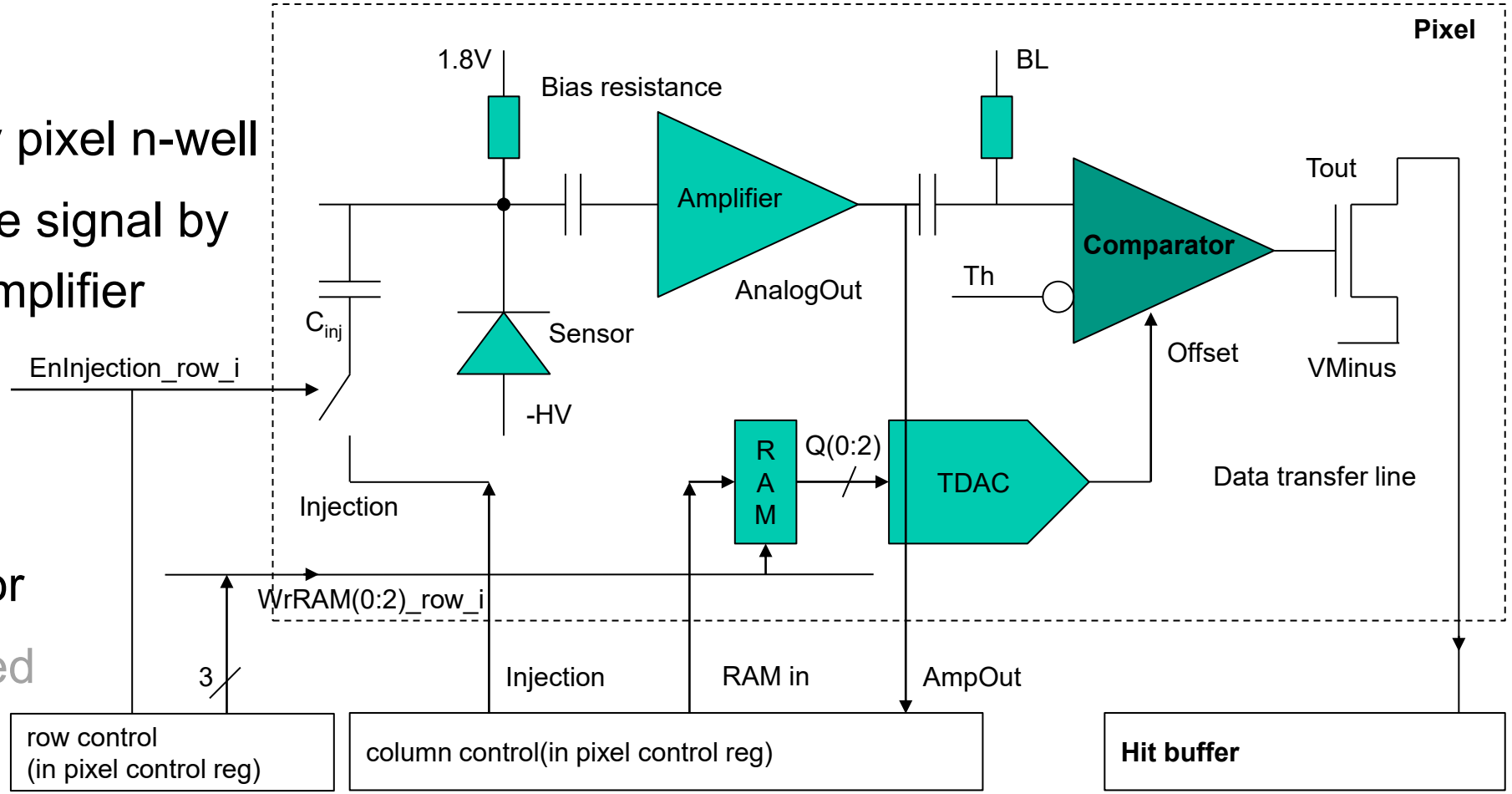

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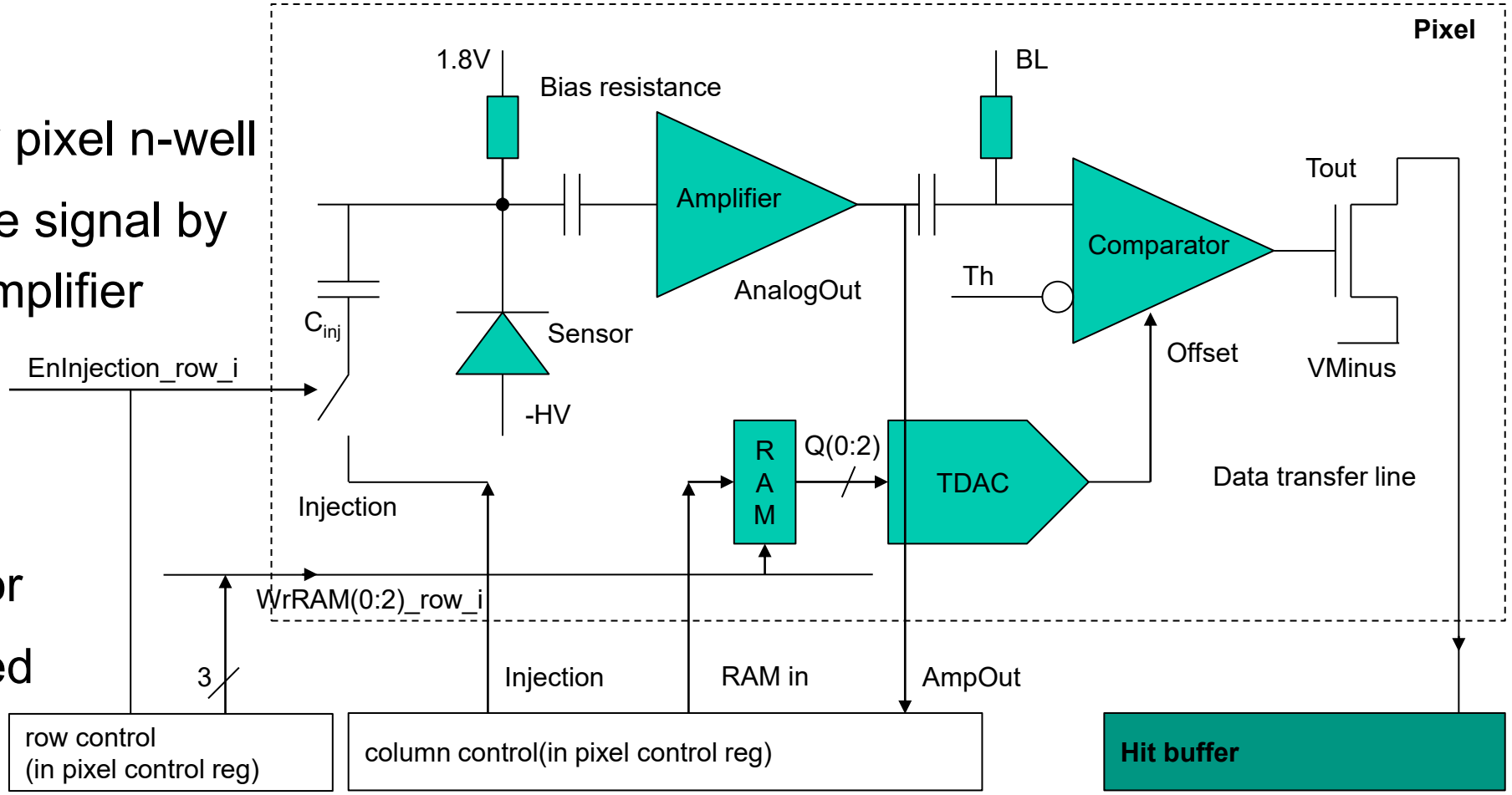
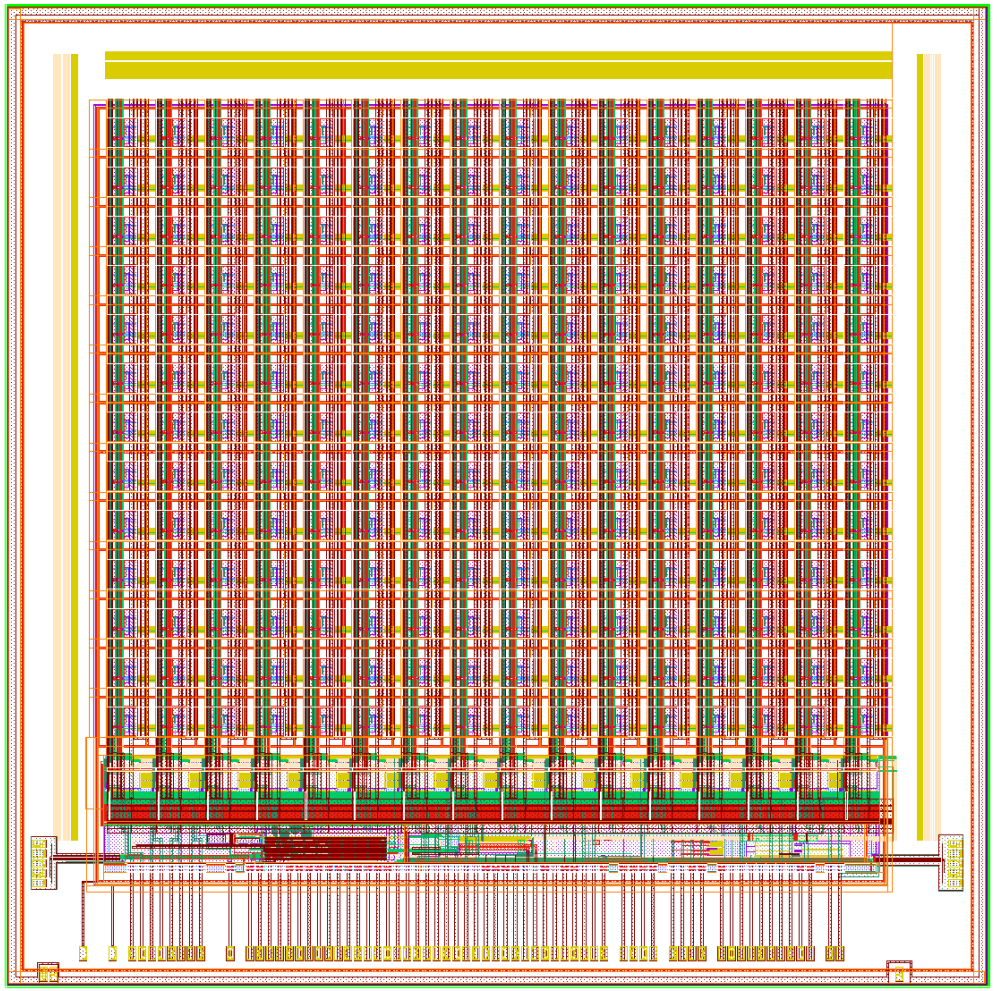


Source: Ivan Perić

Specifications for TSI May 2023 run

- Size: 1 cm x 1 cm
- Matrix: 16 x 13 pixels
- Pixel size: 300 um x 300 um
- Pixel pitch: 500 um
- Interfaces: QSPI Daisychain, SR
- Integrated voltage DACs
- Integrated injection switch
- Integrated temperature sensors

- **Improvements over v3:**
  - TuneDACs
  - Hitbuffers + FlashTDC measurement
  - Reduced pixel capacitance
    274 fF vs 391 fF @100um t_dep

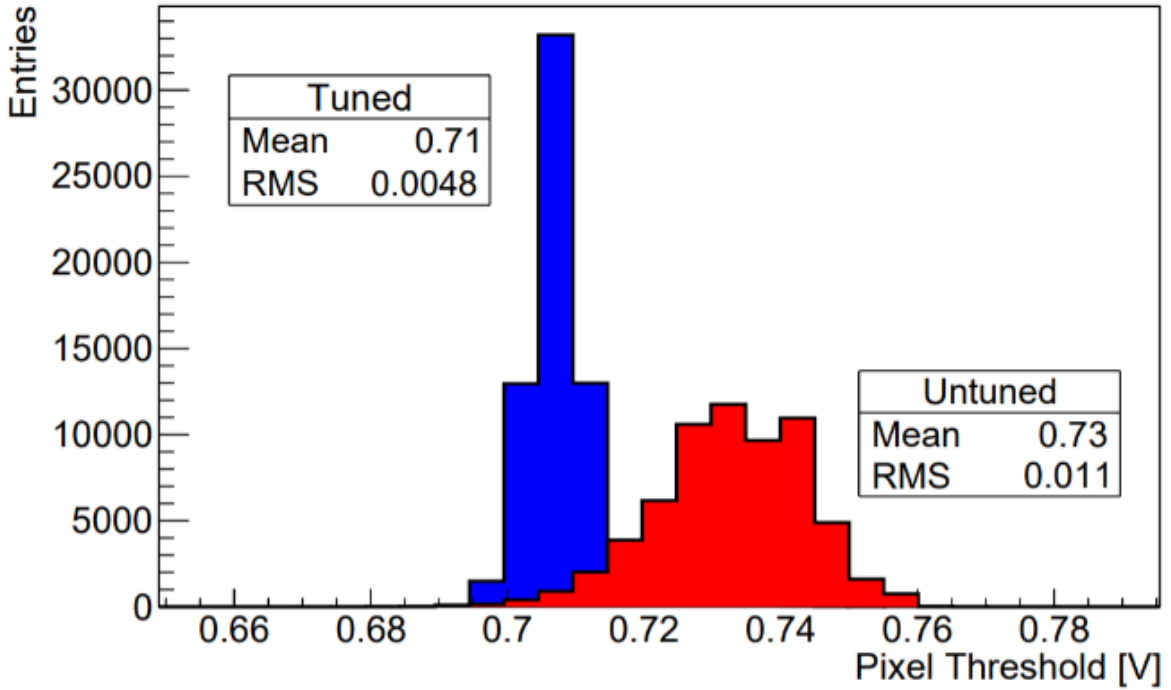


AstroPix4 I/O

- Clocks: 2.5 MHz timestamp clock (used as refclk for PLL)
- Digital Interfaces:
  - QSPI max. 5 MB/s: Configuration, Readout
  - Shiftregister Interface: Configuration fallback
- Interrupt, Hold
- Analog output: monitor amplifier output in Row0
- Hitbus: monitor comparator outputs
- Cal: Injection pulse
- Power:
  - Analog 1.8 V + 1.2V
  - Digital 1.8 V
  - Vminuspix 0 – 0.9 V
  - HV

TuneDACs

- 3 SRAM cells per pixel to control current DAC
- Number of bits can be increased if needed
- Placed in periphery
  - would add capacitance if placed in pixel
- Used to tune comparator branch currents to compensate threshold dispersion

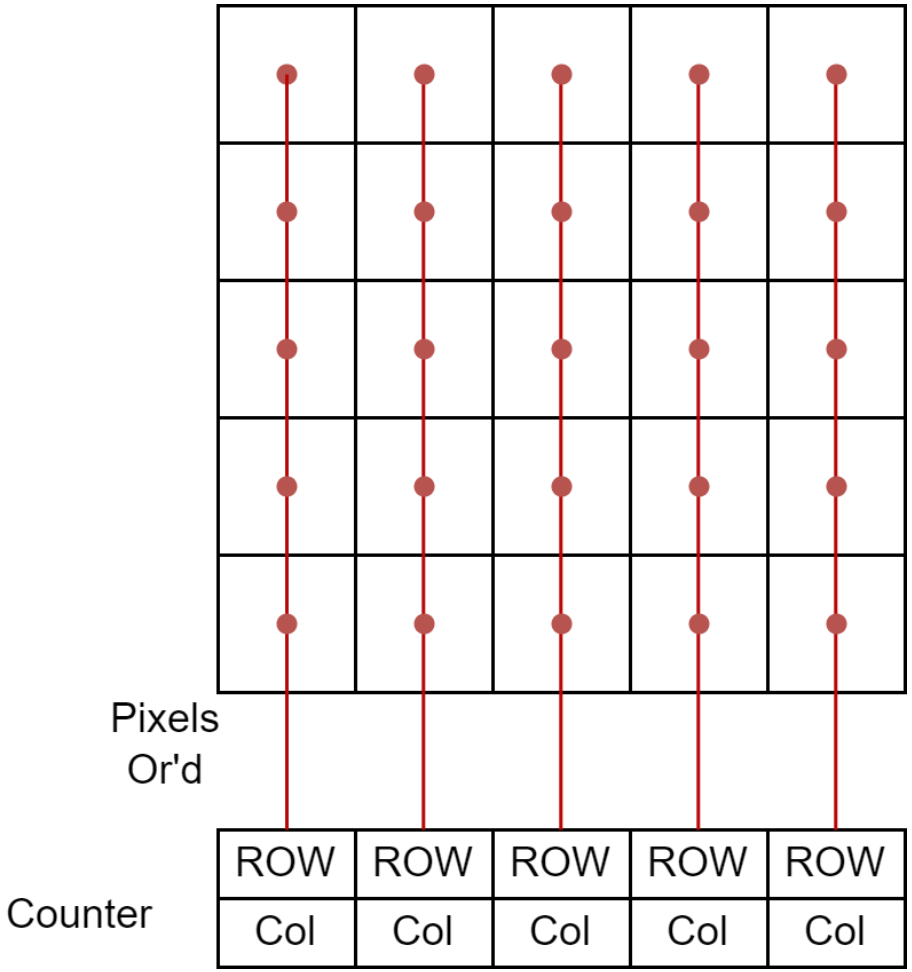


(b) The threshold dispersion before (red) and after (blue) tuning for the full MuPix10 matrix with an equivalent signal of 3000 e^-.

Source: https://arxiv.org/pdf/2012.05868.pdf

Astropix v1 - v3: Or'd Rows and Columns

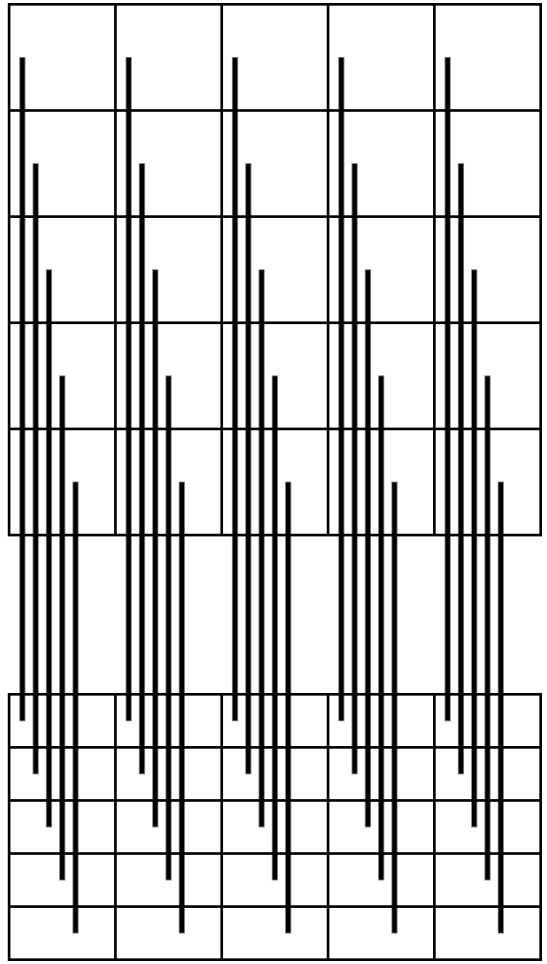
- Or'd Rows and Columns
- Advantages:
  - Low number of channels
- Disadvantages:
  - Identification problems with multiple hits in Row/Col
  - High bus capacitance → limits time resolution



Astropix v4: Individual Hitbuffers

- Hits from every pixel are saved individually
- 16 x 13 pixel matrix -> 208 hitbuffers
- Similar to ATLASpix design

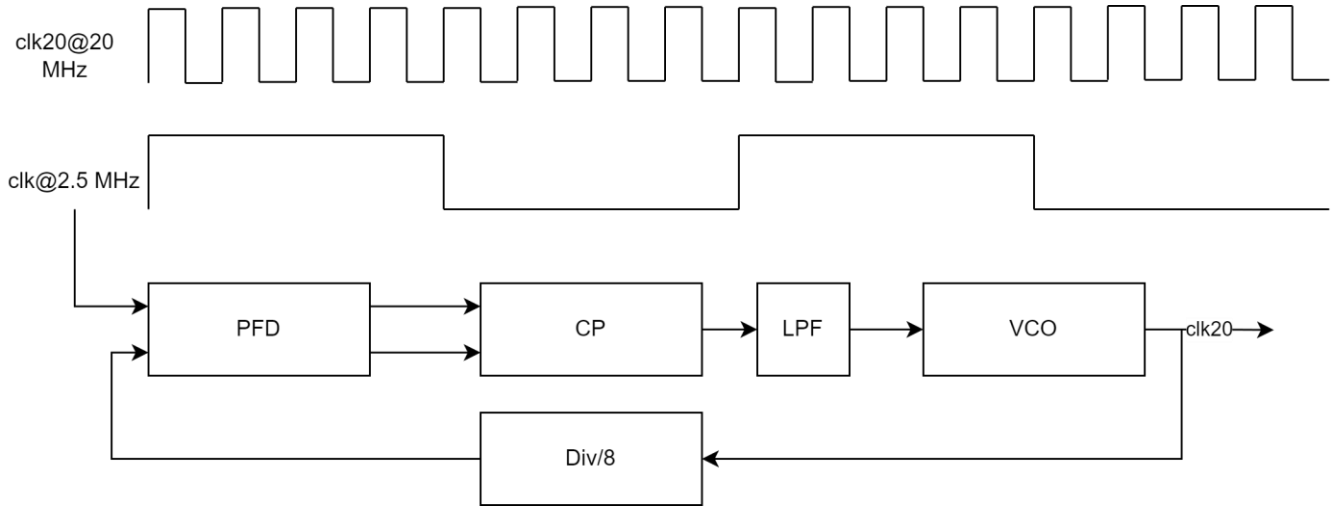
- Advantages:
  - No identification problems with multiple hits in Row/Col
- Disadvantages:
  - Occupies larger chip area



1Hitbuffer per Pixel

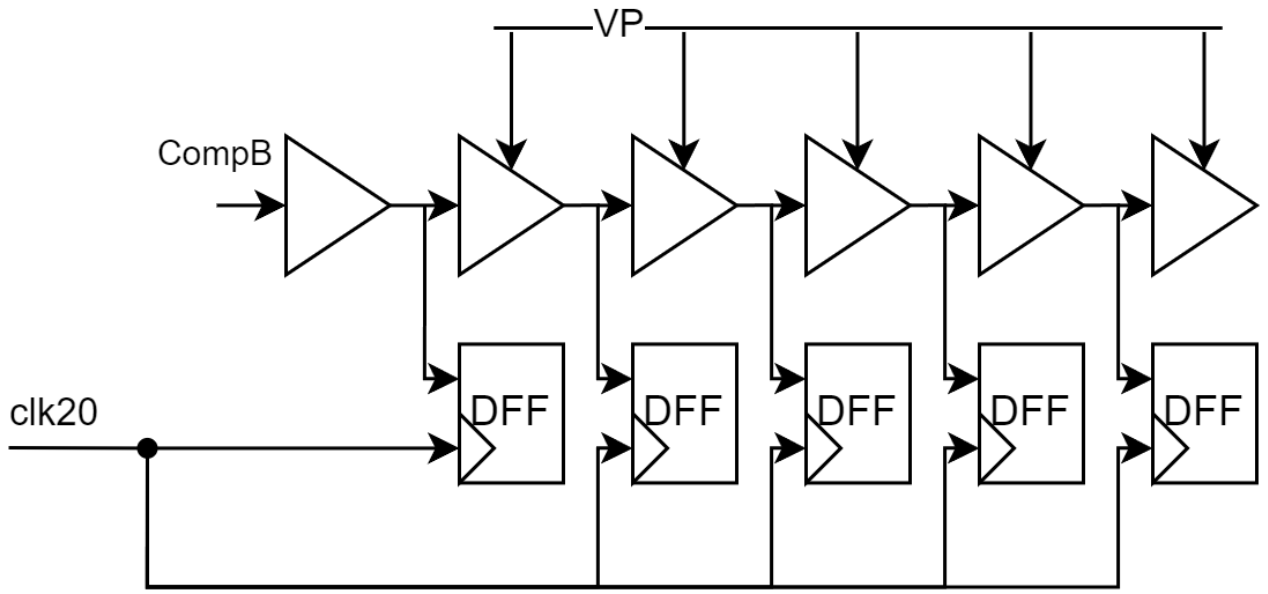
AstroPix Hitbuffer

- Logic + DRAM cells
- TS gets saved on positive and negative edge of a hit:
  - 20 MHz from PLL with 2.5 MHz reference -> 17bit@50ns
  - Covers 6.55 ms



AstroPix Hitbuffer

- FineTS:
  - Flash TDC with 16 delay elements (32 current starved inverters)
  - Resolution of 2.94 ns



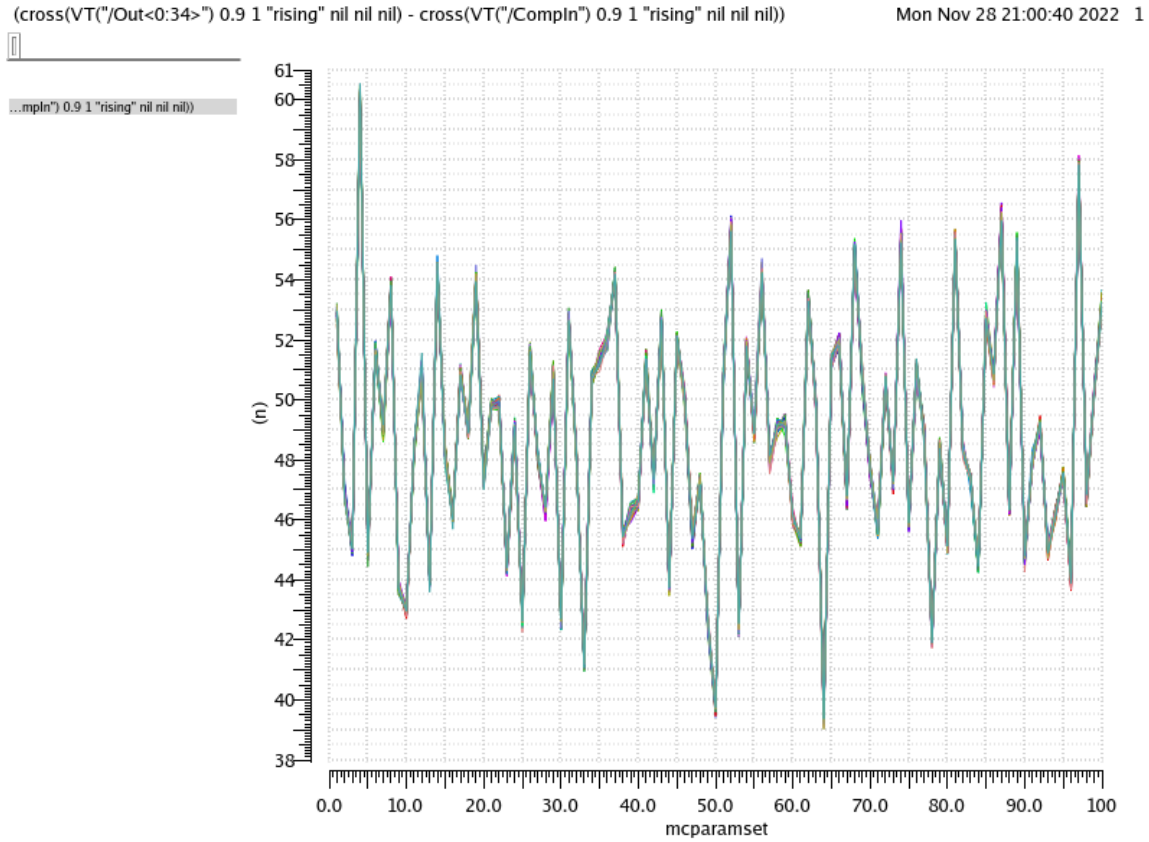
5-bit Flash-TDC example

AstroPix Hitbuffer TDC

- **Problem**: Flash TDC is very susceptible to process and temperature variation

- Without calibration:
  - Nominal delay should be 50 ns
  - Mismatch: +/- 3.7 LSB
  - Temperature variation (10 to 50 °C): ~5.4 LSB

- 1225 Flash TDCs have to be calibrated for mismatch/process and temperature ☹

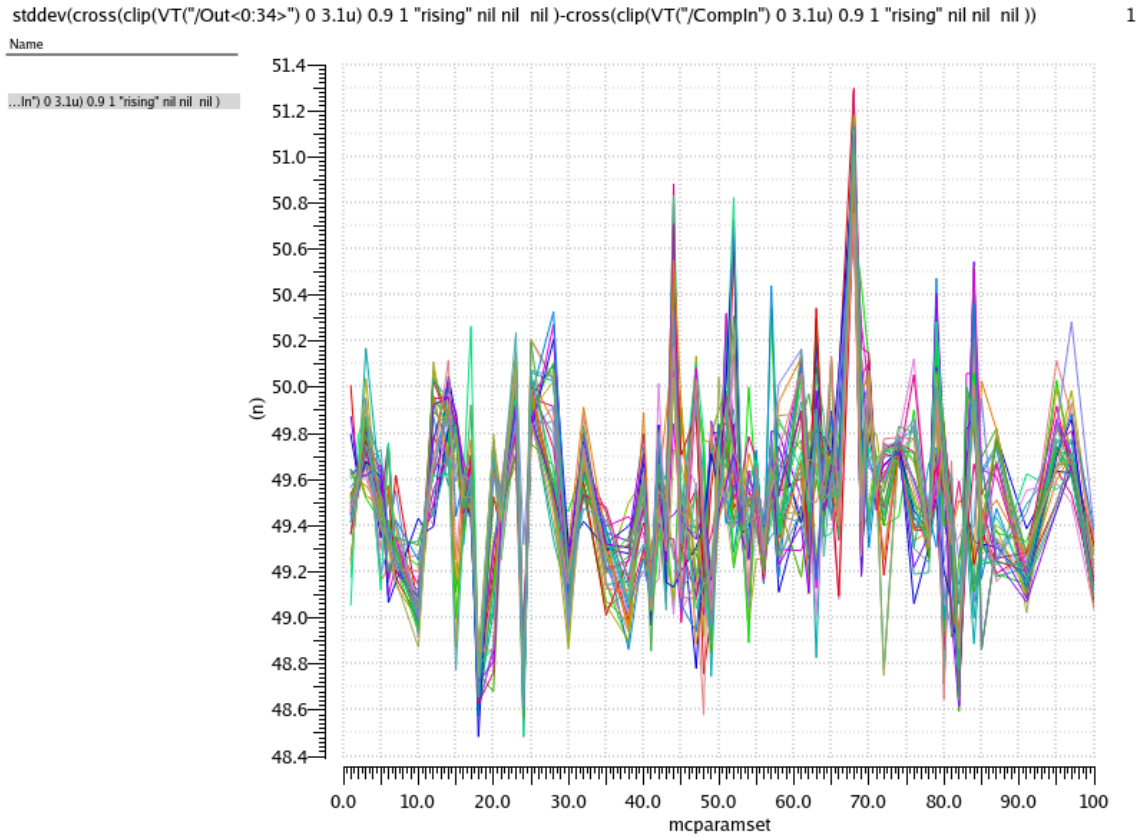


AstroPix Hitbuffer TDC

- **Solution**: TDC delay elemnets are stabilized by global DLL (1 per chip)

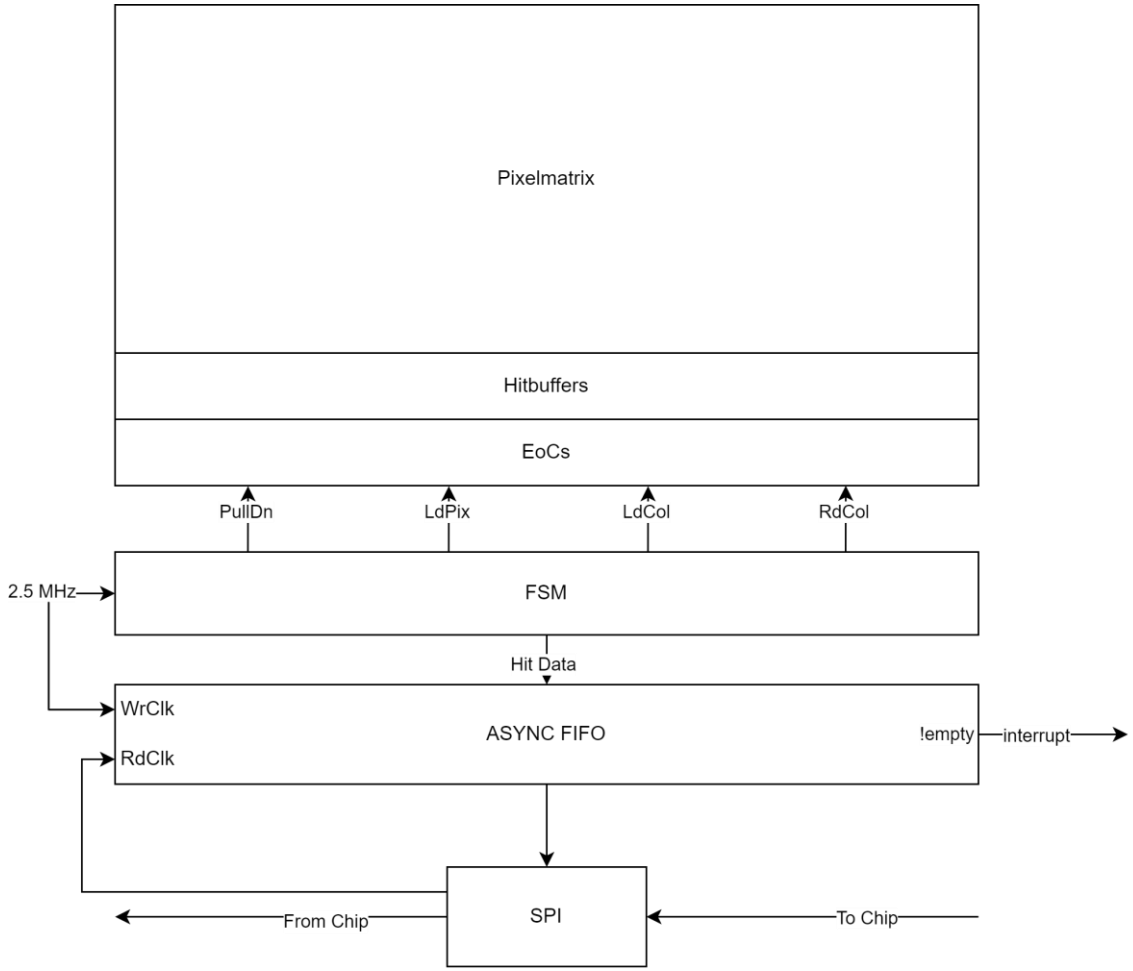
- Without calibration:
  - Mismatch: +/- 0.5 LSB
  - Temperature variation (10 to 50 °C): < 0.17 LSB

- Can be improved with automatic calibration
  - After each measurement, automatic measurement of a fixed time period, i.e. 1 clock cycle



Readout logic

- Controlled by state-machine (FSM)
- Working principle:
  - Priority Logic: Data from highest active Hitbuffers in every column are loaded into EoCs
  - FSM goes trough all loaded columns and writes the data into async FIFO
  - If FIFO is not empty, interrupt goes low
  - DAQ toggles the SPI clock, which initiates FIFO readout via QSPI Interface
  - From the outside perspective i.e. the DAQ, no difference to older AstroPix version, same protocol just different payload size



AstroPix QSPI

- AstroPix2 digital: 2x5 Byte
  - Each per Col/Row
    - 8b Header
    - 8b col/row
    - 8b TS
    - 16b ToT

- AstroPix4+: 1x8 Bytes
  - 8b Header (5 bit ChipID, 3 bit Payload)
  - 6b Row
  - 6b Col
  - 2x 18b TS
  - 2x 4b TDC

Commands

bits

7	6	5	4	3	2	1	0
Command			Chip Address				

BIT	FIELD	DESCRIPTION
[4:0]	Address	Requires 20 single addresses - 0x00 - 0x14 : Single addresses - 0x15 - 0x1F : Reserved - 0x1D: Invalid - 0x1E: Broadcast
[7:5]	Command	8 Commands: - 0x01 - NOCMD / IDLE - 0x02 - Routing: dispatch addresses - 0x03 - Shift Register Config

Readout

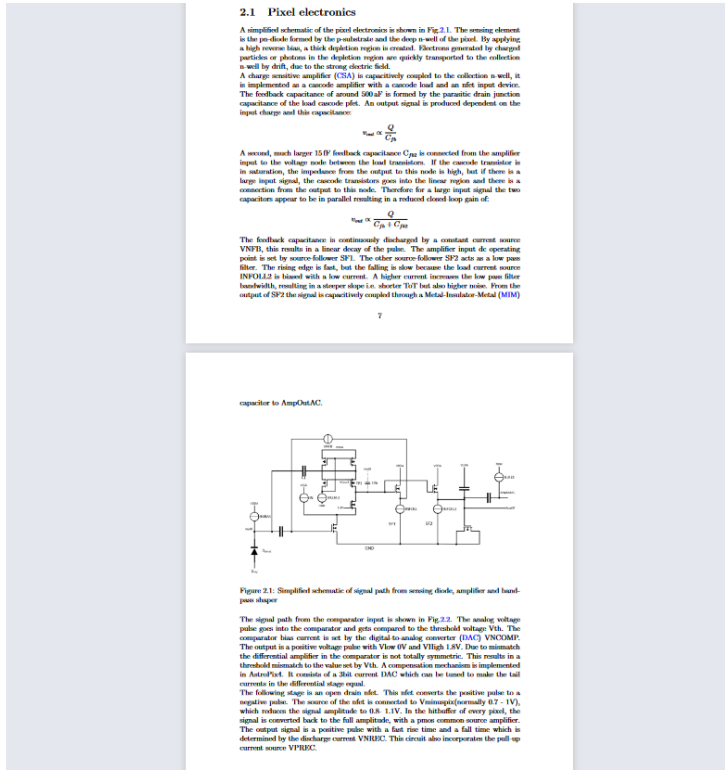
- Wait for interrupt signal low
- Toggle SPI clk to read out

AstroPix4: Requirements for ePIC

- **Dynamic range 20 keV - 3 MeV**
  - Much larger than Amego-x requirement → Amplifier redesign?
  - Wafer: Resisitivity and thickness?
- **Radiation tolerance 1 rad/year and 10^8 neutrons/cm^2/year**
  - Low TID important for HiRes wafer effectiveness
- **10 ns bunch crossing**
  - Which time resolution is actually needed?
  - 4σ would be **~1.25 ns** → not easy with large pixels
  - Amego-x requirement is only 666 ns
  - Off-chip timewalk correction is needed (~20 ns for Vth = 6*Vnoise_rms 6 keV vs. 60 keV)
- **Power consumption**
  - Better timing → higher amplifier and comparator current needed
  - Power budget? 1.5 mW/cm^2 is very optimistic

Documentation

- From Google Doc → nice Overleaf document
- Contents:
  - Explanations
  - I/O List with descriptions
  - Drawings with pad locations
  - Quickstart guide for measurements
- Started working on it
- Takes a bit of time ☺



2.1 Pixel electronics

A simplified schematic of the pixel electronics is shown in Fig.2.1. The sensing element is the pn-diode formed by the p-substrate and the deep n-well of the pixel. By applying a high reverse bias, a thick depletion region is created. Electrons generated by charged particles or photons in the depletion region are quickly transported to the collection n-well by drift, due to the strong electric field.
A charge sensitive amplifier (CSA) is capacitively coupled to the collection n-well, it is implemented as a cascode amplifier with a cascode load and an nfet input device. The feedback capacitance of around 300 aF is formed by the parasitic drain junction capacitance of the load cascode pfet. An output signal is produced dependent on the input charge and this capacitance:

$$v_{out} \propto \frac{Q}{C_{fb}}$$

A second, much larger 15 fF feedback capacitance C_{fbl} is connected from the amplifier input to the voltage node between the load transistors. If the cascode transistor is in saturation, the impedance from the output to this node is high, but if there is a large input signal, the cascode transistors goes into the linear region and there is a connection from the output to this node. Therefore for a large input signal the two capacitors appear to be in parallel resulting in a reduced closed loop gain of:

$$v_{out} \propto \frac{Q}{C_{fb} + C_{fbl}}$$

The feedback capacitance is continuously discharged by a constant current source VNFB, this results in a linear decay of the pulse. The amplifier input dc operating point is set by source-follower SF1. The other source-follower SF2 acts as a low pass filter. The rising edge is fast, but the falling is slow because the load current source INFOLL2 is biased with a low current. A higher current increases the low pass filter bandwidth, resulting in a steeper slope i.e. shorter ToT but also higher noise. From the output of SF2 the signal is capacitively coupled through a Metal-Insulator-Metal (MIM)

7

capacitor to AmpOutAC.

Figure 2.1: Simplified schematic of signal path from sensing diode, amplifier and band-pass shaper

The signal path from the comparator input is shown in Fig.2.2. The analog voltage pulse goes into the comparator and gets compared to the threshold voltage Vth. The comparator bias current is set by the digital-to-analog converter (DAC) VNCOMP. The output is a positive voltage pulse with Vlow 0V and Vhigh 1.8V. Due to mismatch the differential amplifier in the comparator is not totally symmetric. This results in a threshold mismatch to the value set by Vth. A compensation mechanism is implemented in AstroPix4. It consists of a 3bit current DAC which can be tuned to make the tail currents in the differential stage equal.
The following stage is an open drain nfet. This nfet converts the positive pulse to a negative pulse. The source of the nfet is connected to Vminpix(normally 0.7 - 1V), which reduces the signal amplitude to 0.8- 1.1V. In the hitbuffer of every pixel, the signal is converted back to the full amplitude, with a pmos common source amplifier. The output signal is a positive pulse with a fast rise time and a fall time which is determined by the discharge current VNREC. This circuit also incorporates the pull up current source VPREC.

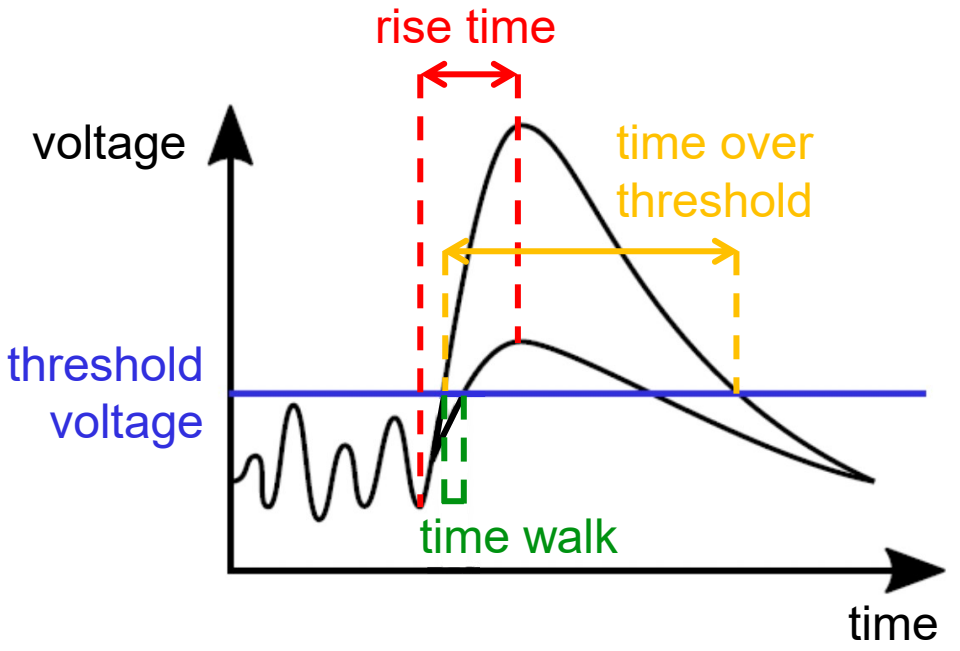
AstroPix4 Summary

- No identification problems with multiple hits in same row/col
- Improved timestamp resolution
- Threshold tuning
- Lower digital power
  - Chip level: Async ToT measurement with low duty cycle due to low rates
  - System level: No fast clocks needed anymore, no highspeed clock distribution
- Documentation

- Some ideas for v5:
  - Self tuning
  - ADC to digitize analog temperature sensor
  - Passive matrix for e-TCT

AstroPix4: Time Walk and ToT

- **Time walk:**
  - Rise time same for all signals
  - Difference in time at which threshold is crossed is called time walk
  - Time walk ~ 20 ns
    - can be corrected with ToT information
- **Time over Threshold:**
  - 1 µs to 30 µs



Schematic description of time walk, rise time, and time over threshold

Power consumption TDC + PLL + DLL

- Hitbuffer with TDC
  - Active: ~700 uW
  - Idle: 50-100 nW
- 20 MHz PLL + DLL: ~240 uW
- Based on hitrate studies:
  - Average 0.008 Hits/s per 500um Pixel
  - For 35x35 Pixel **2cmx2cm Chip**: 35*35*0.008 Hits/s **~10 Hits/s**
- Implications on duty cycle
  - TDC duty cycle D for max. $\frac{10}{1s} \cdot 2 \cdot 50\ ns = \frac{1000\ ns}{1\ s} = 10^{-6}$
- **Avg. power per Chip for ToT**: . $\frac{0.7\ mW \cdot 1\ us + 35 \cdot 35 \cdot 100\ nW * 999.999\ ms}{1\ s} = \mathbf{121\ uW}$ i.e. **360uW incl. PLL and DLL**
- **For comparison LVDS-Receiver in v2/v3 for 200 MHz clock alone consumes 1 mW!**