AstroPix Test Results

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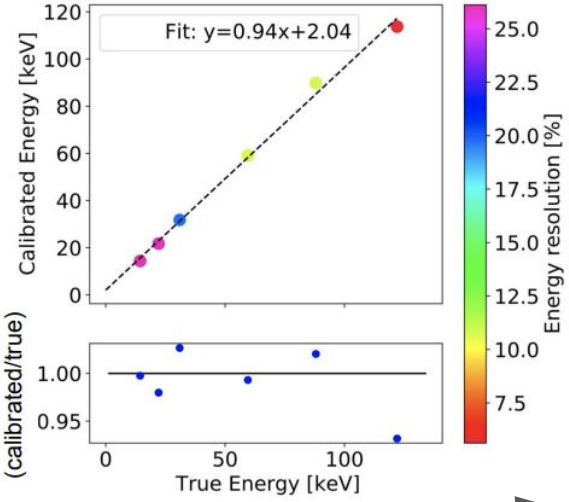
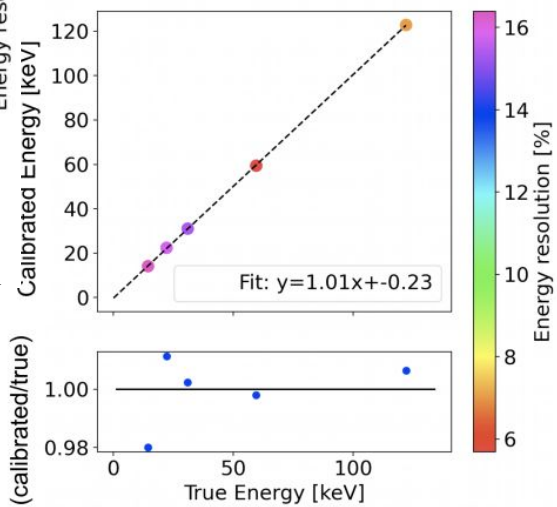
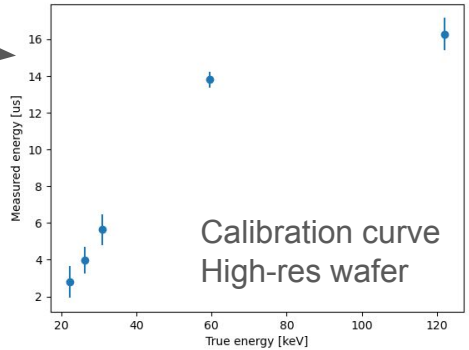
16 June 2023
ePIC Imaging Barrel Calorimeter Meeting

Publication history

- ATLASPix
  - https://arxiv.org/abs/2101.02665
  - https://arxiv.org/abs/2109.13409
- AstroPix_v1 (analog data)
  - https://arxiv.org/abs/2209.02631
- AstroPix_v2 (analog data)
  - https://arxiv.org/abs/2302.00101
- AstroPix_v2 (digital data)
  - Upcoming IEEE proceedings
- A-STEP, utilizing AstroPix_v3
  - Upcoming ICRC proceedings

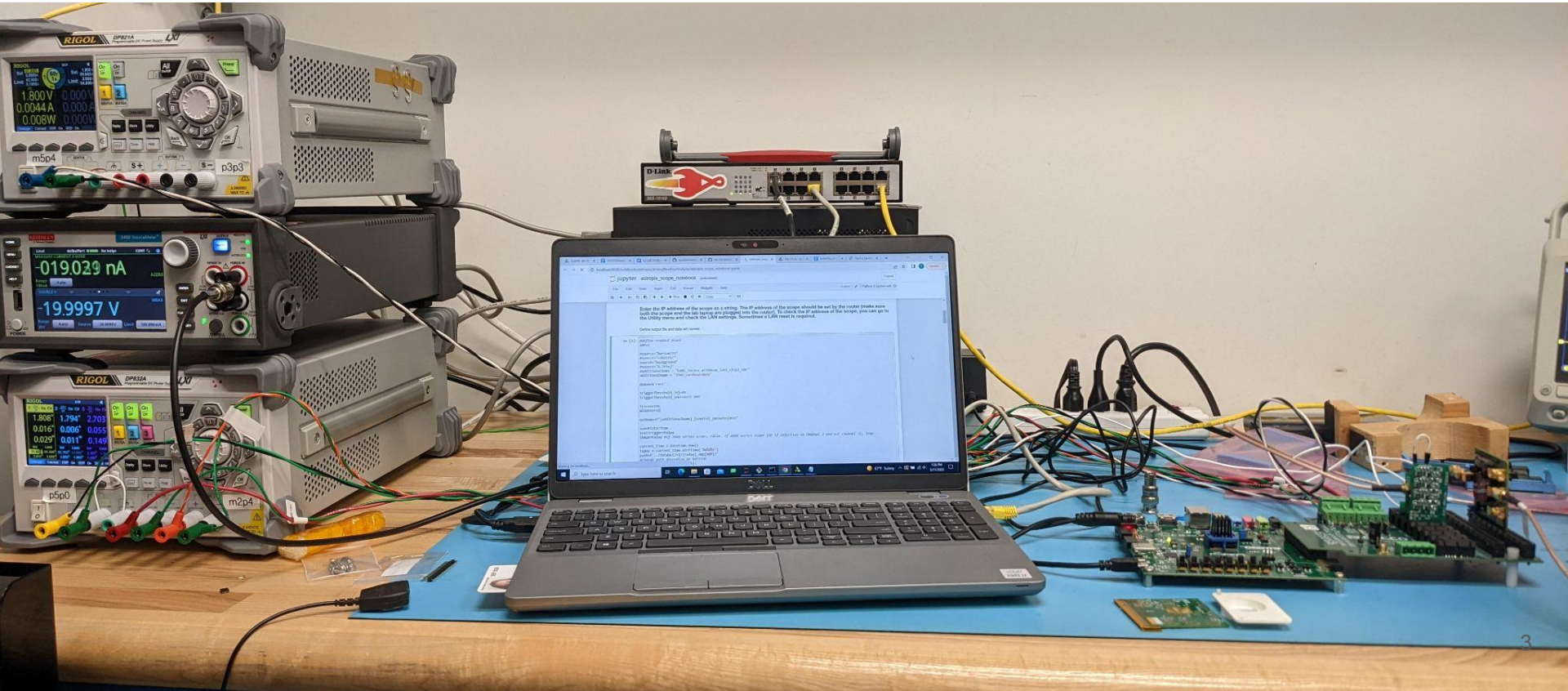




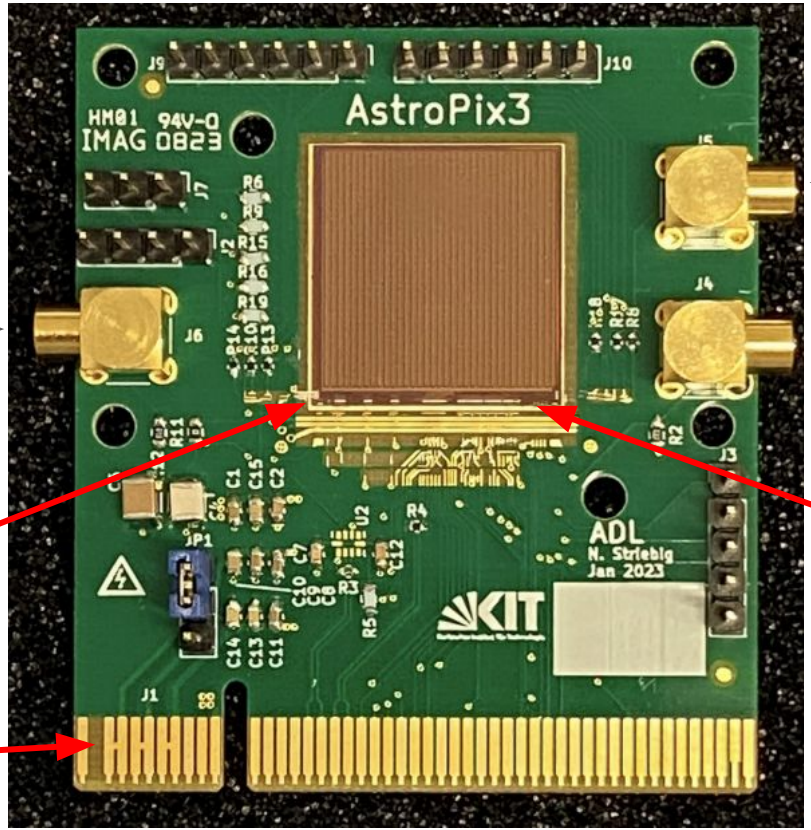


Incremental changes stepping from ATLASPix to benchmarked AstroPix

GSFC Bench


RIGOL
DP821A
1.800 V
0.0044 A
0.008W
m5p4
p3p3
-019.029 nA
-19.9997 V
RIGOL
DP832A
1.808
1.794
2.703
0.016
0.006
0.055
0.029
0.011
0.149
p5p0
m2p4
D-Link
jupyter
astropix_scope_notebook

Chip PCB



200 MHz sample clock

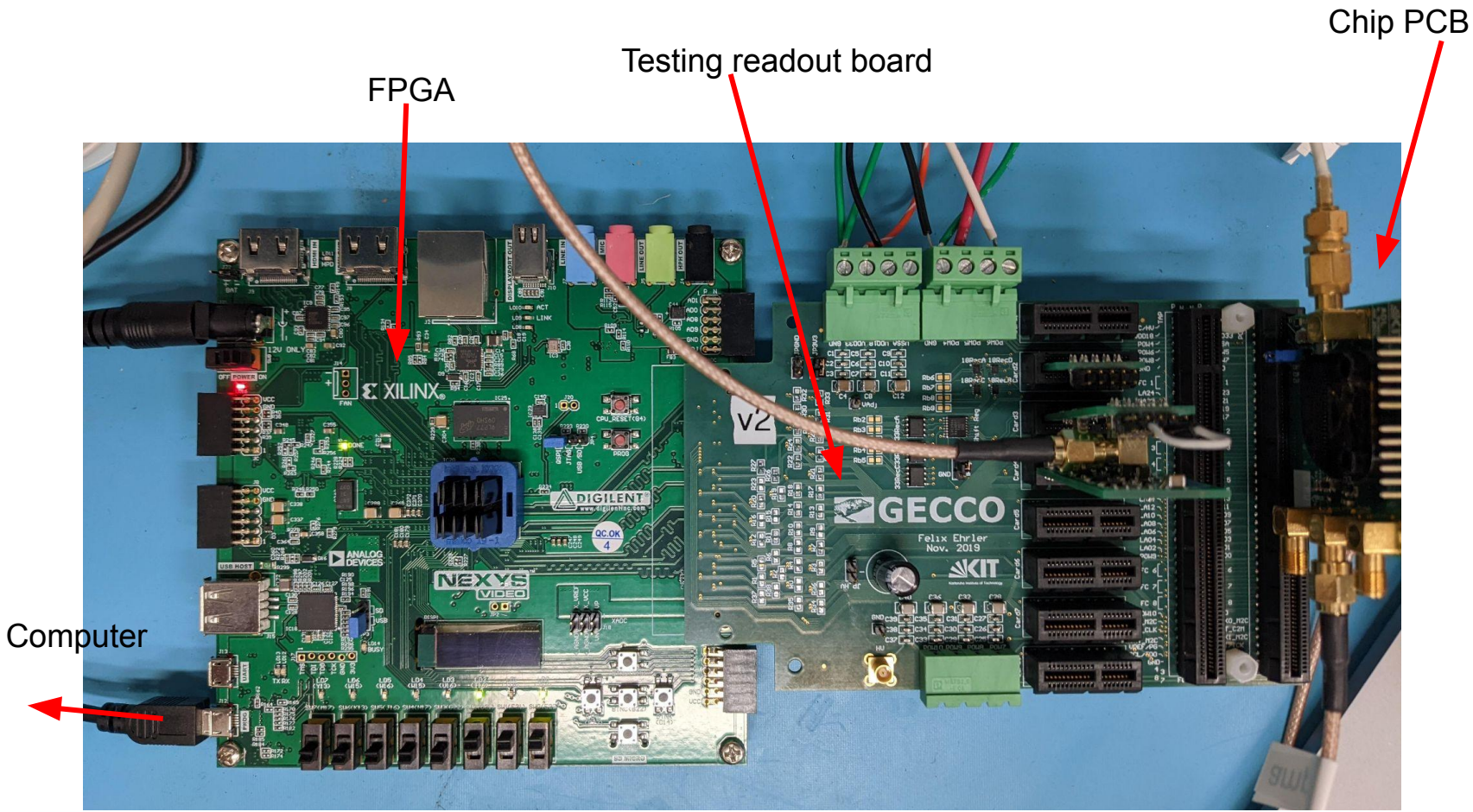
High-voltage bias

Output analog signal

Wire bonds for power and IO

Digital periphery, “digital top”

Connection to testing readout board


Chip PCB
Testing readout board
FPGA
Computer
XILINX
DIGILENT
GECCO
Felix Ehrler
Nov. 2019
KIT
NEXYS
VIDEO
ANALOG DEVICES
v2

Testing Tools

Inputs

- Injected voltage
  - Voltage generated on chip or on board and delivered to individual pixel
- Radioactive sources
  - Focusing on 14-122 keV range for now
  - Have sources with lines up to 650 keV+

Outputs

- Analog data
  - Output of the charge-sensitive amplifier
  - Requires wiring directly to the pixel so limited to the 35 pixels in first row (near periphery)
  - For debugging
- Digital data
  - Fully digitized signal
  - Full array accessable

Disclaimer slide!

There are big design updates in store for v4
and for the final chip version for ePIC integration

These results all feature the newest fabricated chip, v3

Not all configuration/results will be directly projectable

Non- projectable v3 specific features indicated with 

v3

Digital Data

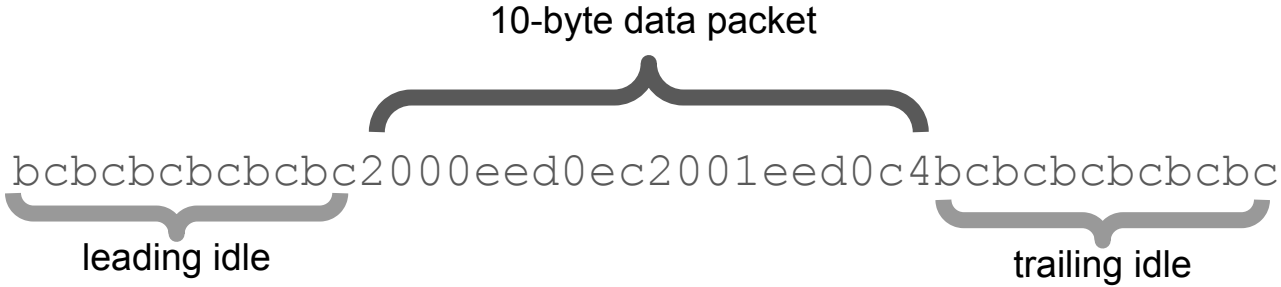
DIFFERENT DATA STRUCTURE IN V3 THAN IN V4

- OR row and column information to only two channels (row, col) are sent to digital top
  - Pixel array acting like strips
- Encoded digital information:
  - ChipID - relates chip to location in daisy chain
  - Payload - relates to SPI line
  - Location - row or column with comparator that measured over threshold
  - Timestamp - 8bit value counted with 2 MHz clock
  - isCol - boolean for row or column
  - LSB, MSB, ToT - time over threshold value, converted to us offline given clock speeds
- Each hit (row or column data packet) = 5 Bytes
- A “good event” requires:
  - One row and one column packet in same readout stream
  - Matching timestamp
  - No ToT matching requirement at GSFC

v3

Example data

Chip returns bitstreams :

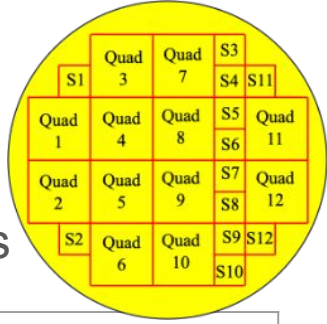


Which encode info:

Chip ID	payload	location	isCol	timestamp	tot_msb	tot_lsb	tot_total
0	4	0	False	119	11	55	2871
0	4	0	True	119	11	35	2851

v3

V3 substrates



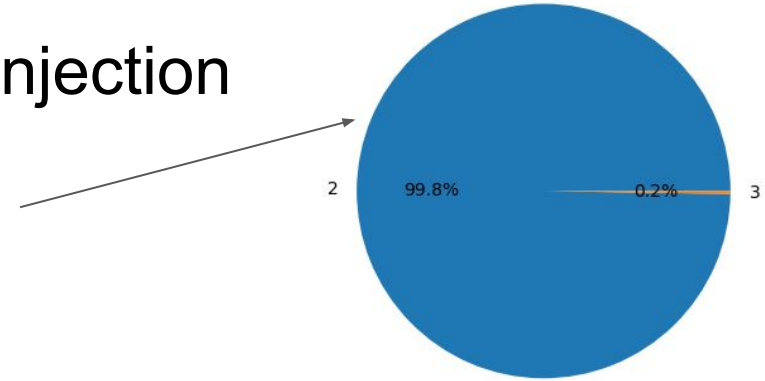
Fabricated chips (single chips and quad-chips) using 3 different substrates

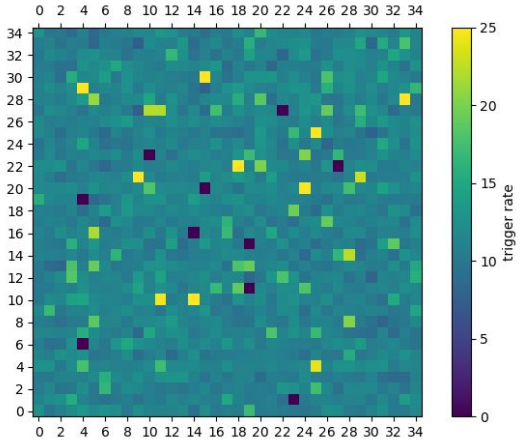
	TSI Substrate	Okmetic Substrate	Topsil Substrate
Purpose	Testing	Backup	Flight
Resistivity [Ω*cm]	50	300-400	10,000
Number of wafers	2	2	3
Diced and mounted on test board?	Yes	No (in progress)	Yes
Breakdown voltage [-V]	250	290	High leakage current (uA) with any applied voltage
Leakage current, -150V [-nA]	40	40	High (80mA at -30V)
Testing notes	Low-quality substrate, high pixel variability	Tested on wafer, sent for dicing	Challenging - will explore in a bit

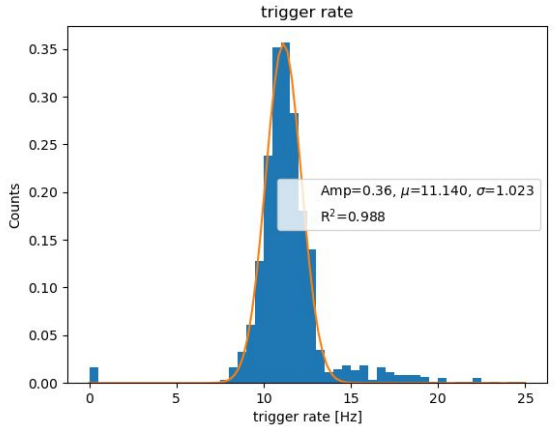
TSI (low-resistivity) v3 response to injection

v3

- 99.8% of readout streams measure two hits - one row and one column
- Pixel scans
  - Enable one pixel at a time
  - Inject a 300 mV square wave (~12 Hz) for 30s into each pixel individually
  - Default 100 mV comparator threshold
  - Plot “good events”

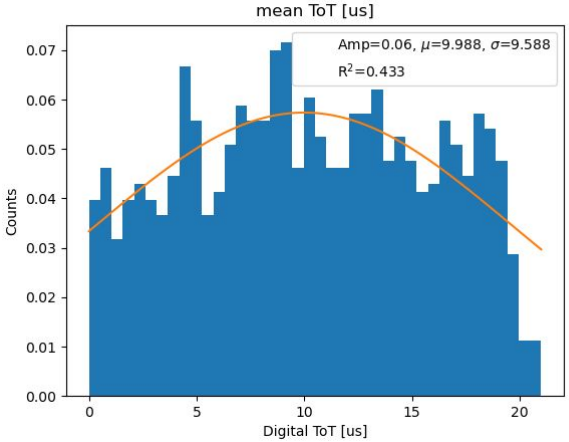


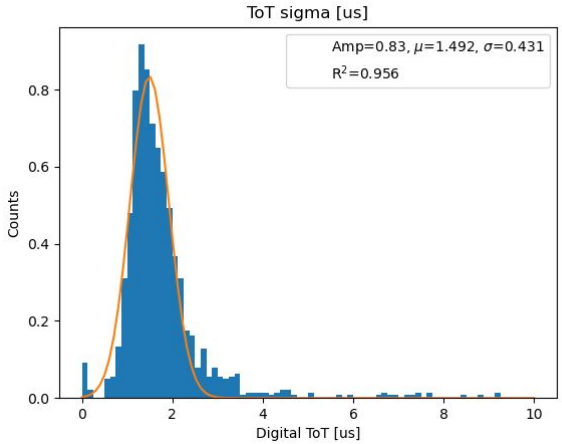


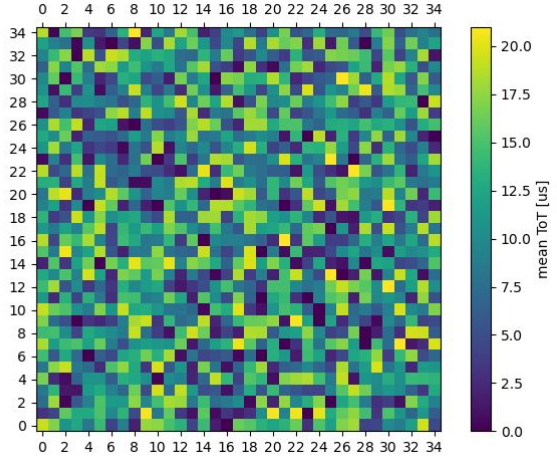


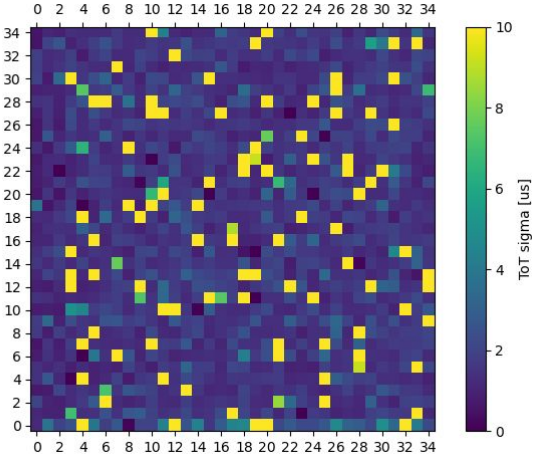
Mean trigger rate discrepancy possibly from DAC settings (configuring amplifier bias/load current, comparator bias, etc) not yet being optimized for v3

ToT response from pixel scan 0.3V injection









- Pixels do not respond uniformly
  - Poorly fit mean ToT value in histogram of mean pixel ToTs
  - Will require individual pixel calibration
- Some pixel ToT spectra are poorly fit with large sigma values
  - Average energy resolution ~ 35%
  - Remember configuration settings aren't optimized yet!

Active and previous work at GSFC

v3 WIPs

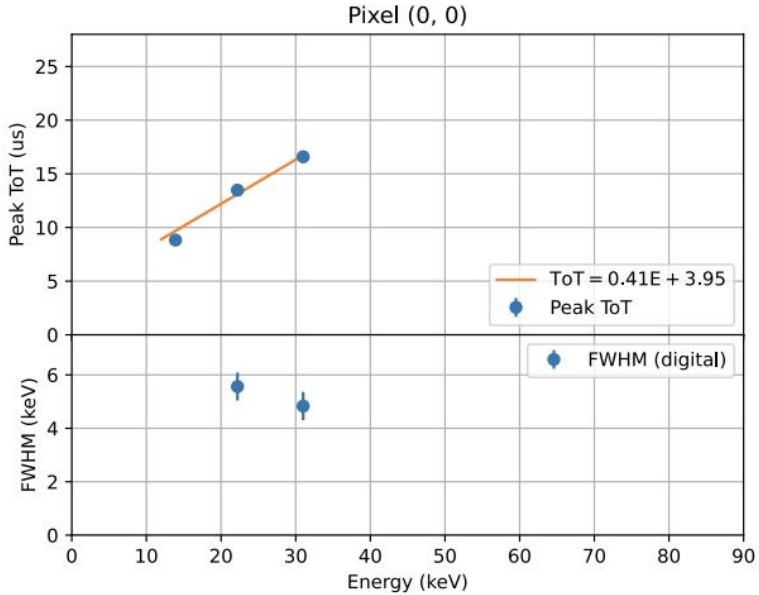
- Determine utility of high-resistivity chip
- Configuration setting optimization
- Pixel variation studies with radioactive sources rather than injections
- Train an undergraduate summer intern
- Software development and maintenance - https://github.com/astropix
  - Please contribute and let me know if things break!

Repeatable v2 Studies

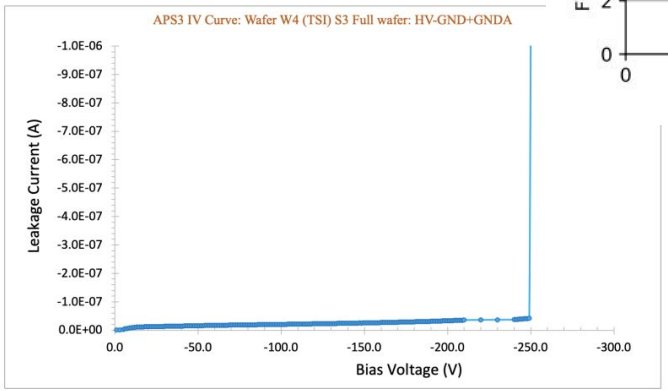
- Pixel-by-pixel digital threshold optimization (S-curve creation) and consequent global threshold setting
- Noisy pixel identification and masking
- Single-pixel energy calibration
- Full (masked) array running

AstroPix_v3 testing outside of GSFC

- v3 digital calibration
  - First results from collaborators In Japan
  - Low-resistivity chip, single pixel
- IV and CV curves for all wafer substrates
  - Diagnostic tools from ANL
  - Low-resistivity TSI Substrate
- Power measure-ments
  - Test and simulation by chip designers at KIT

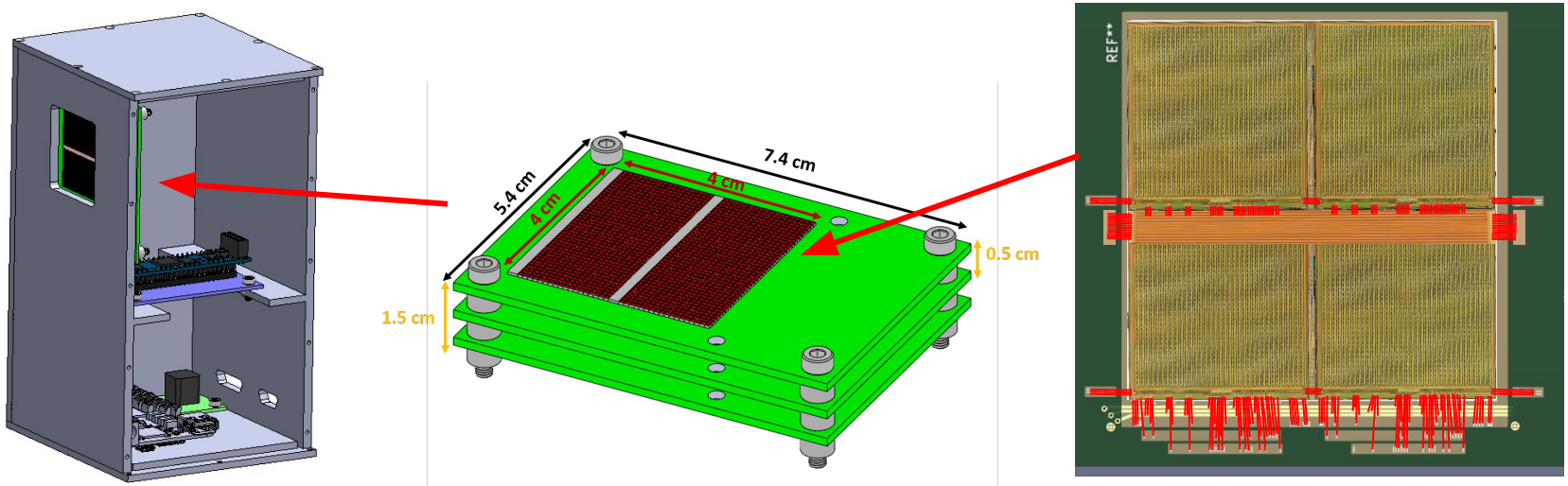


Full Wafer W4S3 - TSI substrate



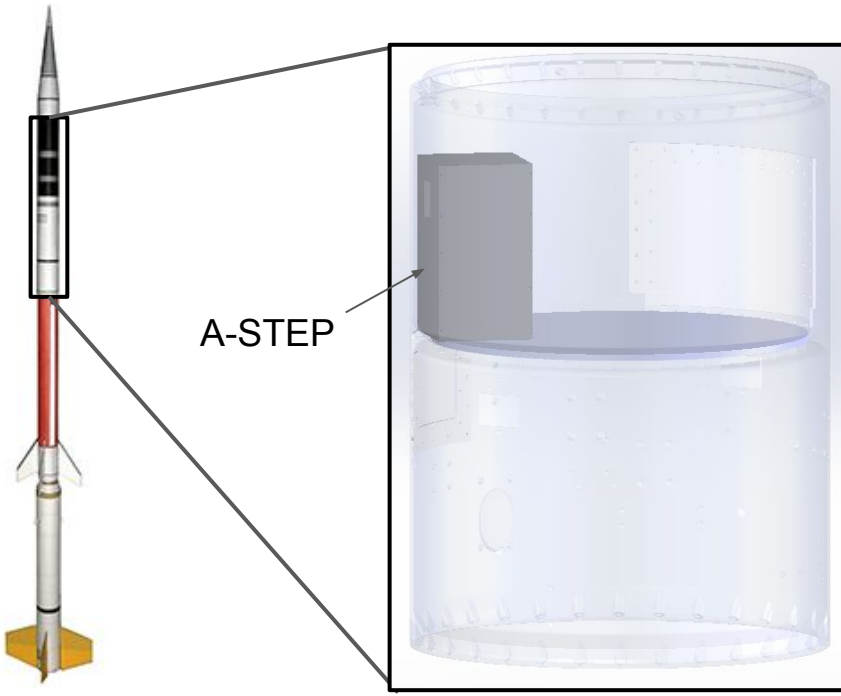
A-STEP and v3

- A-STEP mission objective = Raise technical readiness level (TRL) of AstroPix quad-chip for future use in AMEGO-X
  - Validate operation of v3 quad-chip in space environment on sounding rocket
- AstroPix_v3 is a flight chip to be used on A-STEP
  - Use tools developed while playing around with v3 to create a structured v3 test program



Work to be done for A-STEP

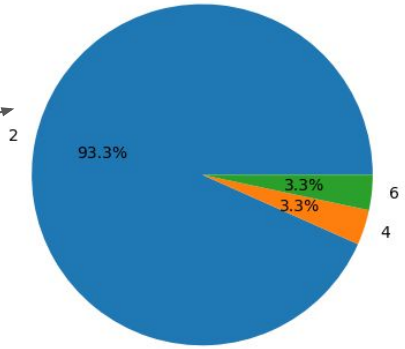
- First flex bus bar designed to connect upper 2 chips in quad chip
- First test of chip daisy-chains
- Scaling of firmware to handle multiple chips / multiple layers
- Mechanical testing of wire bonds, support structure (windowpane-like supports, not solid PCB)
- Flight software for data packetization and telemetry (new sophistication to DAQ)
- Eventual environmental testing of full system
    - Vibration, temperature/vacuum, etc



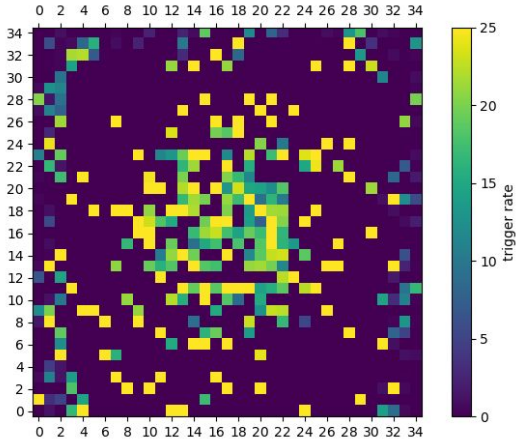
Backup

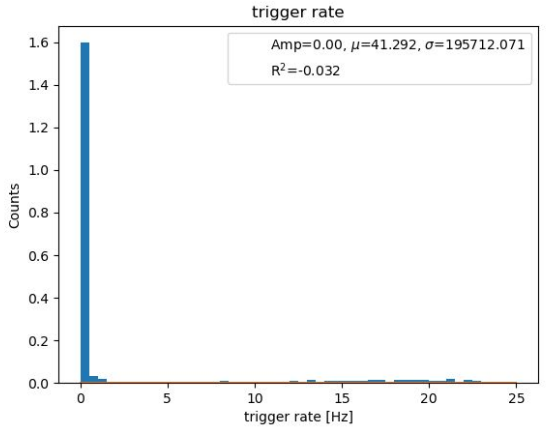
Topsil (high-resistivity) v3 response to injection

- 93.3% of readout streams measure two hits - one row and one column
- Pixel scans
  - Enable one pixel at a time
  - Inject a 300 mV square wave (~12 Hz) for 30s into each pixel individually
  - Default 100 mV comparator threshold
  - Plot “good events”



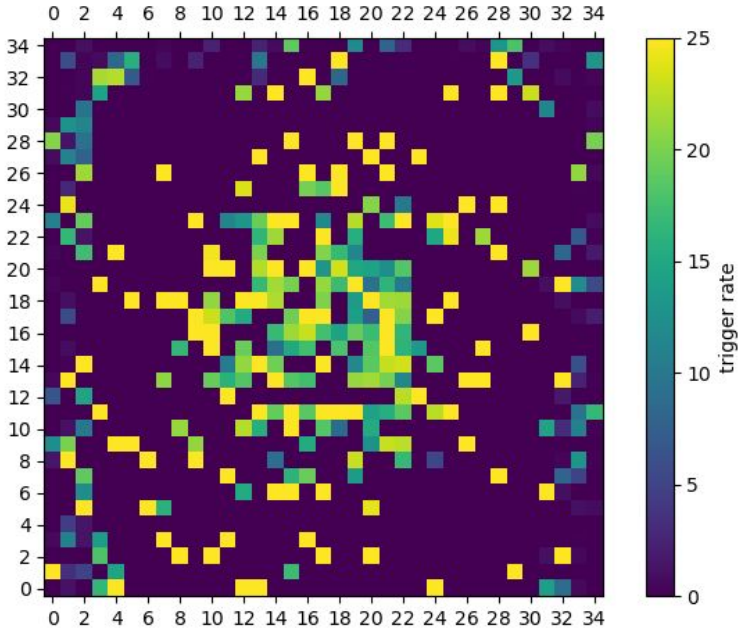
Geometric pattern of pixel sensitivity, currently under investigation



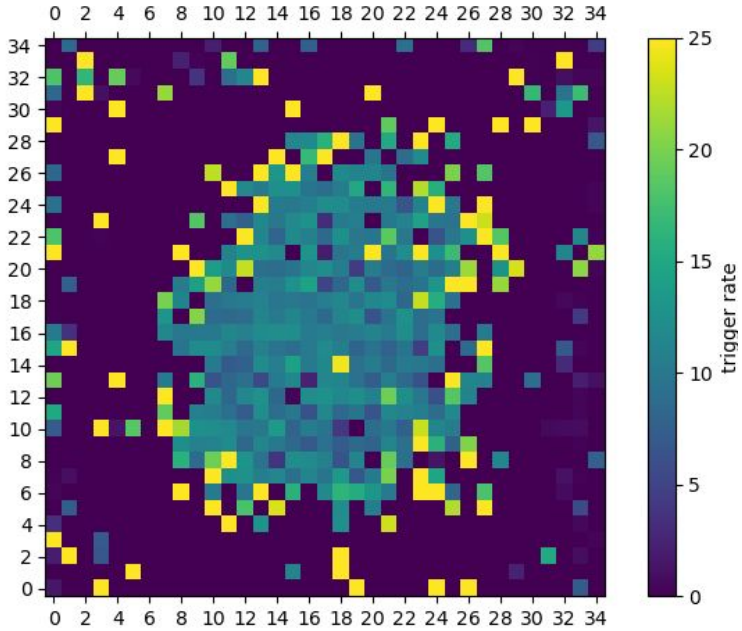


Investigating the high-resistivity wafer - 0.3V injection

100 mV digital threshold
(same as last slide)



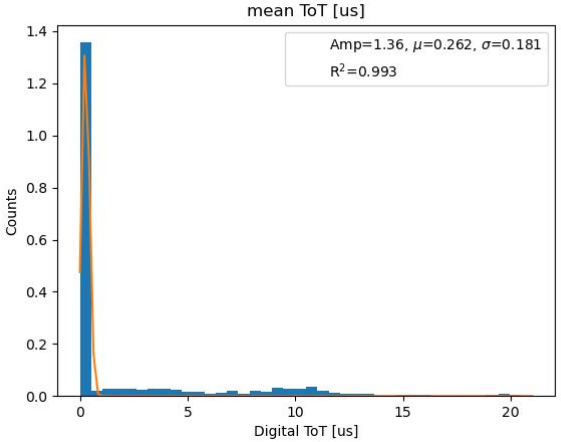
300 mV digital threshold

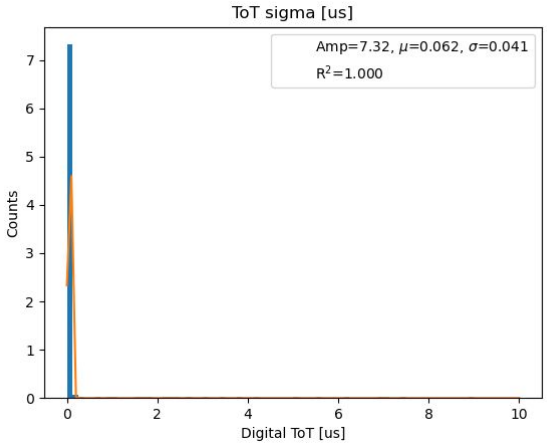


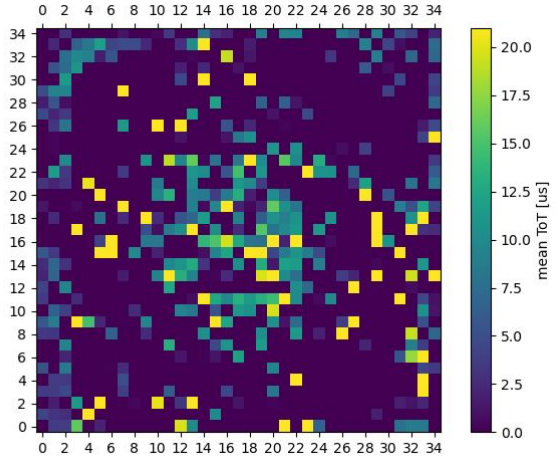
- Increasing the threshold decreases sensitivity to low-energy particles
- 300 mV threshold improves data quality
  - More pixels record data around the expected rate of 12Hz
- This high threshold cannot revive pixels
- Geometric effects still exist

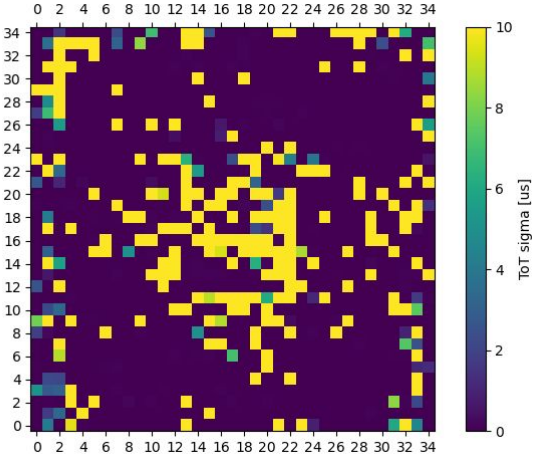
v3

ToT response from pixel scan 0.3V injection, W10S06









- High-resistivity wafer
- Pixels do not respond uniformly geometrically
  - 48% report no data
  - 18% have no good events
  - Remaining hits span full ToT spectrum
- Pixels that do measure ToT spectra return poorly fit data with large sigma values
- Using same un-optimized configuration settings as pixel scan with low-resistivity wafer W02