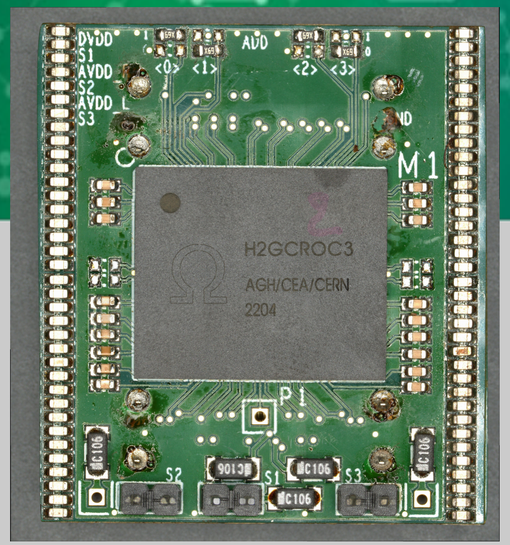
Barrel ECal Front End Readout

Norbert Novitzky
(ORNL)



ORNL is managed by UT-Battelle LLC for the US Department of Energy

H2GCROCv3 architecture

Overall chip divided in two symmetrical parts:

- One half is made of:
  - 39 channels (in CMS 36 channels, 1 Calib, 2 CMN)
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2 trigger, 1 data)

Measurements:

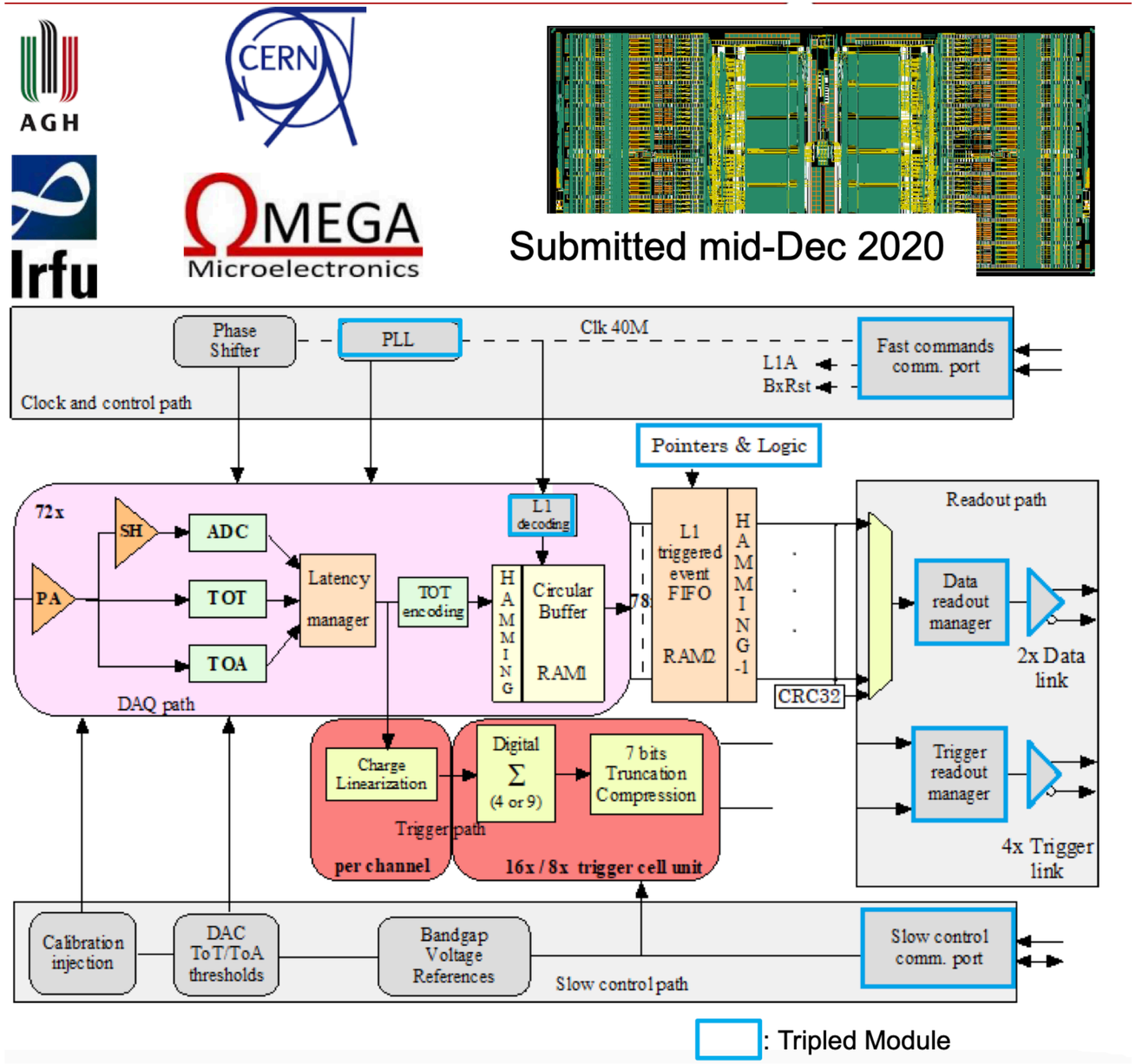
- Charge:
  - ADC peak measurement, 10 bits at 40 MHz, different gain setups possible, 0.4fC resolution
  - TDC: (Time over Threshold), 12 bits, 2.5fC resolution
- Time:
  - Time of arrival, 10 bits (25ps)

Data flow:

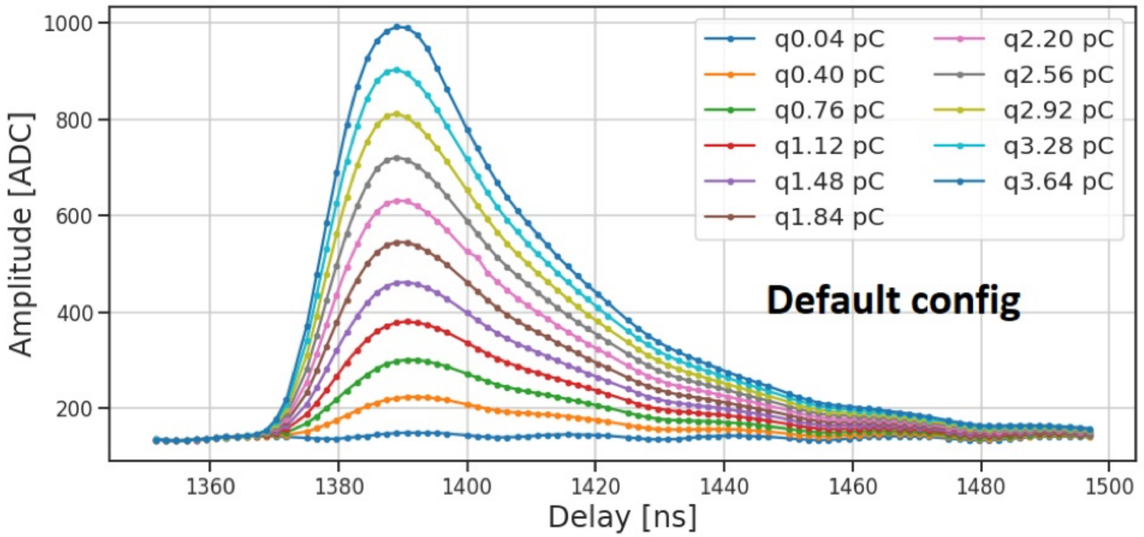
- DAQ path:
  - 512 dept RAM1, circular buffer
  - Secondary RAM2, 32 dept
  - Store all channel data, ADC, TOA, TOT
  - Output 2x 1.28 Gbps links
- Trigger path:
  - Sum of 4 or 9 channels, linearization, compression to 7bits
  - 4 x 1.28 Gbps links

Control:

- Fast commands, 40MHz and 320MHz clock
- I2C for slow control

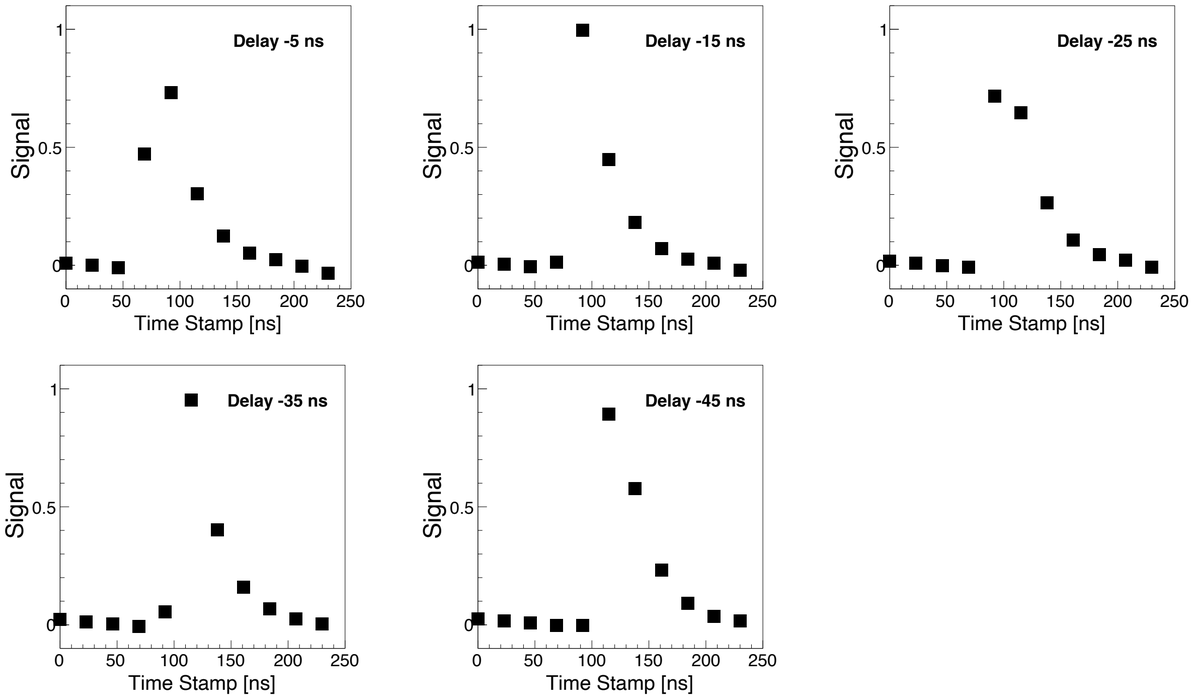


HGCROC use in EIC



Signal from the shapers:

- SiPM response of the H2GCROCv3 (from CMS)
- Default configuration used

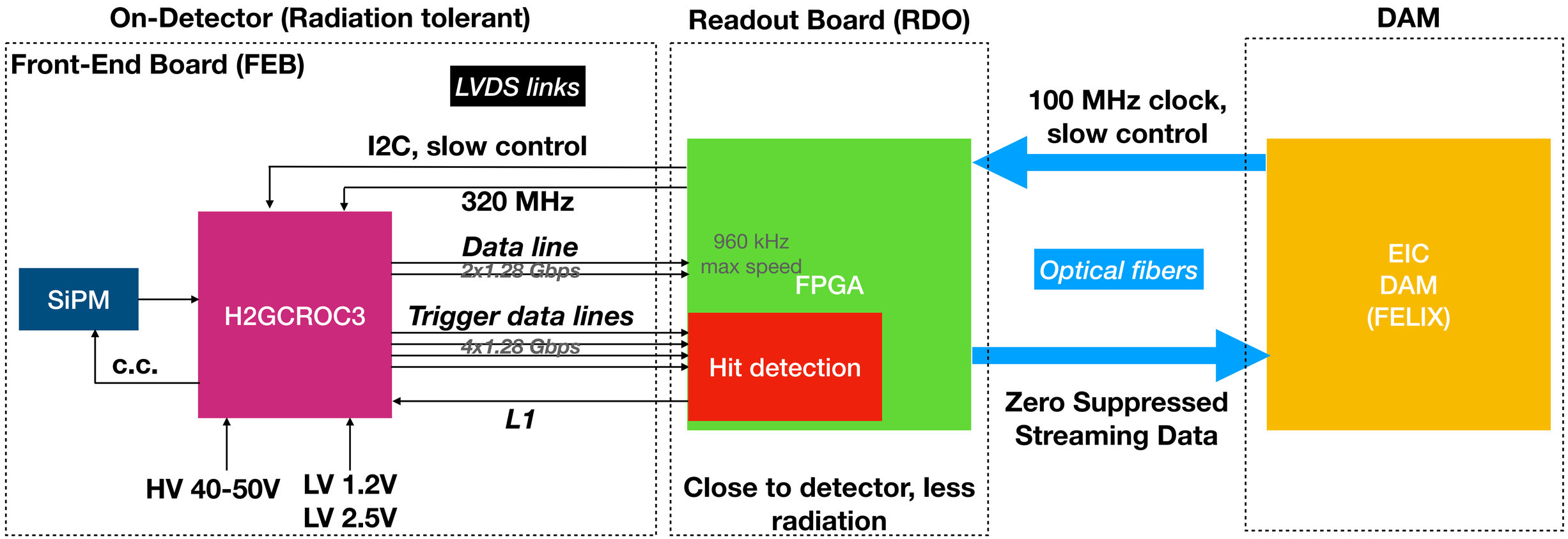


There are 5 different phases of the signal sampled with the 40 MHz clock:

- The new version of the H2GCROCv3 can read out multiple consecutive bunch crossings
- For good signal reconstruction, we plan to save 3 (or 4) samples for each signal
- Total: 3 ADC, 3 TOA and 3 TOT values, 32bitx3 words for each physics signal

We can reconstruct the phases (using TOA) and the shower shape (ADC+TOT template fit) for the EIC 100 MHz clock

LFHCal readout hierarchy (as of now)



Data propagation from the detector to the EPIC DAQ system:

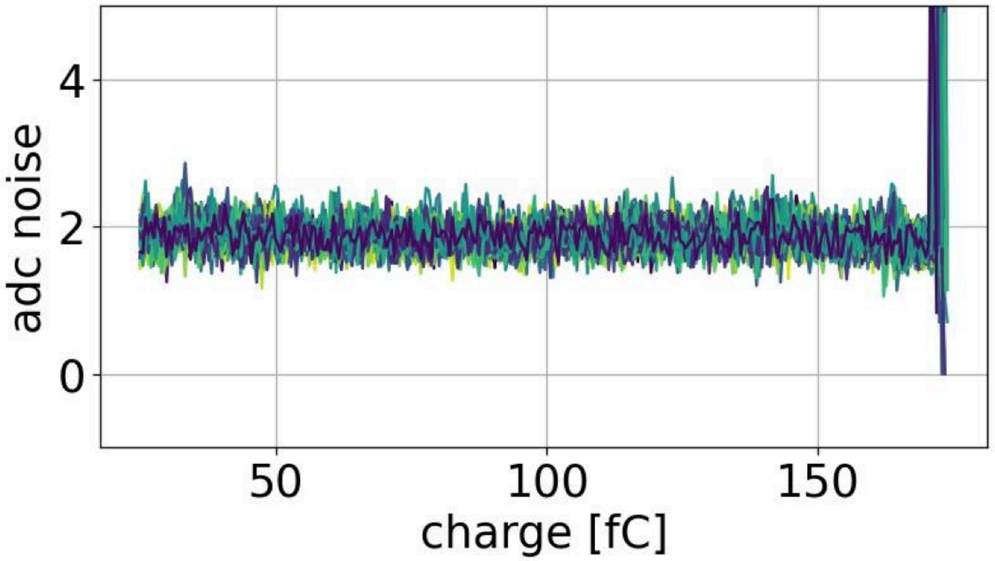
- The H2GCROC3 requires the L1 trigger for readout, with the maximum speed of 960 kHz
- The expected hit rate in **one channel of LFHCal** is up to 50 kHz:
  - With possible 4 sample readout we would reach a maximum of 200 kHz
  - Streaming readout towards the EPIC DAQ system

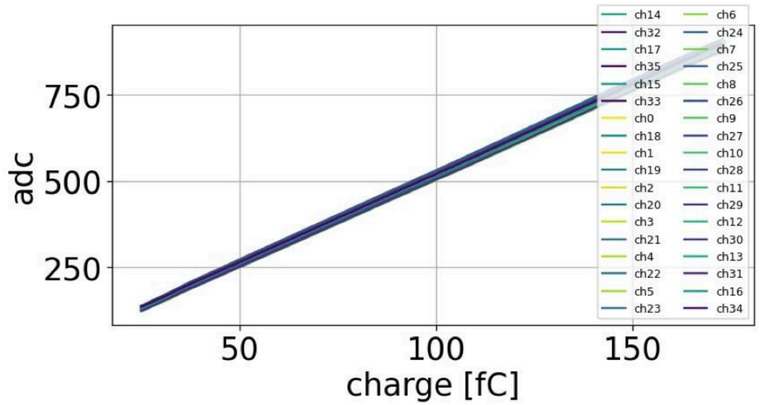
ADC data and noise

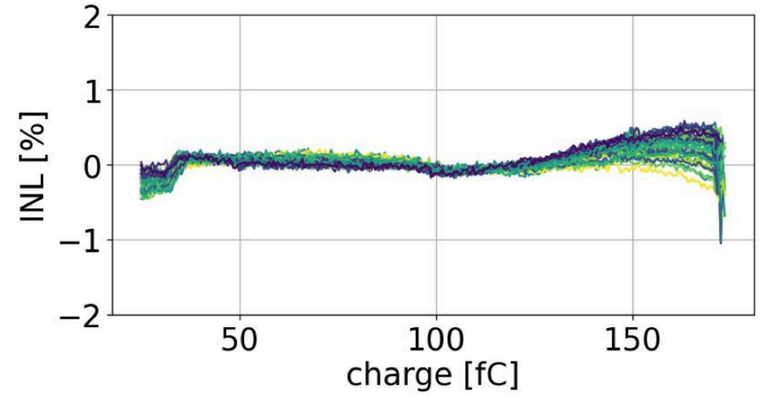
Two 10-bit DAC to globally set the pedestal to desired level (minimum)
5-bit reduce the dispersion from individual channels

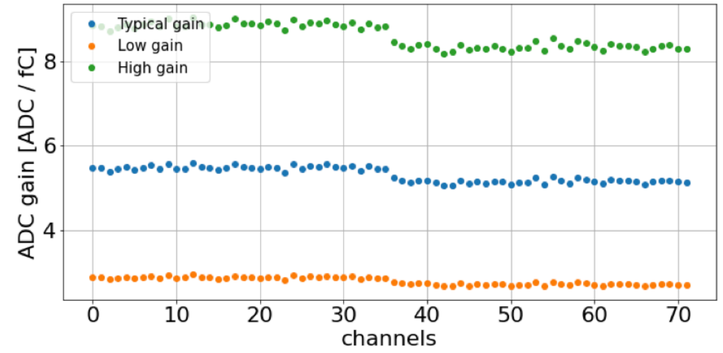
Very good linearity < 1%
- 1.6 fC linearity (~1 MIP) for the typical gain

0.3 fC resolution on 50 pF input capacitor







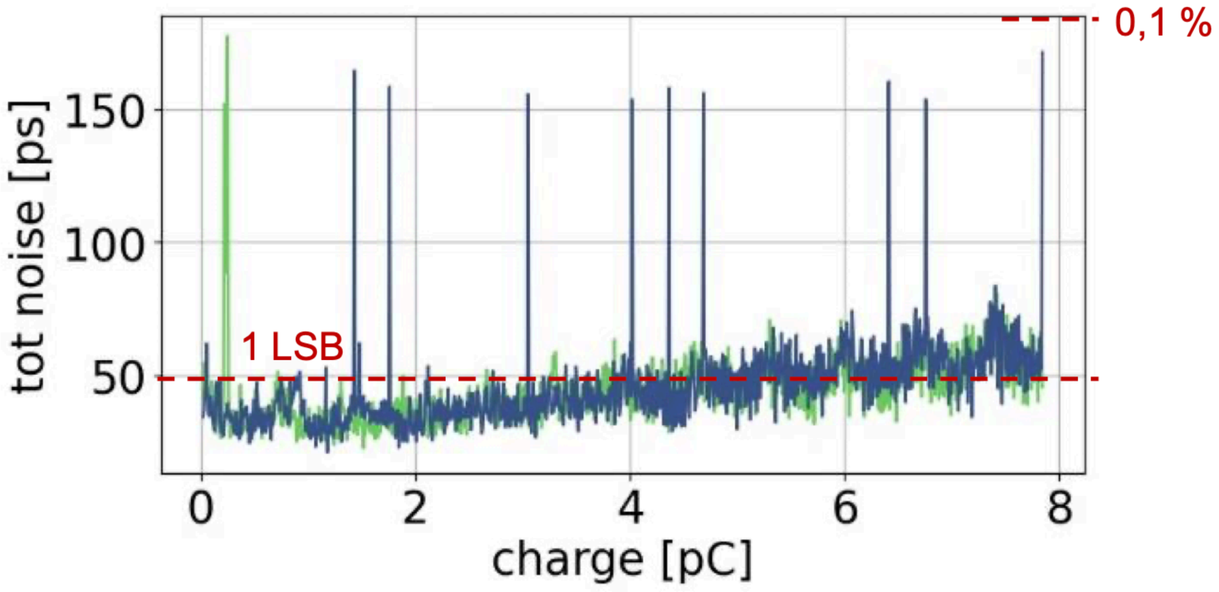


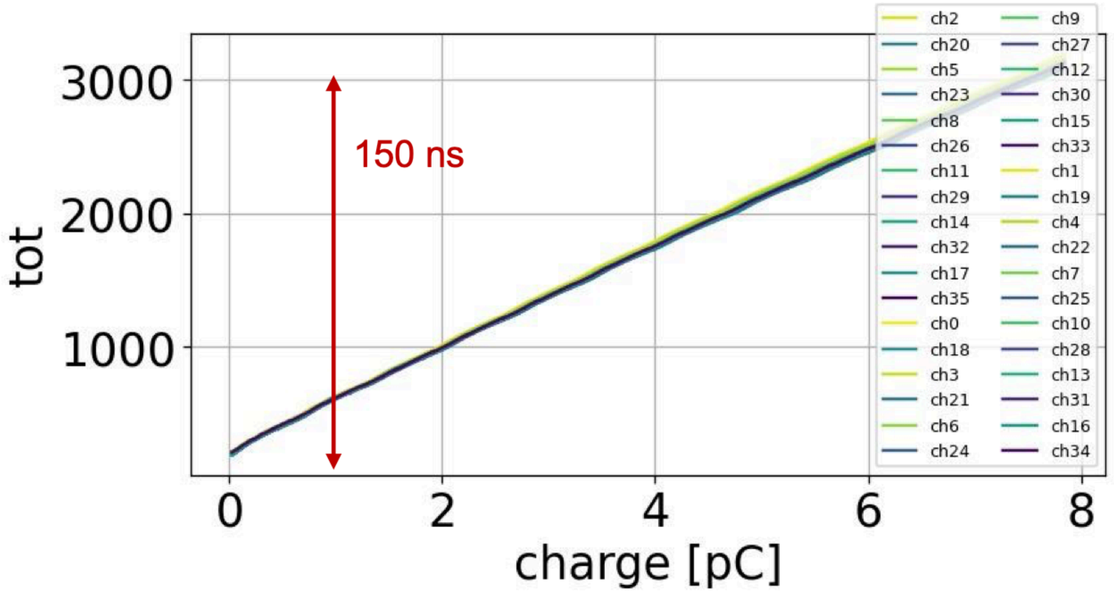
TOT data

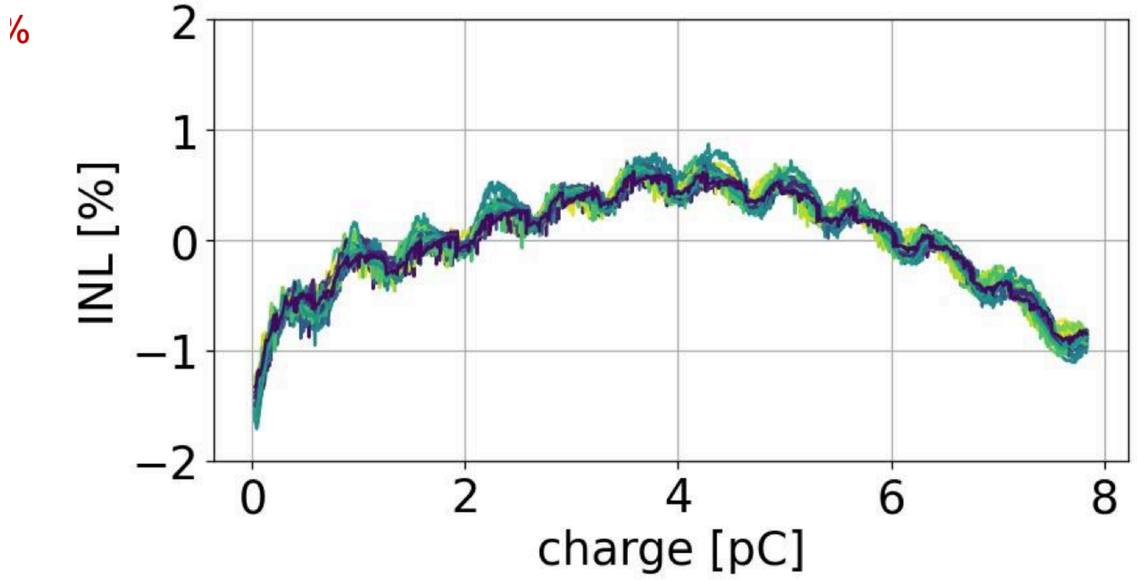
Once the ADC is saturated, the TOT takes over:
Range in silicon is 160 fC to 10pF, in SiPM 16pC to 320pC
50 ps binning

Very good linearity in the ToT:

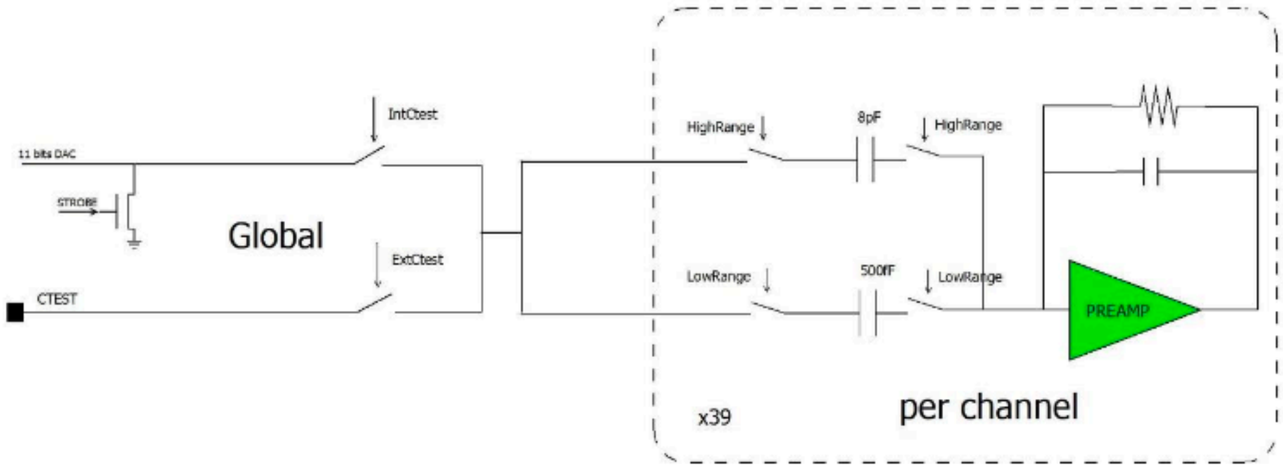
- 99.9% up to 200pC, 99% in full range
- Small residual wriggles on TOT from the digital noise on preamplifier input
- Resolution is about 50ps (the peaks are outliers which were fixed)







Internal Calibration Circuit



Internal Calibration circuit implemented in the H2GCROCv3:

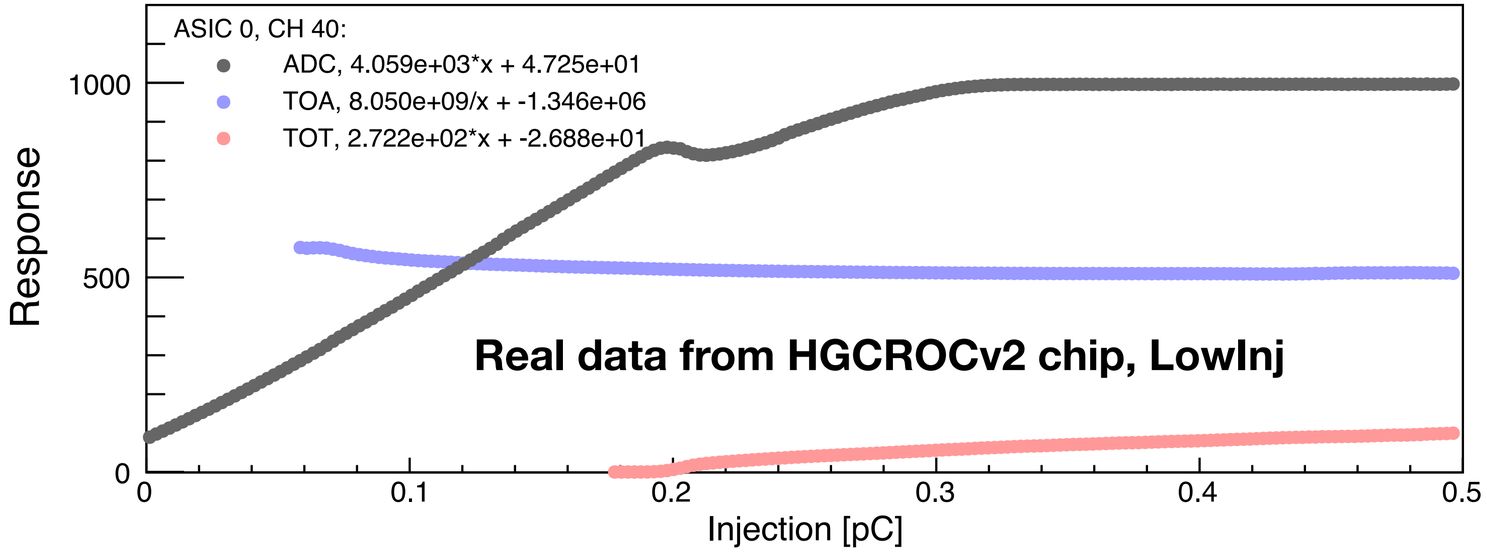
- Almost the full dynamic range. Reference voltage 0-1V:
  - 0.5 pF Low Range: 0 - 0.5 pC
  - 8 pF High Range: 0- 8 pC

Calibration circuit injection value of 11-bit:
Can be used to identify the thresholds for TOA and TOT, check linearity, etc.

Dynamic range of the HGCROC:

- Real data from the v2 chip
- Silicon variant
- ADC set to saturate around 850:
  - Small dip in the ADC happens when the TOT circuit comes online
  - TOT values are shown only to 100 (out of the 4095 range)
  - TOA have a small walk from threshold to 0.18 fC, then it is stable

We are currently working on the same data for the H2GCROCv3 chip



Before moving forward

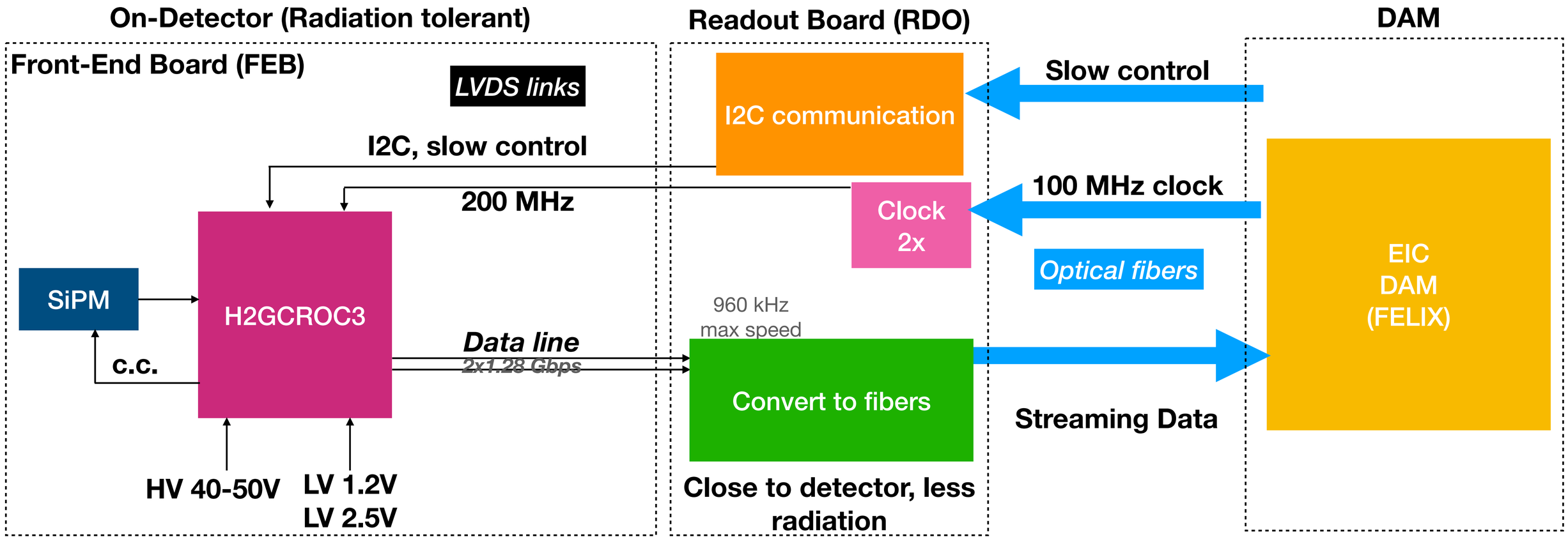
The Paris Omega team joined the ePIC/EIC effort:

- **Provide in-kind contribution to further development of the HGCROC3 to be applicable for the EIC use (link)**

Modifications considered:

- Self-triggering:
  - This will enable more streaming readout without the FPGA need
  - Reduce the services required for the trigger lines (1.28 Gbps lines)
- Clock change to EIC clock:
  - Change the clock provided from 320 MHz to 200 MHz. Internal clock of the sampling will be kept to 40 MHz
  - We can provide the 2x100 MHz EIC clock directly to the chip
  - Reduce the FPGA needed, we need to keep the I2C communication only
- Investigate the input capacitance range:
  - This could be also mitigated with an external circuit at the input

LFHCal readout hierarchy (after the upgrade)



Data propagation from the detector to the EPIC DAQ system:

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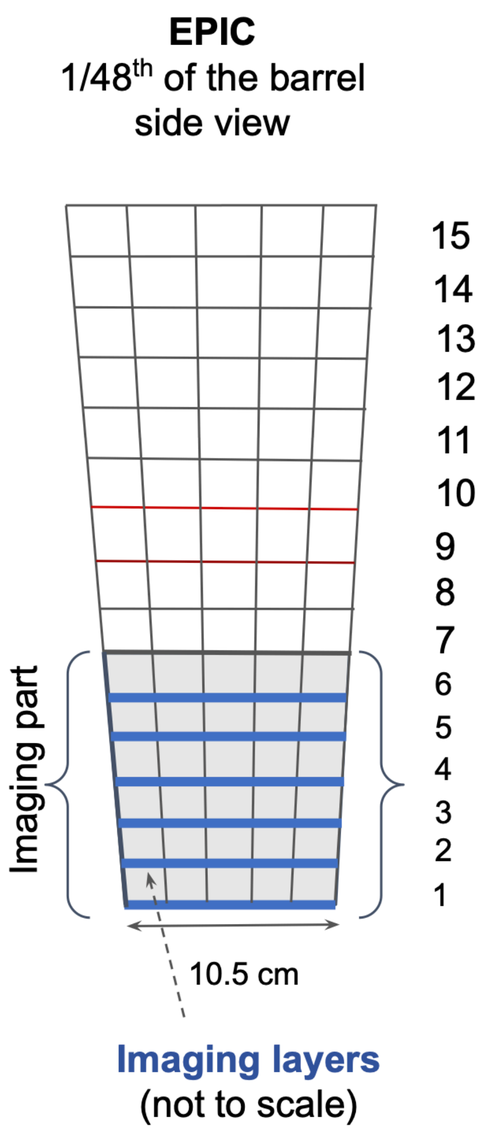
Going to the Barrel EMCal



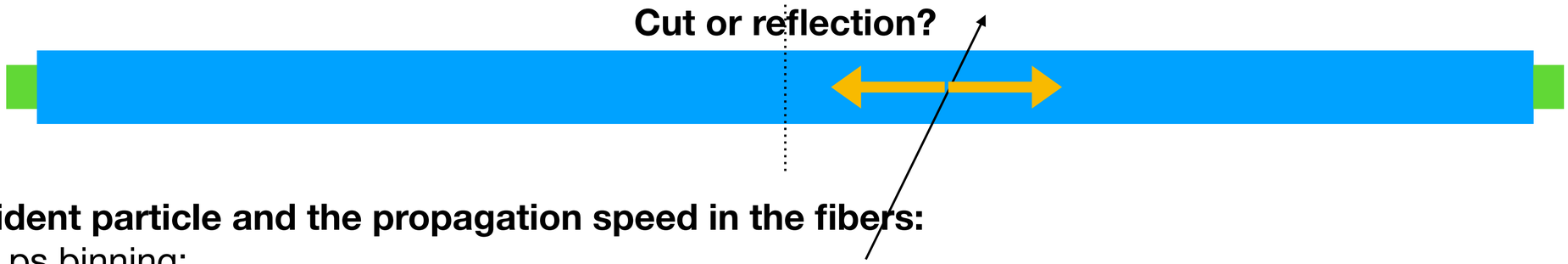
Considering each block will be readout as individual channel:

- 48 x 70 channel on either side = 3360
  - NO Summing - more info about showers
- Option 1: Maximum readout cross-wedges
  - 93 HGCROCs can handle it (9,300$)
- Option 2: Each wedge would be read by single HGCROC:
  - 96 HGCROCs would cover both sides (9,600$)
  - 200 W heat dissipation, half in either side
- One FEB currently with no modification to the HGCROC 1,000$:
  - All trigger lines are read out, etc. towards the “FPGA” (serviced can be reduced)
  - PCB is more expensive because of the BGA packaging 0.8 mm pitch (there is an 0.6 mm option)

FEB cost might be in order of 100k$, RDO’s we still are calculating without FPGA on it if possible

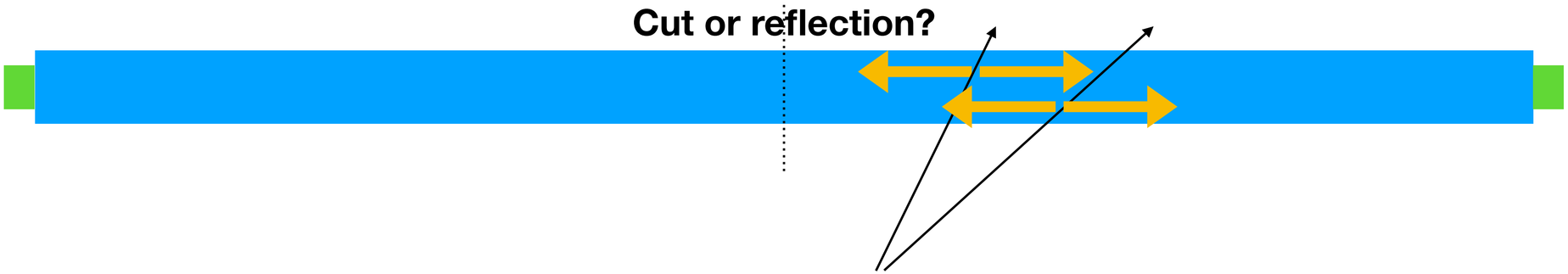
Considering KU060 or higher is at current HGCROC version is 32 HGCROC/1FPGA Max one would need 3-4 FPGA RDO’s, might be reduced to 0-1 if all the updates to the ASIC is done (1 FPGA board is now 15k$ with all components)

Timing and position resolution



Study the incident particle and the propagation speed in the fibers:

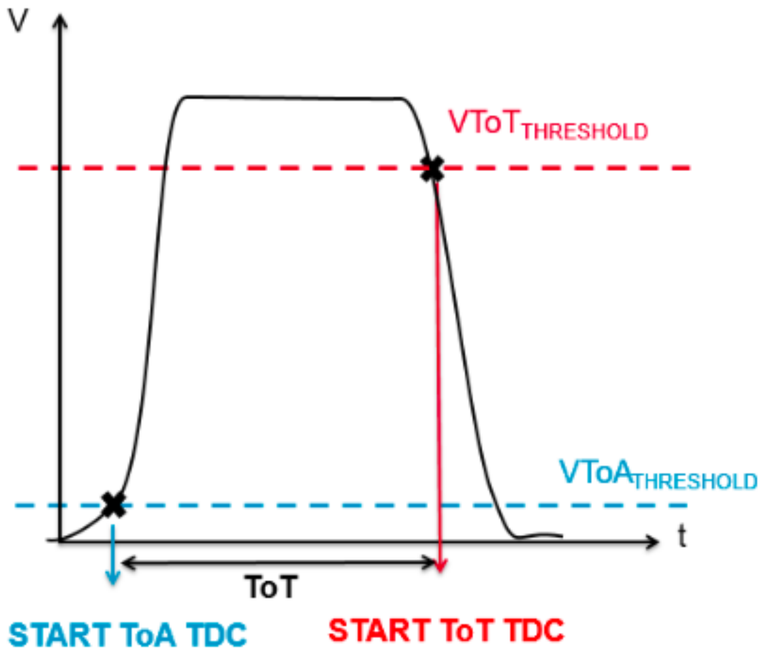
- TOA has 25 ps binning:
  - Possible resolution which was achieved is 15-35 ps
  - Speed of light in the fiber? (Usually it is 50-70%)
  - Counting on the resolution per channel it is about 3-7 cm position resolution

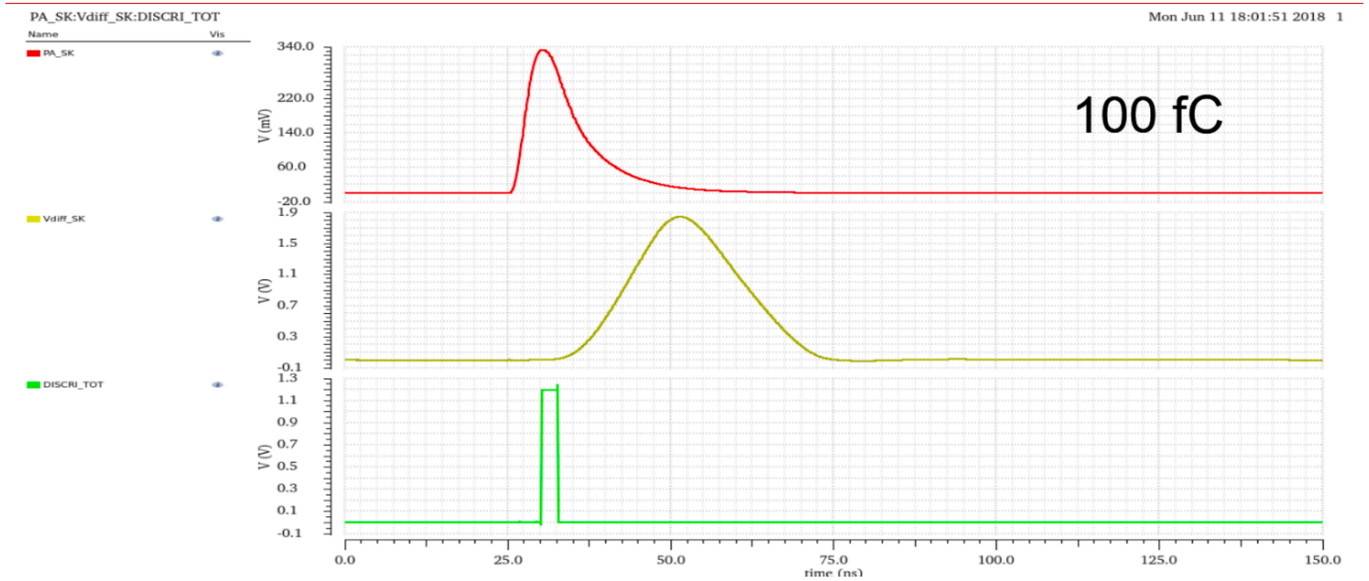


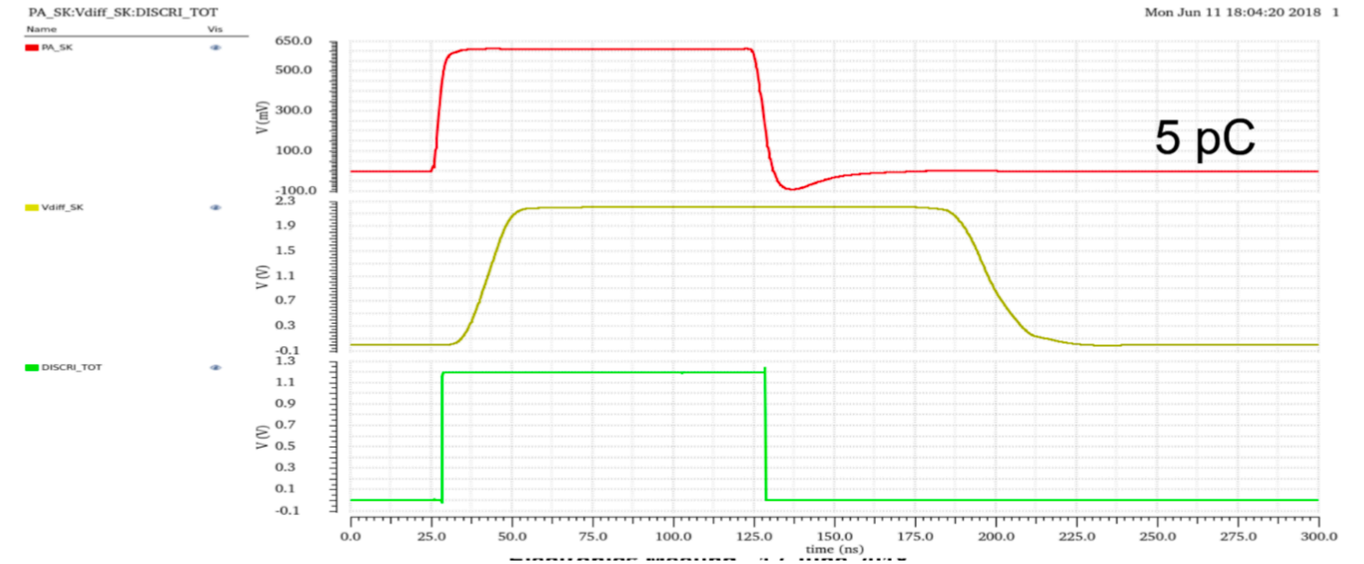
Double hits will be hard to distinguish:

- How often this happens? Considering to have a timing information in each channel, one could imagine to distinguish two showers.

Time of Arrival (TOA), Time over Threshold (TOT) in HGCROC





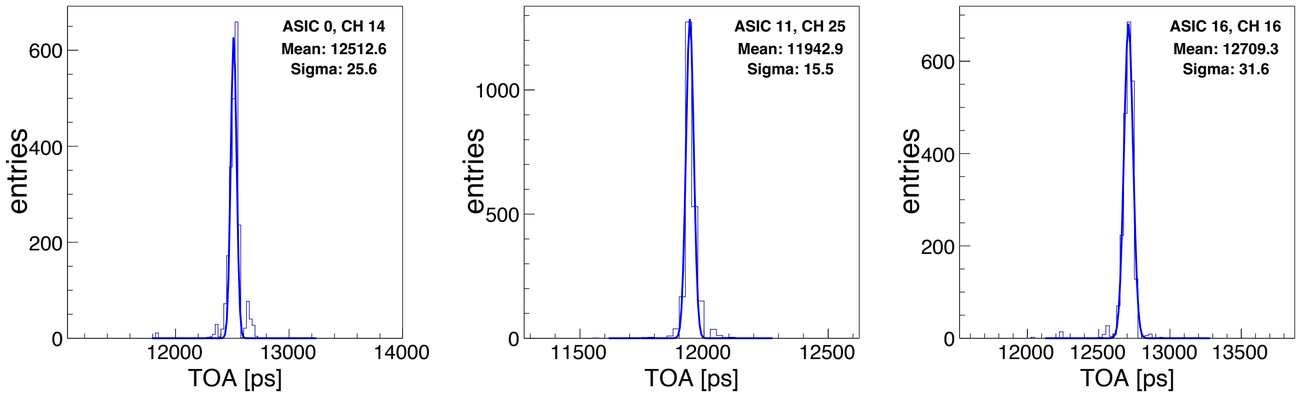


"Start" thresholds can be set for each channel:

- Two Global thresholds for each side of the ASIC
- Channel-by-Channel fine tuning for each channel

OAK RIDGE National Laboratory

Real measurement of the timing distribution in HGCROCv2



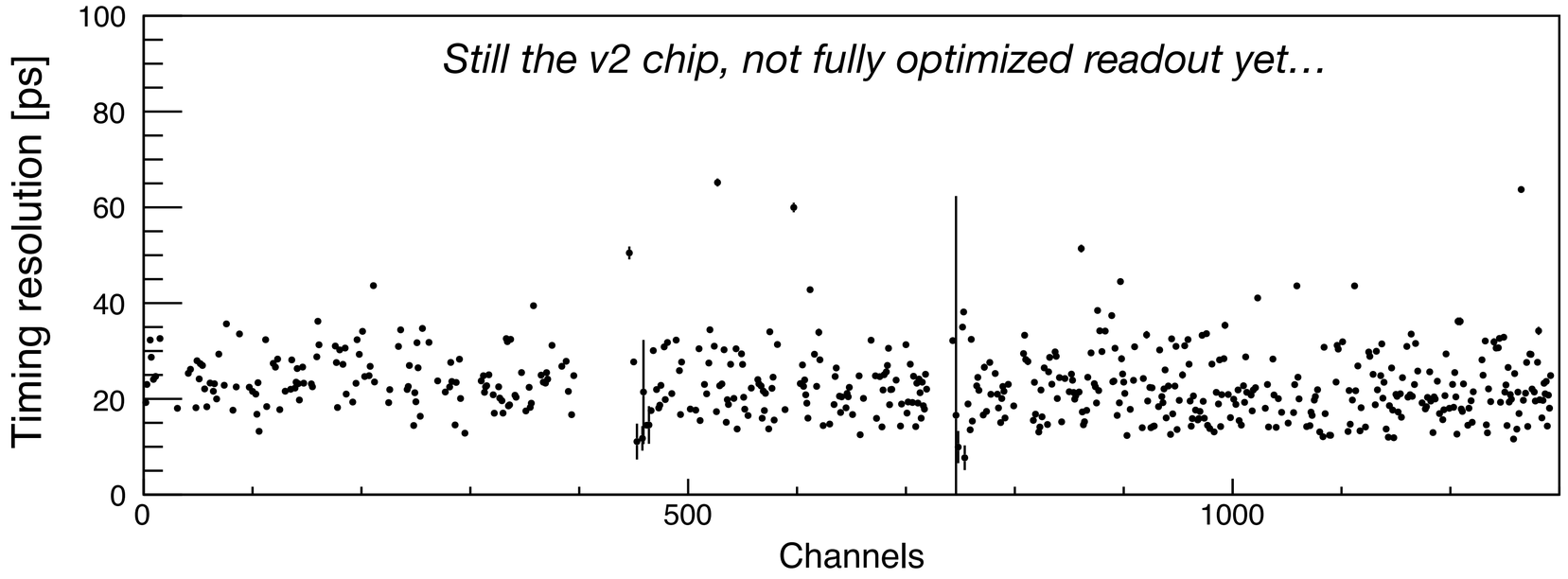
Some examples of the TOA timing distribution

Real data obtained with a prototype used in ALICE-FoCal:

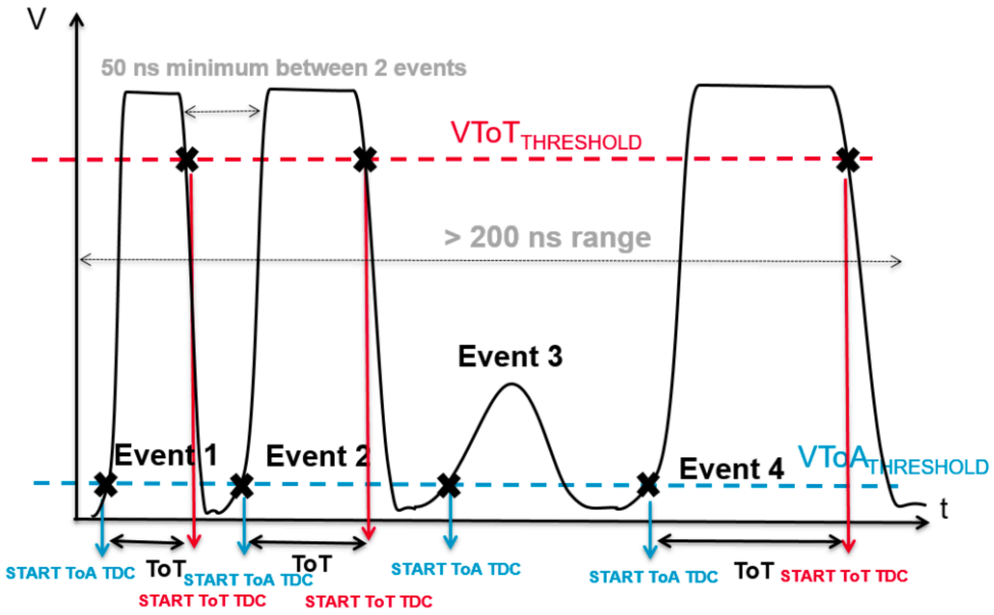
- Older version of the chip
- Realistic resolutions with noise obtained from each channel

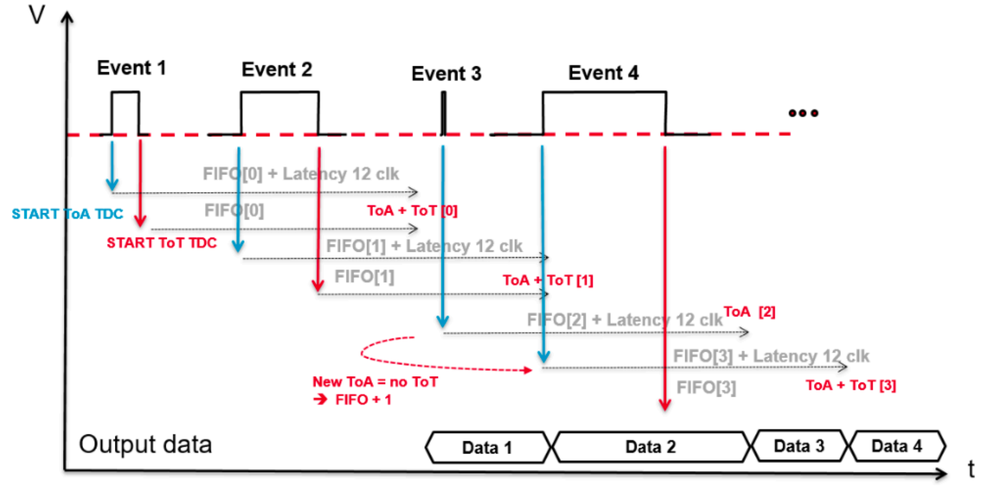
Resolution extracted from 18 ASICs in series:

- Run by a Xilinx Ultrascale FPGA
- 18 in series (from 30cm to 10cm distance from FPGA-ASIC)
- Extracted the timing resolution where I could: 15-35 ps in general



Pile-up effect



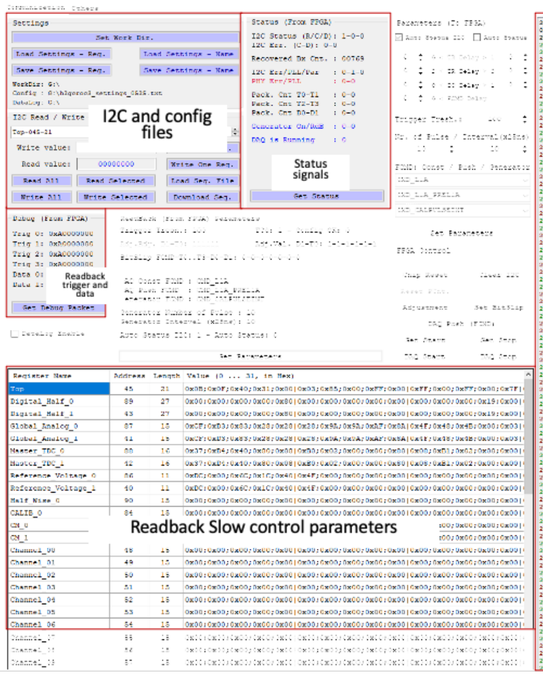


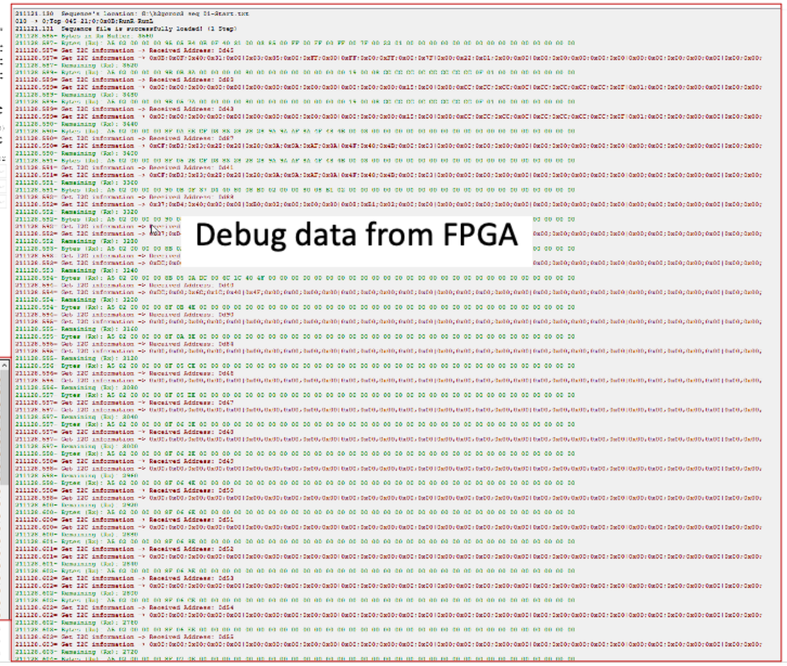
The ASIC was designed for the 25ns bunch crossings at LHC, forward region. The LHC-HL should have 100-200 collisions per bunch crossing in CMS (2800 filled buckets, 50%)

In EIC we would have 10 ns bunch crossing spacing:

- Luminosity will be much less, 500 kHz event rate is expected
- Multiplicity will be much lower, no each channel will be hit in an event
- Large background events:
  - This is substantially larger than in LHC, requires an occupancy and energy deposit study.
  - Precise timing could help us with the rejection also
  - This has to be studied per channel

Work is ongoing already toward a prototype

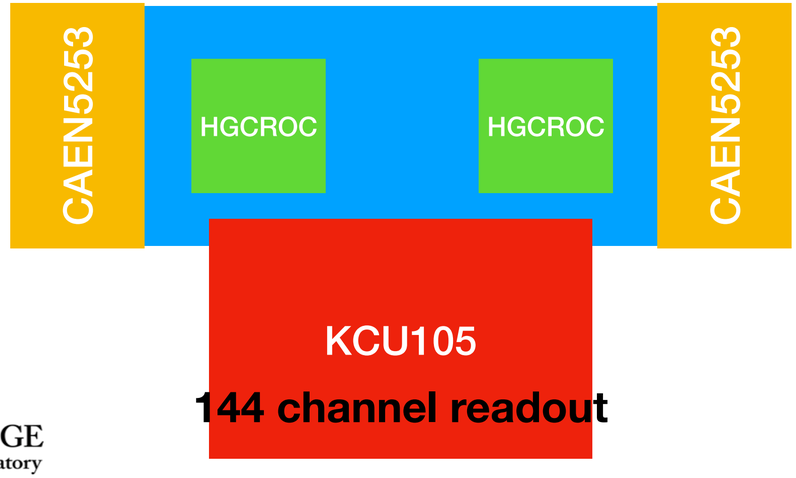




Testing is ongoing already in ORNL. First testing the feasibility for the LFHCal:

- Signal shapes and timing
- Dynamic range
- Linearity
- Sample numbers
- Maybe even clock difference at 50 MHz

First prototype readout with 2 HGCROCs in Sept



A5253 ★ New

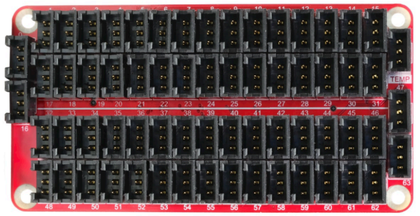
3-pin header adapter for A5202/DT5202

Request a quote

Data Sheet | Downloads

Features

- Adapts to 65 3-pin AMPMODU type 3-102203-4 connectors
- 64 connectors for the readout and bias of as many SiPMs, 1 for the readout of a temperature sensor
- Mating with A5261 cables (having AMPMODU type 102241-1 female connectors)
- A5253 Kit: A5253 adapter and 64 A5261 cables
- Matches with all 5202 form factors (A5202/DT5202)



Front view

Summary

HGCROC use for the barrel ECal:

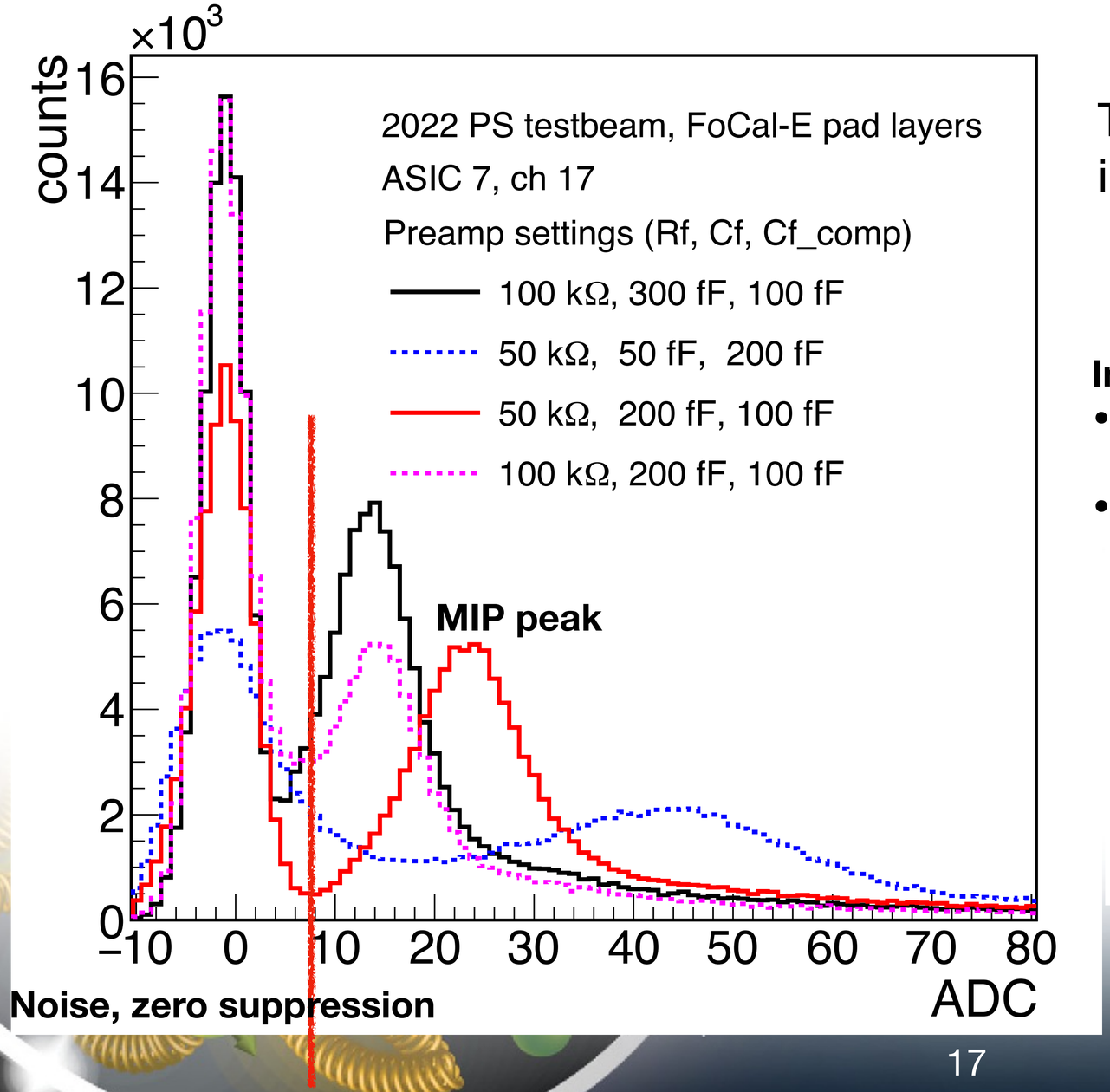
- No summing needed, more information about the shower shape
  - Dynamic range for each channel is about 15-16 bits, from MIP to highest energies
- Low power consumption (100 W on each side)
- Development and feasibility is ongoing now
- Radiation tolerance proven by CMS already (EIC will have 100 times less)
- Timing resolution (with one sample) is 15-35 ps:
  - With template fitting it might improve
  - Could be improved with better grounding scheme
  - Resulting in 3-7 cm position resolution

Max readout is now 150k$ estimate (not including FELIX from DAQ)

Concerns:

- Double signal count - how many times this happens
  - The frequency should be checked in simulation
- Background counts:
  - Where, what energy, how often?

Calibration of the detector



The data is obtained with the HGCROCv2 in PS 2022 June with silicon sensor

In addition, the H2GCROCv3 contains:

- 6-bit current conveyor to adjust the SiPM bias voltage:
  - Adjust the voltage for individual channels
- Different preamp settings

Cd (pF)	5, 10, 20	At the conveyor output and at the preamp input. To ensure the preamp stability.
Rf (Ω)	25K, 50K, 66.66K, 100K	In parallel, these resistors provide 15 values to be adjusted with the Cf and Cf_comp values to get the desired decay time constant.
Cf (fF)	50, 100, 200, 400	Combined with the Cf_comp capacitors, provide the gain of the preamplifier.
Cf_comp (fF)	50, 100, 200, 400	Same purpose than Cf capacitors but connected differently to improve the preamplifier stability. From gain point-of-view can be considered in parallel with Cf capacitors.

Table 1.1: Values for Rf, Cf and Cd