SCIPP
SANTA CRUZ INSTITUTE
FOR PARTICLE PHYSICS
UC SANTA CRUZ

SUOMEN KULTTUURIRAHASTO

SCIPP frontend ASIC efforts for EIC "Third-party ASICs" + FY23 report & FY24 proposal

June 20, 2023

Jennifer Ott
jeott@ucsc.edu

Team at SCIPP

- Simone Mazza (staff scientist)
- Jennifer Ott (postdoc)
- Matthew Gignac (asst. faculty)
- Bruce Schumm (faculty)
- K.-W. Taylor Shin (electronic engineer / senior specialist)
- Max Wilder (electronic specialist)
- Noah Nagel (junior specialist)
- Undergraduate students
- *Abe Seiden (faculty emeritus)*
- *Hartmut Sadrozinski (faculty emeritus)*

SCIPP activities overview

"In collaboration with two small electronics firms, SCIPP is currently a driving force in the development of two complementary approaches to LGAD readout. These include the CMOS-based HPSoC precision-timing "system on chip" development (Nalu Scientific) and the SiGe-based low-power ASROC front-end development (Anadyne, Inc.), both described above. We plan to continue our collaborative work with these two companies. For the case of HPSoC, characterization data accumulated for the initial five-channel prototype has allowed Nalu to begin, under our continued guidance, the refinement of the front-end design to meet the emerging goals of the EIC Detector effort. Support from this source, coupled with that expected from other sources, should allow the HPSoC collaboration to produce and characterize a second, more optimized prototype with a 10 Gs/s back-end digitizer. For the case of the ASROC effort, the FY23 will be expected to produce and characterize the first prototype of a 16-channel SiGe-based front-end amplifier ASIC geared towards the specific design goals of EIC LGAD sensors. SCIPP will also continue to collaborate with INFN Torino for the characterization of the FAST family of chips of which a new version is expected soon."

From the eRD112/eRD109 FY2023 proposal

4.2.3 SCIPP

Workforce at SCIPP on EPIC: 3 Faculty (20% FTE) + 1 junior faculty (30% FTE), 1 staff scientist (30% FTE), 3 technical staff (20% FTE), 2 postdocs (40% FTE), 3 PhD students, 8 undergrad students. Given the involvement of SCIPP both in the sensor and ASIC development a support in both. The total budget amount requested by SCIPP is 100 k$ split evenly between the two efforts, Tab. 19 contains the breakdown of the budget allocation at SCIPP.

Resource	Task	FTE (%)	Budget (k$)
Electronic Design Specialist	Service board design and layou	7.5	12.4
Electro-Mechanical Engineer	Board Assembly	5	11.8
Assistant specialist	Board loading and lab msmt	5	5.5
Materials and Supplies	ASIC service boards	-	3.3
Total	-	-	**33**

Table 19: eRD109 SCIPP budget request for FY23 on frontend ASIC R&D. All entries in thousands of dollars.

Only referring to frontend ASIC-related section – work on sensors comes in addition

SCIPP activities overview

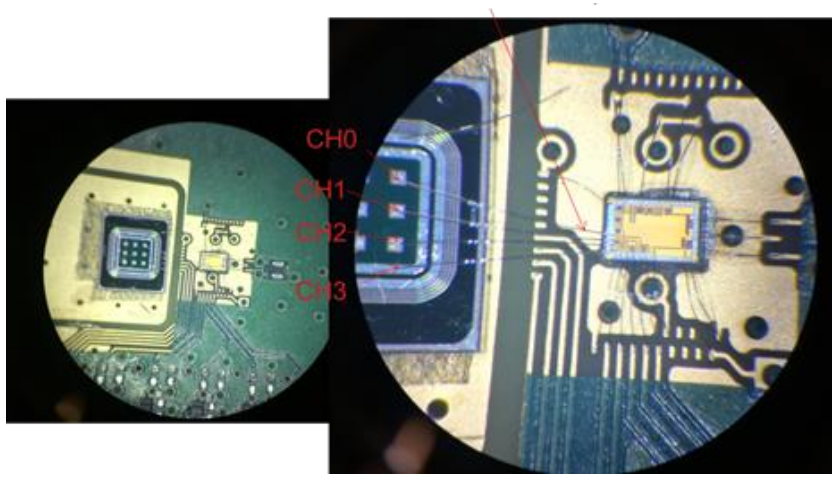
- Guidance on ASIC requirements for companies, active communication and collaboration on chip design
- Design and assembly of service and readout boards
- Characterization of ASICs
- Bonding of ASICs to relevant sensors, testing of sensor-ASIC system with signals from laser, alpha, beta particles

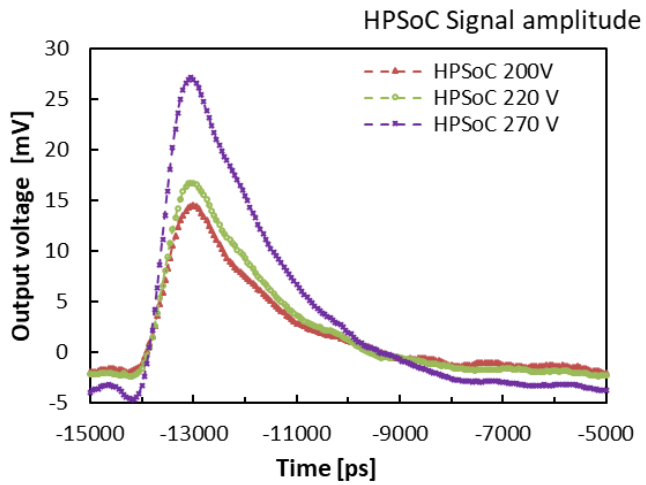
➢ $ 33k in EIC eRD funds: envisioned project distribution over FY2023 as shown below, details for each frontend ASIC in the following slides

ASIC	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sept	Oct	Nov	Dec
Nalu												
ASROC												
FAST3												

HP-SoC / HD-SoC (Nalu Scientific LLC)

- 65 nm CMOS, aimed at waveform digitization
- First 4-ch prototype developed, fabricated and tested through SBIR Phase-1 funding
- Emphasis on characterization of first-stage transimpedance amplifier with LGAD sensors
- Reaches 600 ps rise time and ~45 ps jitter: main issue was the lower than expected output signal amplitude

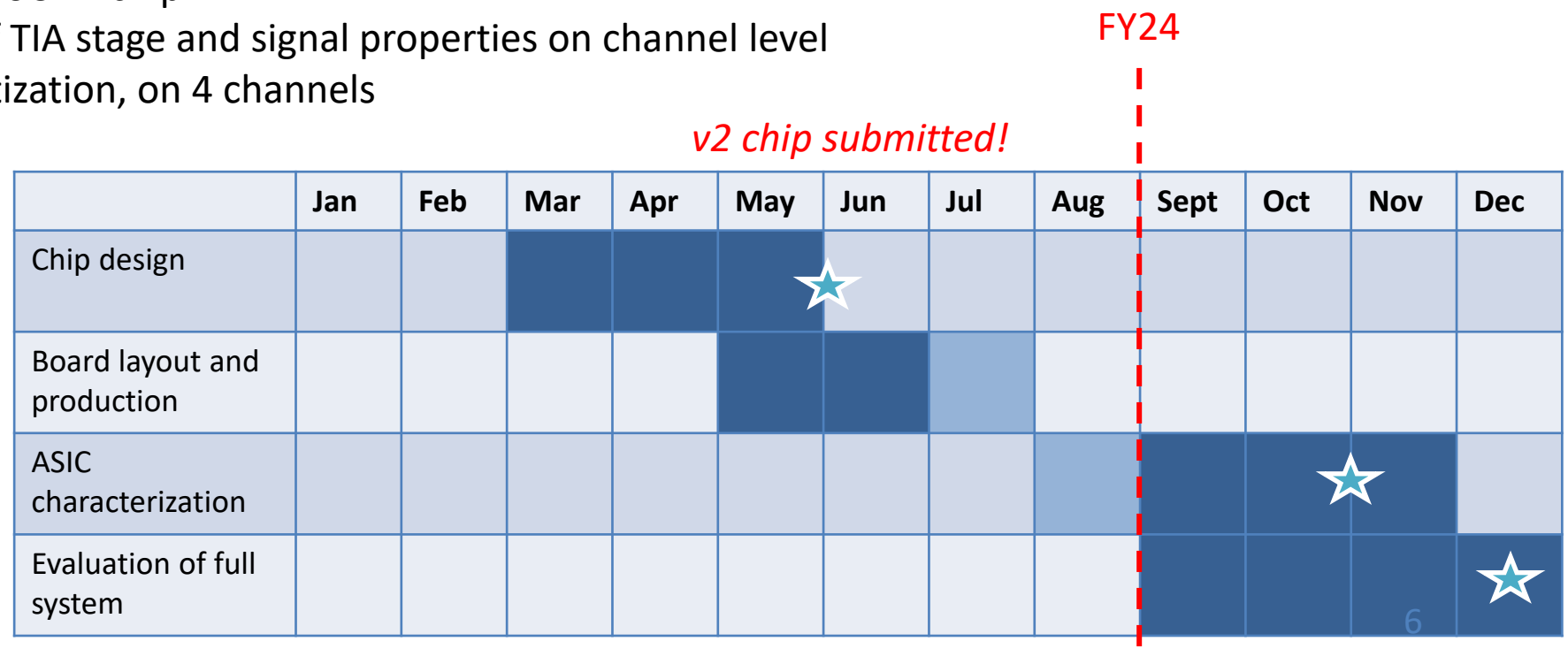




TWEPP 2022: https://indico.cern.ch/event/1127562/contributions/4904727/ https://arxiv.org/abs/2210.09555v2

HP-SoC / HD-SoC (Nalu Scientific LLC)

- Prototype 2: improved first amplification stage, waveform digitization at 10 GS/s, independent operability of multiple channels
- Partly funded by Jefferson Lab EIC funding (primarily design and production costs of Nalu)
- SCIPP:
  - $ **Electronic engineer, specialist(s)**
  - $ Production of readout PCB
- Milestones:
  - Submission of HP-SoC v2 chip
  - Characterization of TIA stage and signal properties on channel level
  - Full waveform digitization, on 4 channels



Key developments to v2

- Assuming 0.4 pF input capacitance
- Simulation before any parasitics
- In order to achieve timing resolution below 30 ps, it is likely necessary to go to thinner sensors (Landau distribution of charge deposition can only be reduced in this way)

	TIAv1+Gain v1	TIAv2 + follower	TIAv2 + Gain
Gain (signal/ freq=0)	6.48/13 (kOhm)	6.50/9.9(kOhm)	11.9/43(kOhm)
Rin (signal/freq=0)	872/1.4k (Ohm)	177/246 (Ohm)	63/254 (ohm)
Bandwidth	228Mhz	356MHz	129MHz
Rise time	649ps	627ps	691ps
Output bias	357mV	359mV	249mV
Noise (5 GHz)	0.093mV	0.162mV	0.14mV
Current	1.63mA	2.4mA	3.15mA (2.24mA final)
Vpeak (from Base)	92mV	92.3mV	169mV
Estimated jitter (assuming 1 mV total noise)	8.8ps	8.5ps	5.1ps

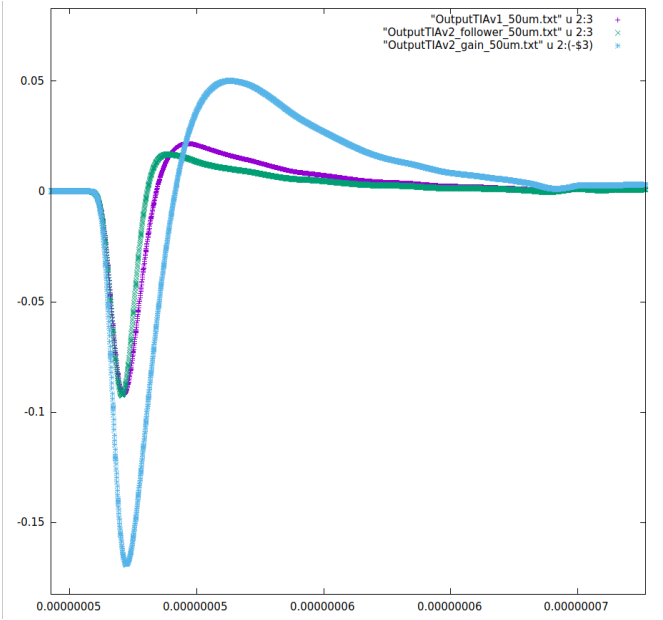
50 µm (~10 fC signal)

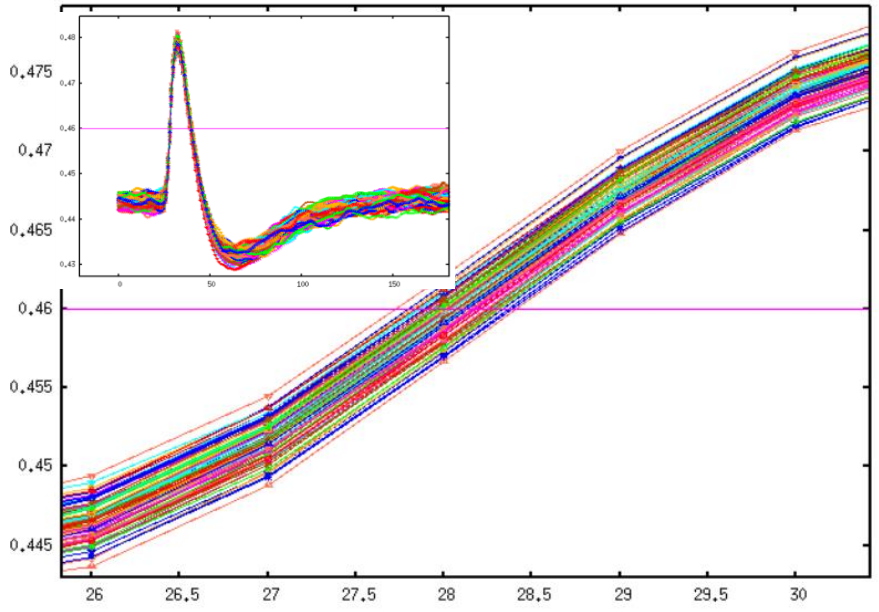
	TIAv1+Gain v1	TIAv2 + follower	TIAv2 + Gain
Gain (signal/ freq=0)	3.05/13 (kOhm)	3.16/9.9(kOhm)	5.15/43(kOhm)
Rin (signal/freq=0)	503/1.4k (Ohm)	117/246 (Ohm)	29.5/254 (ohm)
Bandwidth	228Mhz	356MHz	129MHz
Rise time	348ps	332ps	368ps
Output bias	357mV	359mV	249mV
Noise (5 GHz)	0.093mV	0.162mV	0.14mV
Current	1.63mA	2.4mA	3.15mA (2.24mA final)
Vpeak (from Base)	43.3mV	44.9mV	73.6mV
Estimated jitter (assuming 1 mV total noise)	10ps	9.24ps	6.24ps

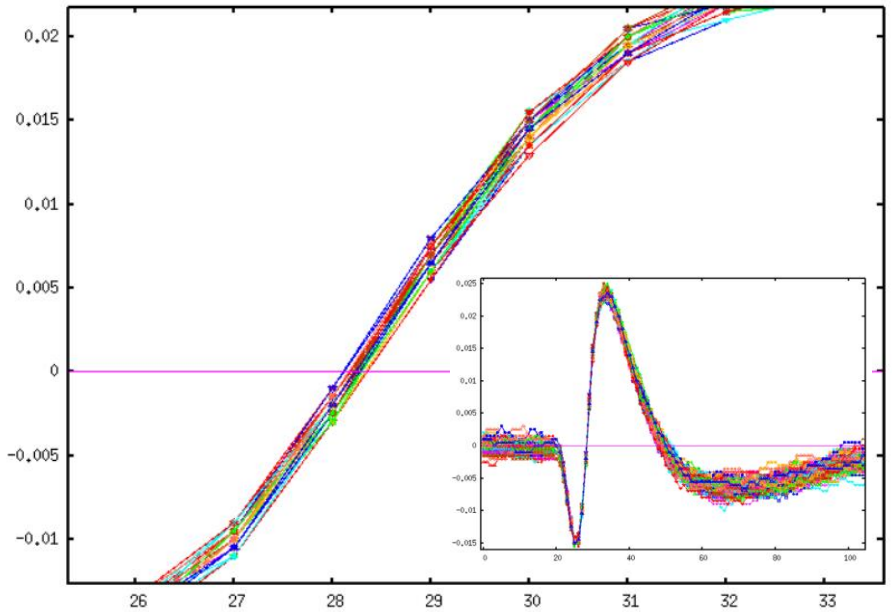
20 µm (~4 fC signal)

Expected output and power consumption

- Improved TIA and gain stage: higher signal amplitude
- Waveform digitization at 10 GS/s (10-bit): allows baseline correction, CFD and other algorithms for improving jitter component of the timing resolution
- Simulated HP-SoC v2 output digitized waveforms with noise: estimated reduction from 13.7 ps (leading edge) to 5 ps





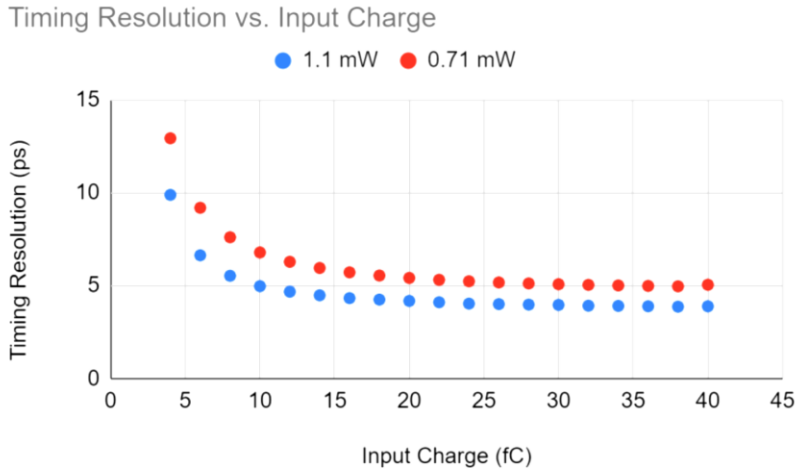


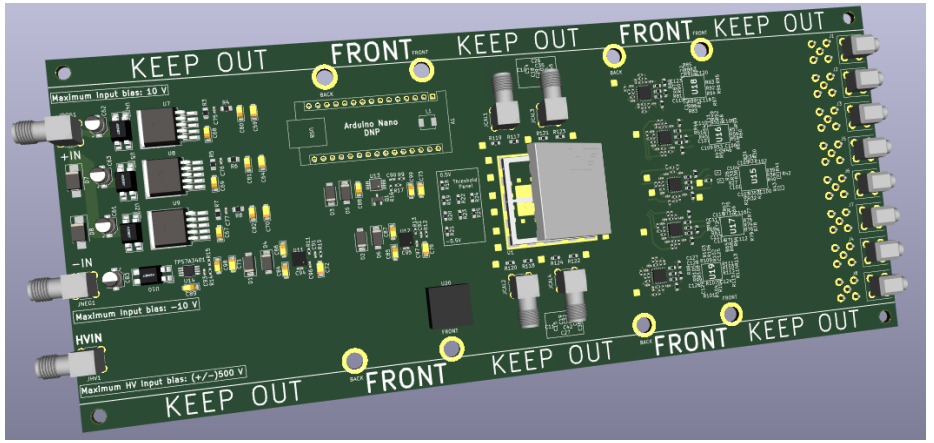
Power consumption

- TIA (with gain): 2.24mA
- Trigger: 0.720mA
- Ramp: ~30uA
- Comparator: 256x1uA = 0.256mA
- Total w/out clock and counter distribution: 3.25mA
  - Ca. 3.3 mW (1 V op)

ASROC (Anadyne Inc)

- 16-ch SiGe BiCMOS analog (discriminator) chip, developed under SBIR Phase-1 funding
- Focus on low power consumption (0.7-1.1 mW/channel) and noise
- ROC design finalized, tapeout: Dec 2022





TWEPP2021: https://indico.cern.ch/event/1019078/contributions/4444426/

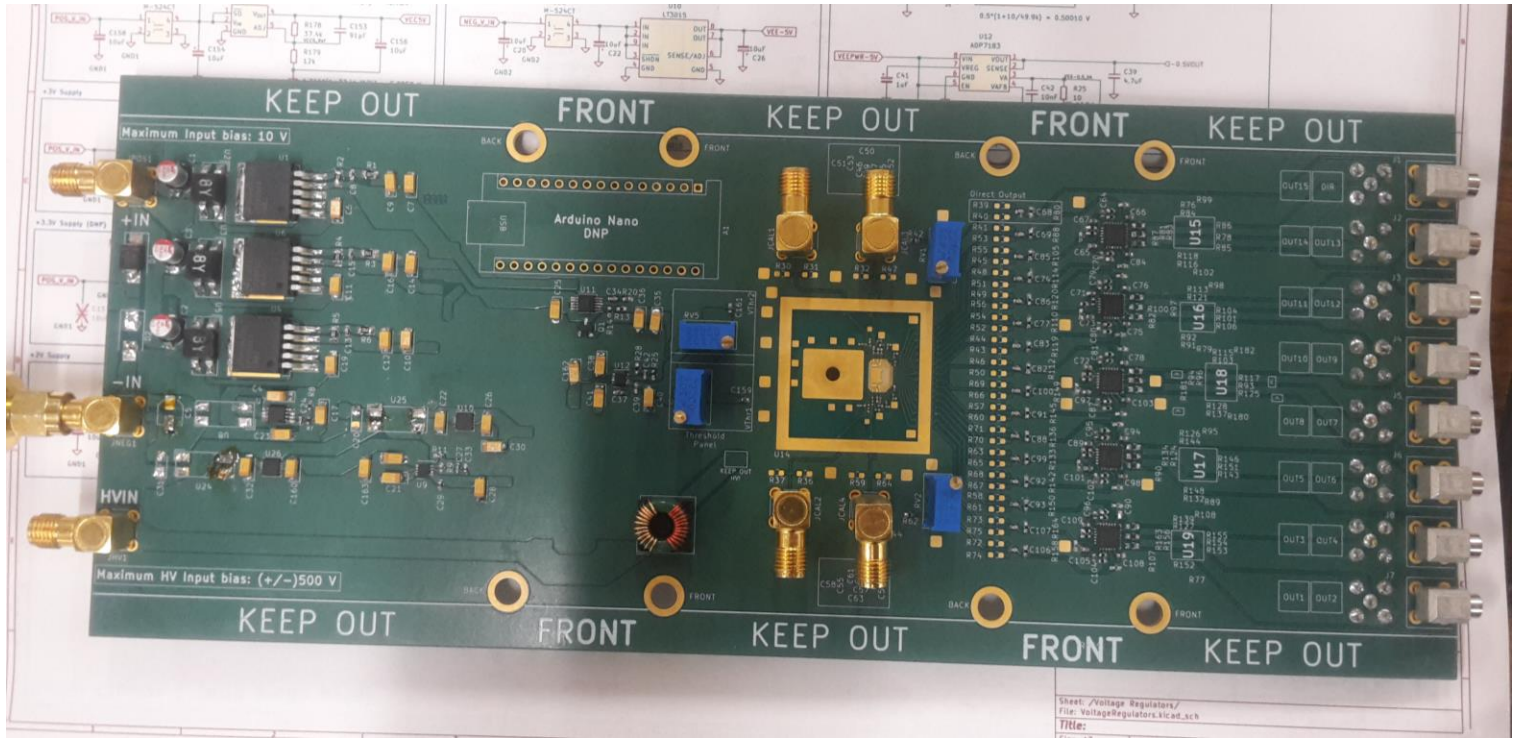
ASROC (Anadyne Inc)

- ROC design finalized, tapeout: Dec 2022
- Development of readout board ongoing, estimated finish Feb 2023
- SCIPP:
  - $ **Electronic engineer, specialist(s)**
  - $ **Production of readout PCB**
- Milestones:
  - Complete first electrical tests with ASROC
  - Evaluation of ASIC in both power modes, with multiple channels bonded to sensor and read out

	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sept	Oct	Nov	Dec
Board layout and production												
Initial ASIC testing							☆					
Full ASIC characterization								☆				

ASROC update

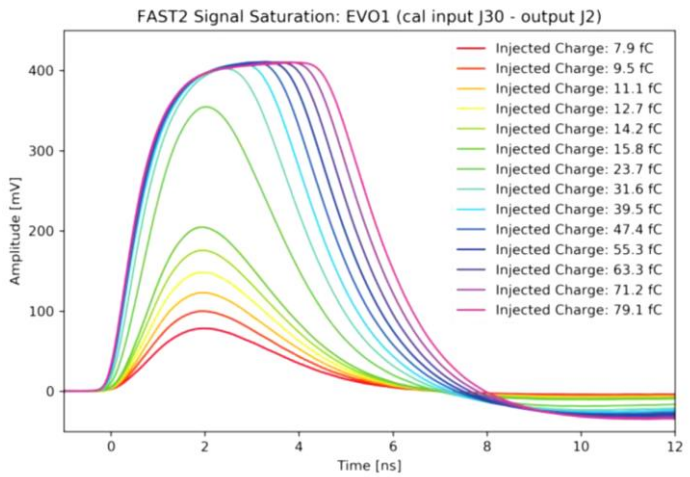
- Readout board fabricated, assembled, first tests of voltage rails and buffers ongoing

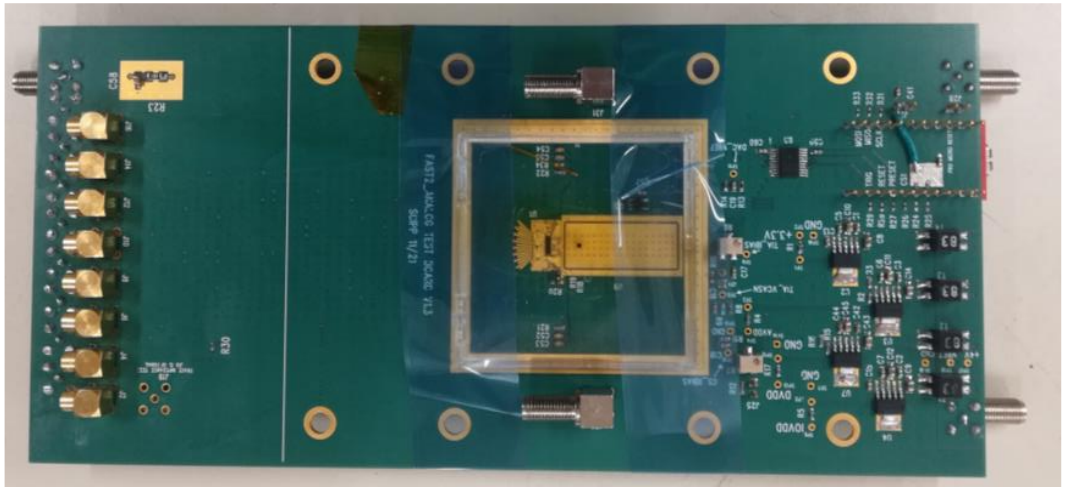


- Delivery of functional chip on time, but delays in finalization of backgrinding, back metallization, dicing: ETA June-July

FAST (INFN Torino)

- Good contacts with University and INFN Torino through fast sensors R&D
- FAST ASIC family: 110 nm CMOS, 16-(20)-ch discriminator & TDC
- Programmable high- and low-gain stages; longer rise and fall time
- FAST and FAST2 analog chips have been tested at SCIPP with different signal polarities and injected charge
- Custom readout board developed for FAST2

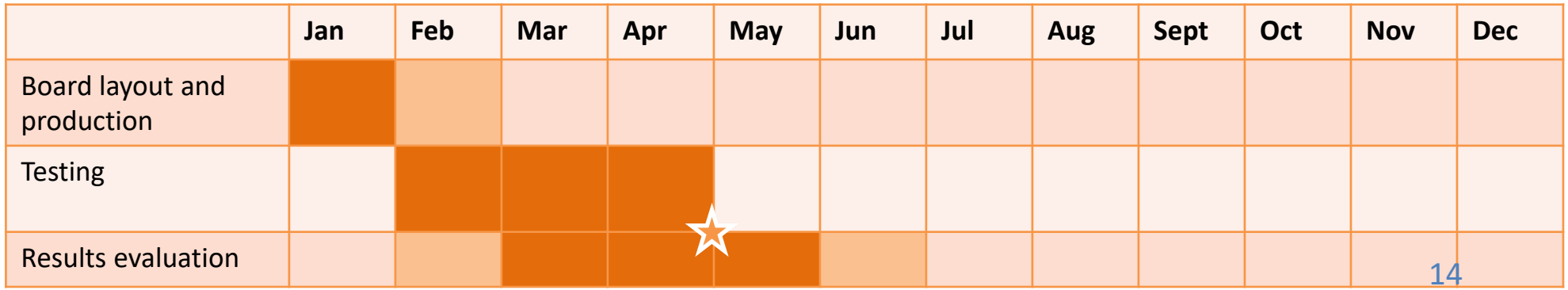




E.J. Olave et al (FAST): https://www.openaccessrepository.it/record/74450#.Y7WoDRXMJPZ
A. Martinez Rojas et al (FAST2): https://ieeexplore.ieee.org/document/9875441

FAST3 (INFN Torino)

- New designs for input bias cell, analog output buffer, pulse width regulator; several test versions (analog and digital) produced
- SCIPP: custom readout board developed for FAST2: can be used with no or minimal adaptations for next generation – FAST3
  - $ (Modification) Production of readout boards
  - $ **Junior specialist or student(s)**
- Milestones:
  - Testing of FAST3, comparison of performance to FAST2 and other ASICs



FAST3 update

- Chip delayed?

- We are still interested in this chip for reading out long strip sensors with higher input capacitance, and gain switching, primarily for the PIONEER experiment Active TARget
  - This chip can handle higher input capacitances than others – valuable information also for ePIC
- Low-effort activity: will be mentioned in report and proposal, but not highlighted in proposal budget

FY23 Summary of costs / budget, distribution

- PCB production and population: 3.3 k$
- 7.5 % / 5 % FTE electronic engineer / senior specialist
- 5 % FTE junior specialist

- FAST and corresponding readout board is the most mature technology: can rely more on students and junior specialist
- ASROC and HP-SoC require electronic engineer for board design; testing will be led by staff scientist and postdoc

FY24 Summary of costs / budget, distribution

- Asking for $45k in eRD109 – similar as previous year but intensifying some efforts
- Exact itemization still to be decided
  - Fractions of electronics engineer, specialist(s)
  - Materials and supplies, readout boards

eRD109 FY23 report

- Short summary of third-party ASICs

- Input to Nalu HP-SoC fast preamp and waveform digitization chip, v2 – chip submitted
- Starting layout of new readout board, including larger/more probe pads to allow readout of 4 channels

- ASROC 16-ch SiGe chip delivered, sent for back-end processing
- ASROC readout board produced

- Testing with FAST2 including digital side

eRD109 FY24 proposal

- Sources of risks to the project related to AC-LGAD readout: **three subsystems (Forward, Barrel, Roman Pots) with at least two different sensor design benchmarks** and hence different requirements for readout; no final layout for any of these systems yet decided
- EICROC0 is primarily targeted at pixelated Roman Pots sensors and has not been evaluated together with a sensor yet
- Reaching ambitious timing and position resolution goals appears challenging…

  - Different sensor designs and performance goals bring potentially different requirements for the readout electronics, which may be best answered with different front-ends
  - R&D on several ASIC candidates should continue to be funded, to increase the likelihood to have a readout within the project which can deliver the targeted performance on the relevant AC-LGAD sensor(s)

Sensor designs

- **Strips**: larger sensors, fewer channels per sensor, larger input capacitance; Time-of-Flight more important, spatial separation of hits at EIC luminosities less critical (lower occupancy)?
  - ➢ Capacitance ‘tolerance’, timing, large sensors, uniformity, wirebonding

- **Pixels/pads**: smaller capacitance, more channels, more complex reconstruction with multiple channels
  - ➢ Precision spatial hit reconstruction, signal-to-noise, timing, channel density, power consumption and material budget (presumably bump-bonding)

eRD109 FY24 proposal

- Third-party ASICs include front-end amplifier layouts, waveform digitization etc which could significantly support reaching the timing and spatial resolution targets for ePIC AC-LGAD –based ToF-PID, with slightly different emphases depending on the detector subsystem

- Low-noise and low-power SiGe front-end is attractive, if it can deliver up to expectations: testing/evaluation once chip is delivered
  - Study multi-channel operation and check for noise and cross-talk in 16-ch first prototype
- Nalu HP-SoC is the only ASIC under consideration that provides waveform digitization at high rate: especially relevant for precise position reconstruction? CFD or other algorithms also lower the jitter = improve timing resolution

- High capacitance of strip sensors is a challenge for all ASIC candidates

- SCIPP is also considering to acquire an EICROC test system to support testing and comparison in equivalent conditions (with the same sensors) with our other ASICs
- Anything that is learned from these other ASICs could be utilized in future developments and improvements of selected (common) AC-LGAD readout