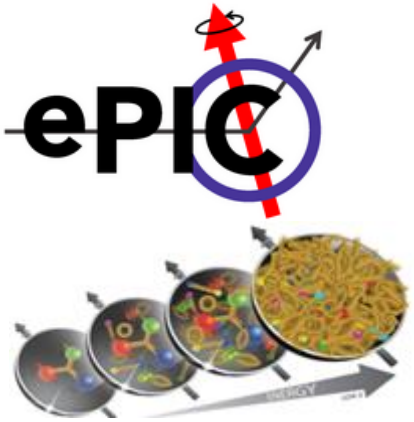


DOE/eRD109

The EICROC Project

Objective: **Development** and **characterization** of an **ASIC EICROC (32 x 32)**
able to read-out the new generation of pixelated (500 x 500 µm²) silicon sensors: **AC-LGAD**
(**L**ow-**G**ain **A**valanche **D**iode) coupled **AC**
for the **Electron Ion Collider** (EIC)
1st intention: optimized for Far Forward detectors: the **Roman Pots**

RC2
RC3

Stepping up through succesive ASIC iterations to control performances fulfilling ePIC detector requirements

- EICROC0 prototype (16 channels; 4 x 4): under test since March '23
- EICROC0_V1: updated EICROC0 fixing observed issues + lower power consumption ADC: 2024
- EICROC1 including EIC clocking): 2025
- ./.. EICROC2 (32 x 32 channels): 2026

(EICROC Project Timeline in back-up slides, p15)

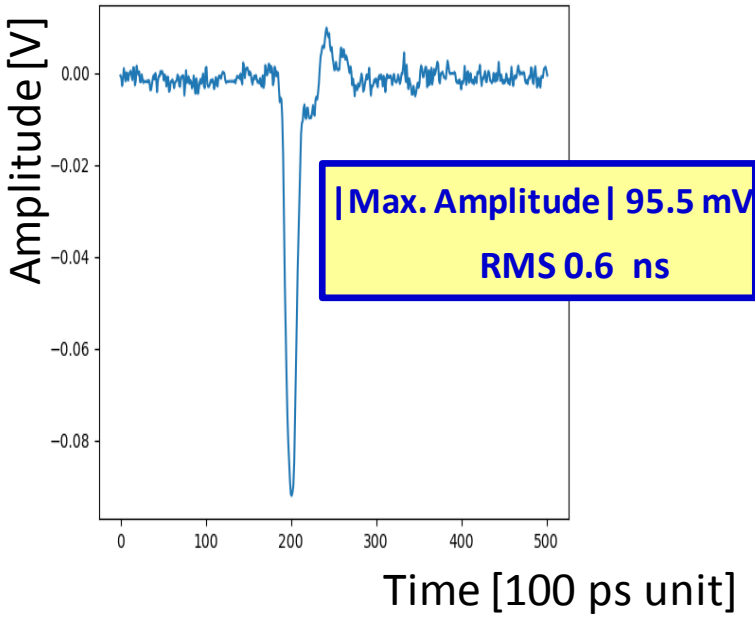
Status of EICROC0 Test Bench at IJCLab

RC2 | RC3

Preliminary studies [board w/ EICROC0, no AC-LGAD]

- TZ Pre Amplifier output signals
  - S/N > 70 for 12.5 fC input (expectation S/N > 5 for 1 fC input)
  - Jitter evaluation: 34 ps (25 fC), 41 ps (6 fC) [theoretical 12 ps] investigation of a flloor jitter contribution from charge injection
- TDC performance:
  - Time resolution ~ 20 ps
  - quantification step (~25 ps) in fair agreement with design
- ADC performance in agreement with design
- Investigation of noise / clock couplings on-going to drive next ASIC teration
- Evaluation of cross-talk between channels underway

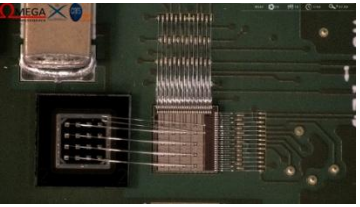
Typical **PA output signal** (12.5 fC input)



Rise (Fall) Time (RT) computed between 10% and 90% of |Max. - Ampl.|

RT 0.7 ns

Short term plan: to evaluate performances of the existing board w/ **EICROC0 + AC-LGAD** (4 x 4)



Wire-bonding by Brookhaven National Laboratory

AC-LGAD ASIC effort: Status (June '23)

Supported by DOE/eRD109 Consortium

- **EICROC developments (OMEGA, CEA/Irfu, IJCLab in close collaboration with BNL):**
  - *EICROC0 characterization on-going to drive next ASIC iteration*
  - *Individually each component shows performance in agreement with design*
  - Investigation of noise / clock couplings on-going to drive next ASIC teration
  - Evaluation of cross-talk between channels underway
  - *additional test benches at OMEGA (operational), at BNL (shortly), at CEA/Irfu*
  - *EICROC French team reinforced*

For risk mitigation: other AC-LGAD ASIC designs considered (eRD109 supports)

- **FCFD (Fermi Lab): FCFDv1, FCFDv2**
- **UCSC/SCIPP: characterization of 3rd party ASICs: HPSoC, ASROC & FAST-2/3**

RC3 | RC4