UK activities and plans

Georg Viehhauser for the UK ePIC SVT collaboration

UNIVERSITY OF BIRMINGHAM

Brunel University London

Lancaster University

UNIVERSITY OF LIVERPOOL

UNIVERSITY OF OXFORD

Science and Technology Facilities Council

ePIC UK

Funding

- Currently funded through UKRI Preliminary Infrastructure Fund
  - Oct ‘21 – Mar ’24, 2.97M£ for MAPS, Timepix, and Polarimetry (29.2 FTE)
  - This award is a Preliminary Activity or Scoping Project
- Future funding: EIC Full Phase Infrastructure Fund
  - Starting in ’25 for 7 y, for remaining R&D and construction
  - 5 WPs (WP1 – Silicon Tracker, WP2 – Electron Tagger, WP3 – Luminosity Monitor, WP4 – Accelerator, WP5 – Project Management)
  - Has been prioritised by STFC SB/TAAB, Council and EB to go forward to Wave 3 of the UKRI Infrastructure Fund
  - Have until June 30 to submit the final pro-forma application and costings for sign-off by EB before submission to Infrastructure Advisory Committee
- Bridging funds from ‘24 to start of Full Phase Infrastructure Fund
  - Under negotiation with UKRI

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What we are currently doing

- Sensor design
  - Contributions to MLR and ER1 submissions
    - High speed data transmission blocks, I2C on-chip transmission, library redesign for DFM
- Sensor characterisation
  - Full characterisation of two APTS process splits at BHM and LIV, plots under approval by ITS
  - DTPS setups to be received at RAL and DL in the next few weeks
- SVT layout
  - Tiling study at BHM and initial work on CAD model at DL
- Powering
  - Work on serial powering regulator, architecture, services
- Detector and physics simulations
  - Parametrisation of momentum and vertex resolutions
  - Studies of beam spot effect on the tracking performance
  - Acceptance at large η
    - Barrel MPGD layer contribution to tracking
      - New method developed for reconstruction of DIS kinematic variables

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Programme to be funded

- Funding for 7 years, starting form 2025
  - The schedule is based on CD4A (transition into operation) in Apr ‘32 with detector delivery one year earlier in Apr ’31
- We requested 153 FTEs for 7 years (70% of cost of UK project)
  - 25 FTE academics, 30 FTE PDRAs, 56 FTE engineers and 42 FTE techs
- For silicon submissions we costed
  - A contribution of 37% to the mask/NRE costs of the EIC LAS V2 and EIC LAS production
  - A contribution of 37% to production of the EIC LAS V2 wafers
  - Entire production of wafers for the sagitta layers
  - We assumed mask/NRE at 10 M£, wafers at 10 k£ each, and a yield factor 2
    - Also consumables, equipment and travel to support the proposed programme

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What we would like to do

- If compatible with preferences of the rest of the SVT community,
- We would like to supply the complete barrel sagitta layers (SL)
  - Sensors, local and global support structures, powering, and on-detector services (cooling, cables and/or bus tapes, etc.)
  - Including QA and QC during design and construction, incl. final acceptance of complete package

Tentative sharing of tasks

Task during R&D phase	Institute
Sensor design	RAL-TD
Sensor characterisation	BHM, BRU, DL-TD, LIV, LAN
On-detector electrical services (i.e. FPC)	DL-TD, OX
Powering	BHM, OX, RAL-PPD
Local supports incl. cooling (i.e. staves)	OX, DL-TD
SW/FW DAQ (EIC LAS/system test)	BRU, DL-TD, LAN, RAL-PPD
Tooling (module assembly, stave loading)	BHM, RAL-PPD, OX
Global support (mechanics)	OX, DL-TD, LIV

Task during construction phase	Institute
Sensor QC/QA	BHM, BRU
Module assembly & testing (QC/QA)	BHM, BRU, RAL-PPD, LIV
On-detector electrical service production	DL-TD, OX
Local support production	OX, DL-TD
Loading modules onto staves + system test	DL-TD, RAL-PPD, BHM
Full layer(s) assembly + system test	OX, RAL-PPD, BHM
Shipping to BNL	OX, RAL-PPD

BHM – Birmingham, BRU – Brunel, DL – Daresbury Lab, LAN- Lancaster, LIV – Liverpool, OX – Oxford, RAL – Rutherford Appleton Lab

Contacts and next steps

- Contacts: Peter Jones (overall UK project)
  Laura Gonella, Iain Sedgwick, Georg Viehhauser (UK WP1, SVT)
- Planned next steps:
  - F2F meeting of UK SVT groups on June 28th in Liverpool
  - Develop set of requirements and specifications for SVT and specifically SL
  - In close collaboration with international SVT collaboration

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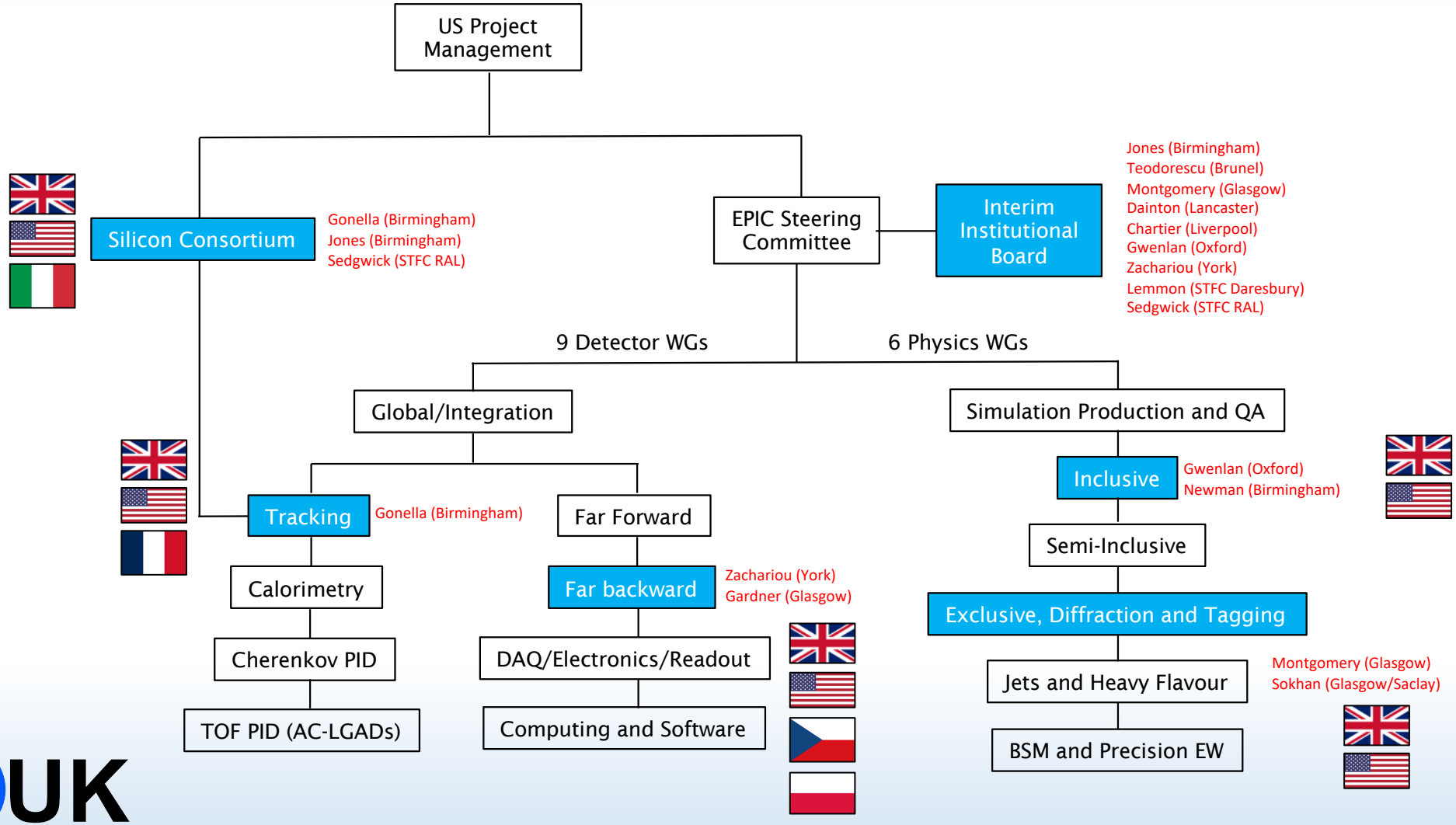
Further Material

ePIC Collaboration and UK leadership



Effort sharing

Task	Effort (FTE)
Sensor design	7
Sensor characterisation and testing	23
Flexible printed circuits, modules and DAQ (incl. powering)	50
Staves production, global mechanical support and integration	29
FTE for tooling and assembly (including installation and commissioning)	41
Performance studies	3

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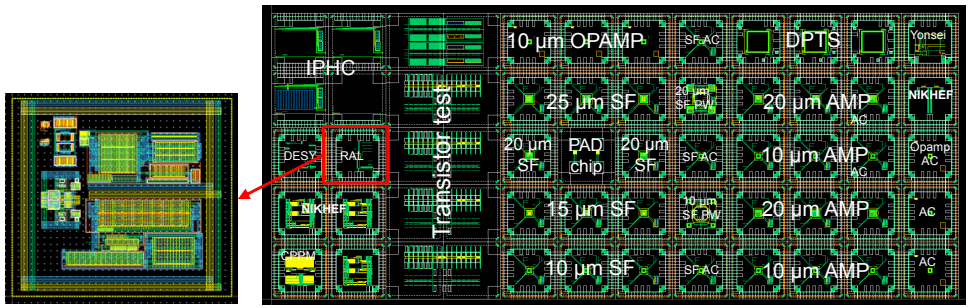
WP1.1 – Sensor Design

- MLR1 Designs from RAL (Q4 2020)

First submission in TPSCo 65 nms
Scoped within CERN EP R&D WP1.2 Significant drive from ITS3
Contributions from several groups



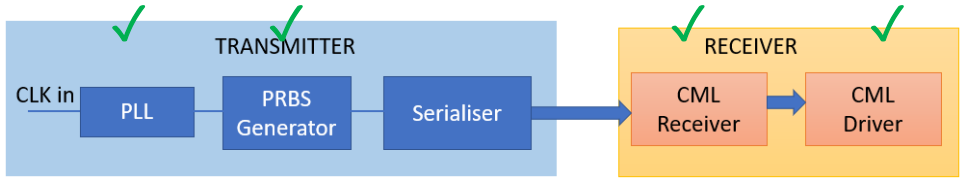
RAL: LDVS receiver and CML transmitter

Scope: Technology exploration and prototype circuit blocks for future sensors

Large number of test structures; including Analogue and Digital Pixel Test Structures

- ER1 Designs from RAL (Q4 2022)

Functional blocks for high-speed data transmission



PLL dual mode 1 GHz/ 7 GHz
PRBS Generator
CML Receiver
I^2C block for on-chip data transmission

Plus, redesigned standard cells for DFM

Buffers, AND gates, NAND gates, inverters, Filler cells, Flipflops

WP1.1 – Sensor Design

- ER2 Plans

  RAL is now part of the ITS3 ER2 designers team contributing

  - New logic libraries
  - Fast driver/receiver blocks
  - On-chip regulation

  In parallel, RAL is working on the design of a Shunt-LDO regulator for the serial powering scheme specific to the ePIC detector

  - Specifications captured
  - Bandgap circuit design advanced
  - Shunt-LDO schematics design started
  - Technology choice under consideration

WP1.2 Sensor Characterisation

- MLR – RAL IP Block

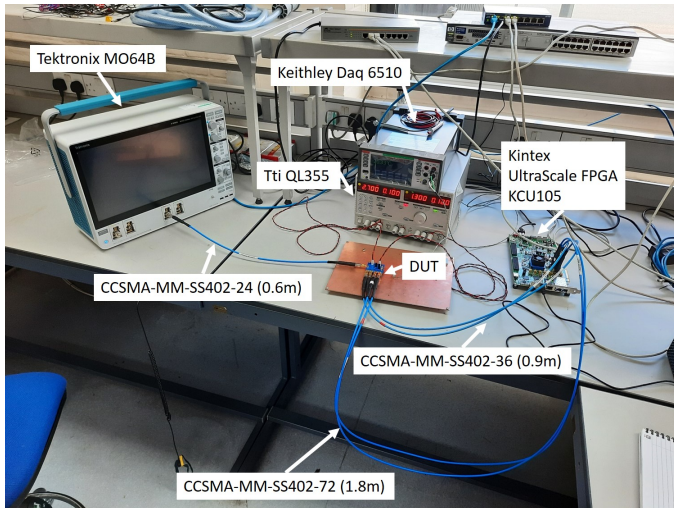
  New MLR test setup for RAL IP block: LVDS receiver and CML transmitter

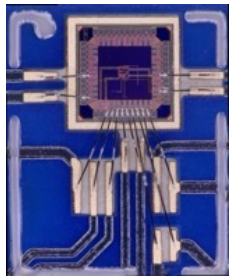
  Chips bonded to carrier boards at Birmingham and Liverpool

  X-ray irradiations carried out at CERN up to 9900 krad at two dose rates (Sep 22)

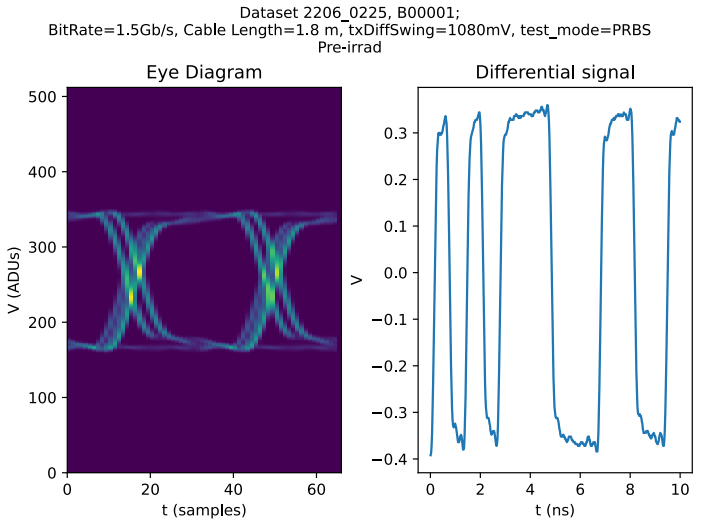
  Tests performed at Daresbury before/after irradiation

  Chips survived irradiation up to target dose ~10 MRad (Full results in: 20221021-XrayIrradReportV1-rep-2021a05.pdf, e.g. plots in slide 13 if needed)





RAL chip in new test system by DL/BHAM/LIV



WP1.2 Sensor Characterisation

- MLR - APTS / DPTS

MLR contains Analogue Pixel Test Structures (APTS) and Digital Pixel Test Structures (DPTS) designed by ITS3 groups

Birmingham and Liverpool fully integrated in the ITS3 WP3 group

Full characterization of 2 out of 4 process splits with APTS, preparing plots for June approval session

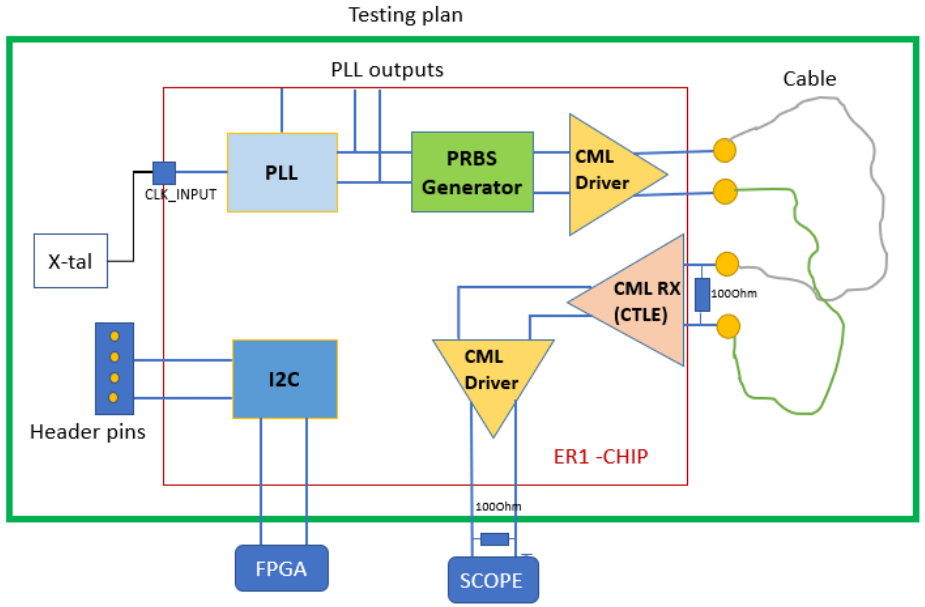
Contribution to APTS test beam data analysis

DPTS setups for RAL and DL expected in June

- ER1 – RAL IP block

The ER1 sensor and test structures received from manufacturing in March.

Setup for RAL blocks testing in preparation (RAL TD, DL)



WP1.3 – Modules and System Tests

- ALICE – ITS3

  Wafer-scale sensor: L = 280 mm

  Each layer composed of 2 sensors

  L0 = 2 x (3 x 9 reticles)
  L1 = 2 x (4 x 9 reticles)
  L2 = 2 x (5 x 9 reticles)

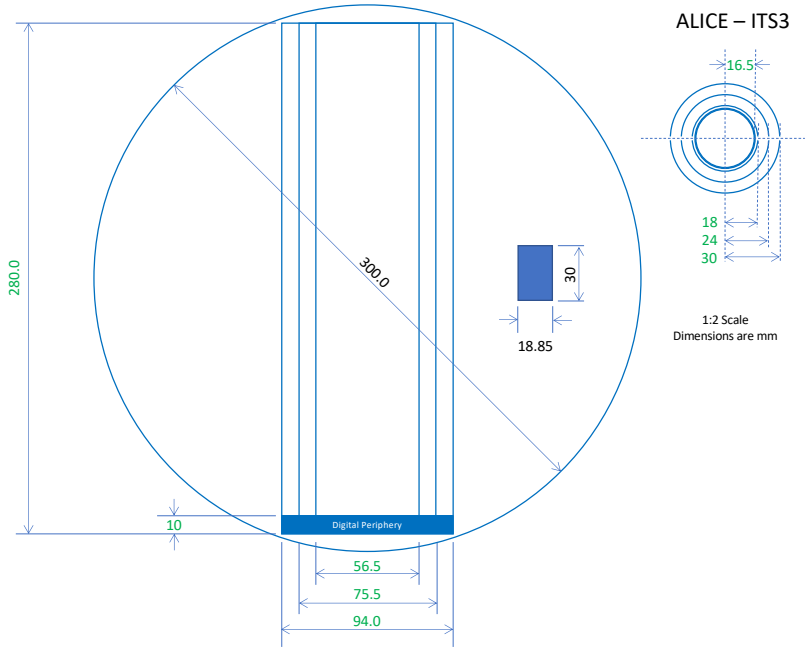
- EPIC – SVT

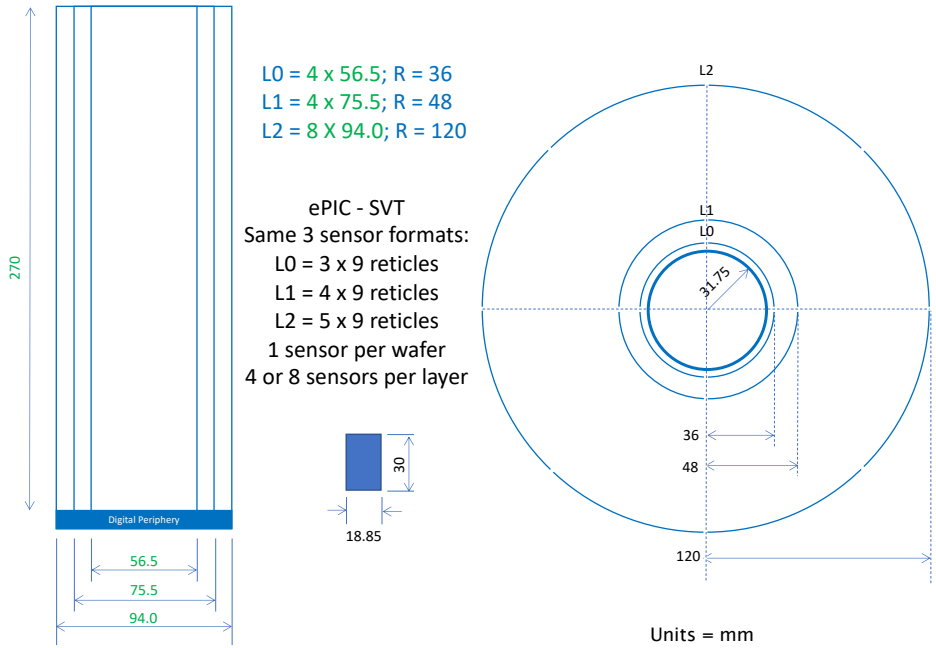
  Will use same 3 sensor formats

  Each layer composed of 4 or 8 sensors

  L0 = 4 x (3 x 9 reticles)
  L1 = 4 x (4 x 9 reticles)
  L2 = 8 x (5 x 9 reticles)

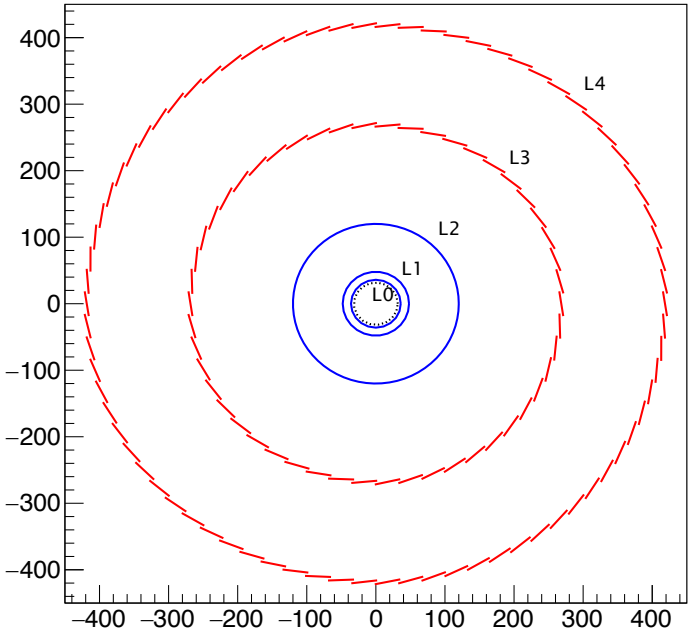
  Note: 5 mm gap for beam pipe bake out

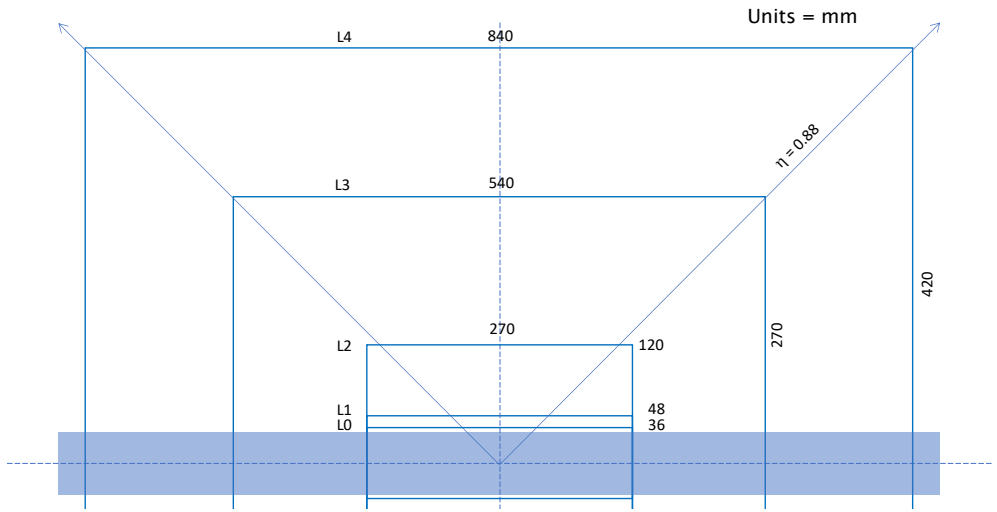




WP1.3 – Modules and System Tests

- EPIC sagitta layers





L0, L1 and L2 lengths are single sensors that are 270 mm long (9 reticles)
L3 length can be achieved using two sensors 270 mm long (9 reticles)
L4 length can be achieved using four sensors 210 mm long (7 reticles)

- L3 – 50 staves

2 sensors wide = 37.7 mm
2 sensors long = 540 mm (2 x 9 reticles)
Mean radius = 268.4 mm
Rϕ overlap = 3.5 mm ~ 10%
4 sensors per stave; 5 sensors per wafer
Require 200 1x9 sensors (40 wafers)

- L4 – 78 staves

2 sensors wide = 37.7 mm
4 sensors long = 840 mm (4 x 7 reticles)
Mean radius = 418.5 mm
Rϕ overlap = 3.5 mm ~ 10%
8 sensors per stave; 10 sensors per wafer
Require 624 1x7 sensors (63 wafers)

WP1.3 – Modules and System Tests

- Disk tiling strategy

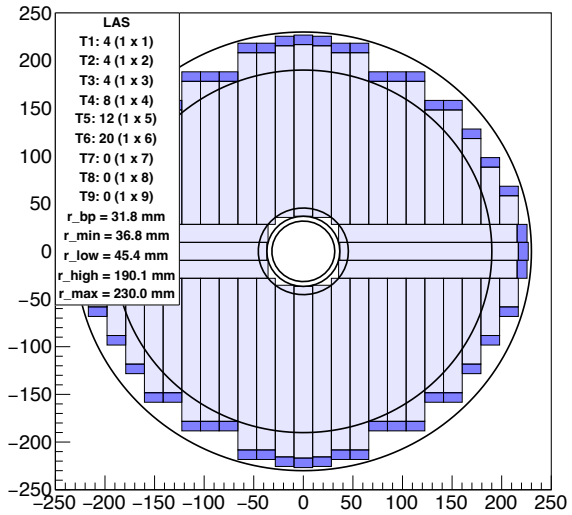
  Investigate sensor formats needed

  Two designs studied:
  Design #1 = vertical tiles/sensors
  Design #2 = herringbone pattern (alternating vertical and horizontal tiles)

  No sensor overlap on same side of disk

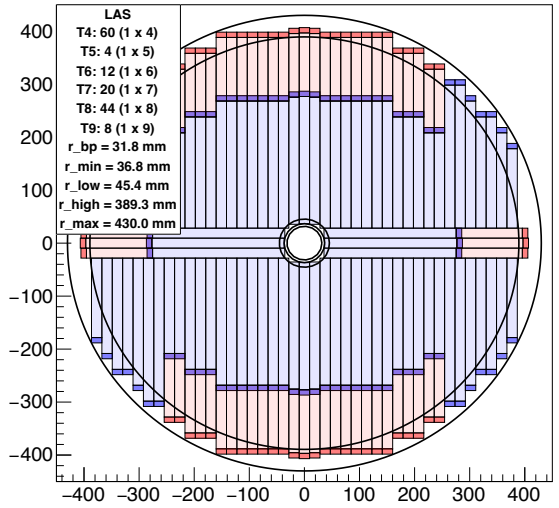
  Sensor variants are assumed to be 1 reticle width by up to 9 reticle lengths

EIC-SVT Disk-1 Tile



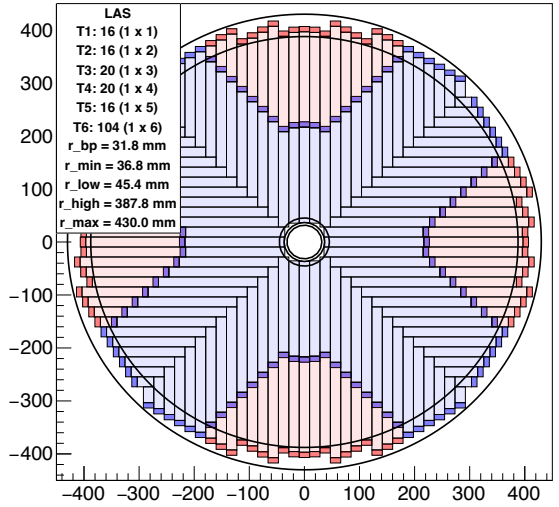
- Disk 2 – restricting sensor size

EIC-SVT Disk-2/3n Tile



148 sensors
896 reticles
Fewer, longer sensors
T4 – T9

EIC-SVT Disk-2/3n Tile

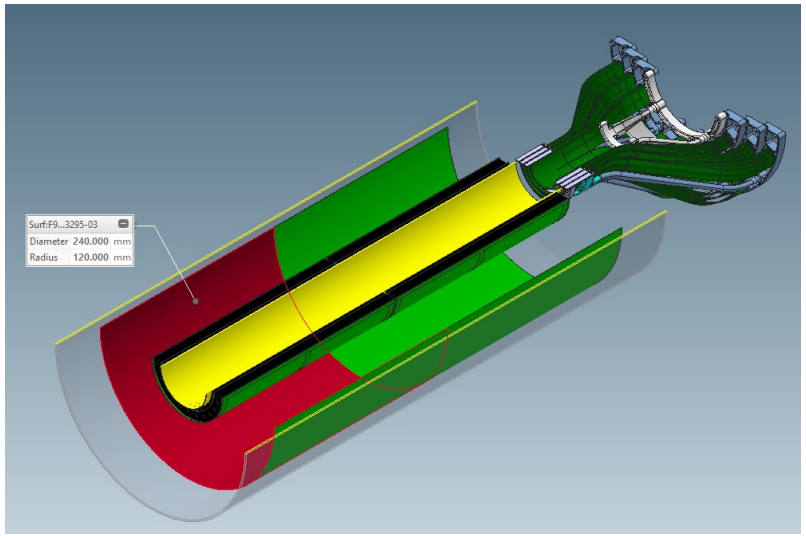


192 sensors
892 reticles
More, shorter sensors
T1 – T6

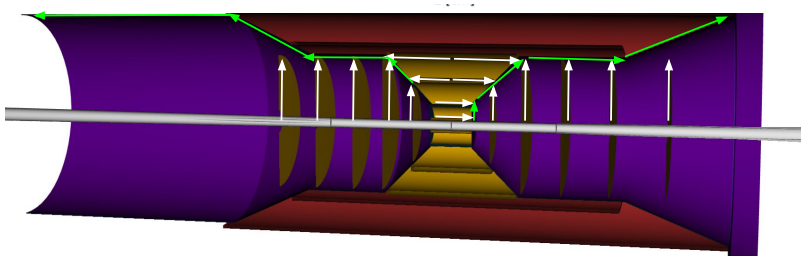
WP1.3 – Modules and System Tests

- Mechanical design

Work has started on modifying ITS3 mechanical design for the vertex layers



Need to address cable routing, cooling and compatibility with EPIC support cone



WP1.3 - Modules and System Tests

- Serial powering scheme chosen as baseline for the ePIC SVT

  Provides lowest material option

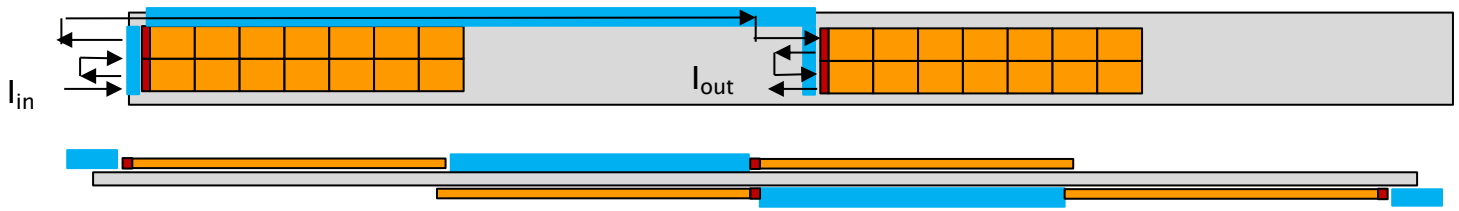
- Shunt-LDO placement on a dedicated powering chip outside the sensor

  Allows re-using of ITS3 sensor on-chip power distribution; Does not require modification of sensor periphery; Can be prototyped and fabricated in cheaper technology

- SP scheme drafted for sagitta layers

  Current flowing between sensors on each side of the stave

  Factor 4 current reduction for L4, factor 2 current reduction for L3

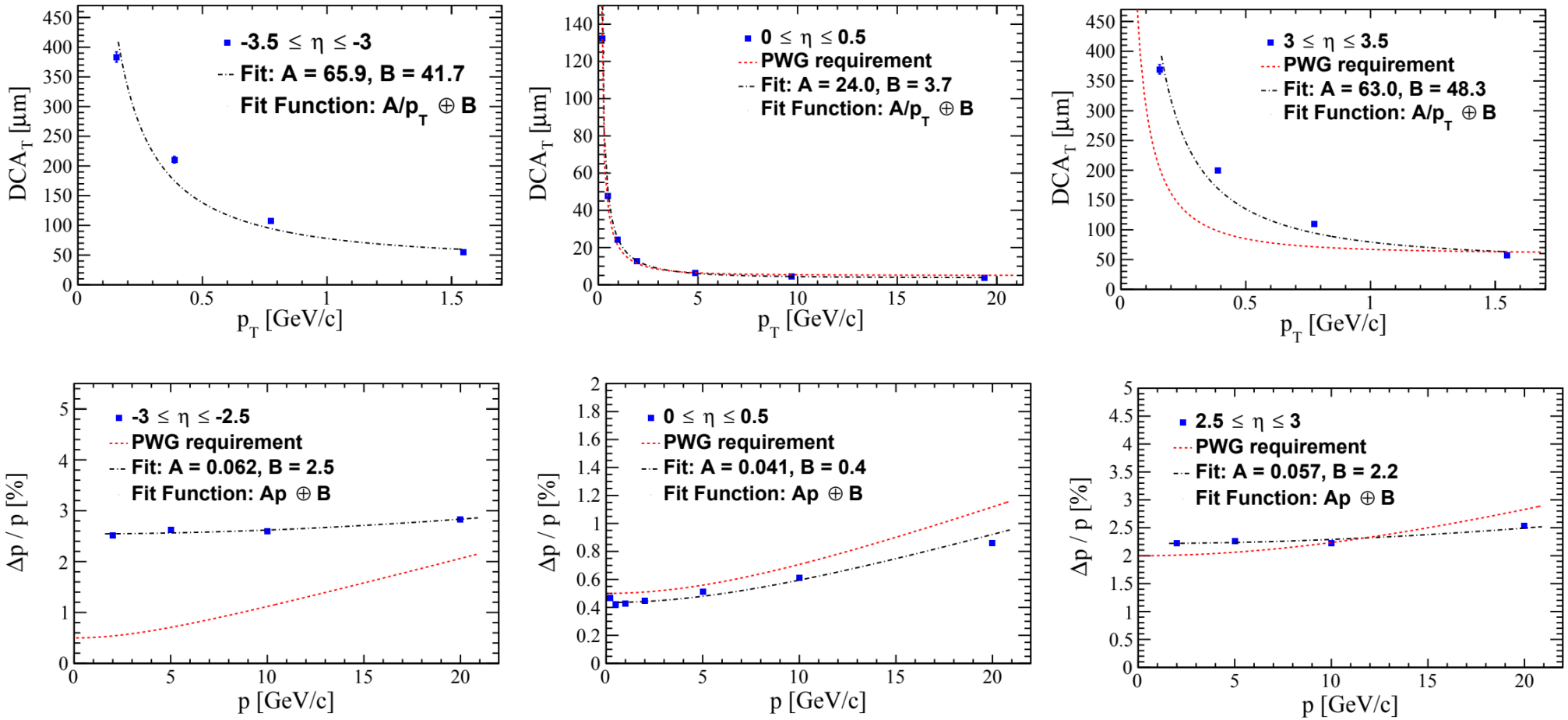


L4 serial powering scheme;
top – stave top view, bottom – stave side view

- Number of sensor low voltage and bias cables estimated and provided to EIC project engineers for integration exercise

WP1.4 - Detector layout simulations

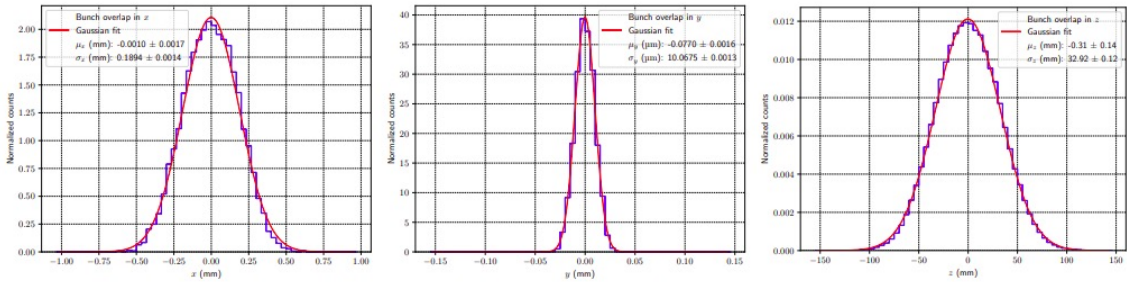
- Parametrised momentum and vertex resolutions with the latest ePIC tracker configuration

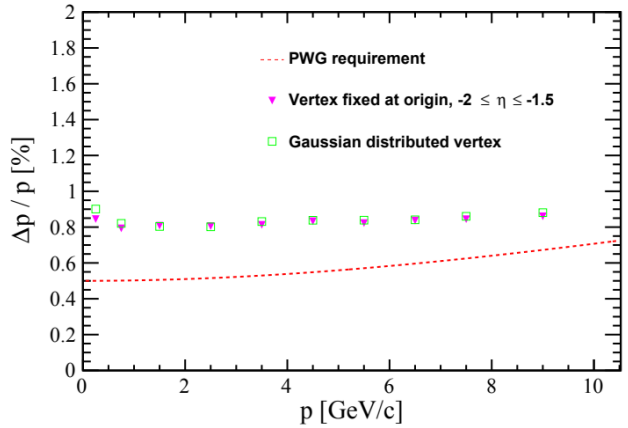


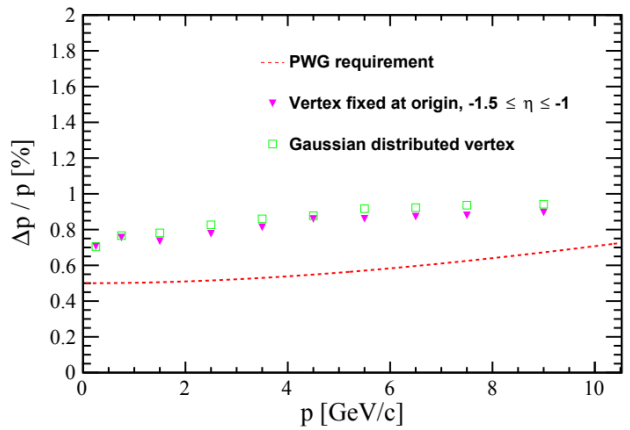
WP1.4 - Detector layout simulations

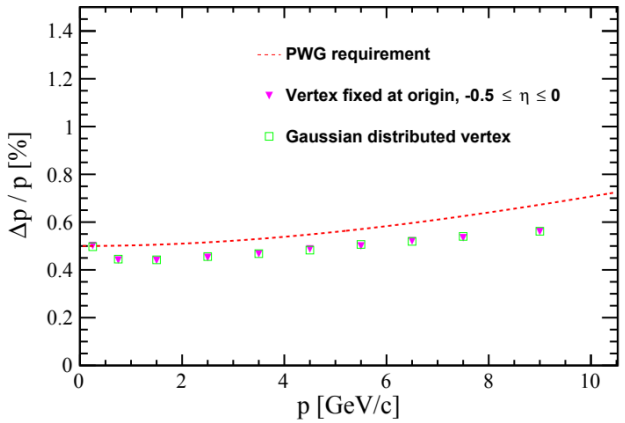
- Study of beam spot effect on the tracking performance

  Minimal degradation of momentum resolution in specific pseudorapidity intervals where particles traverse support material; no effect on the vertex resolution.







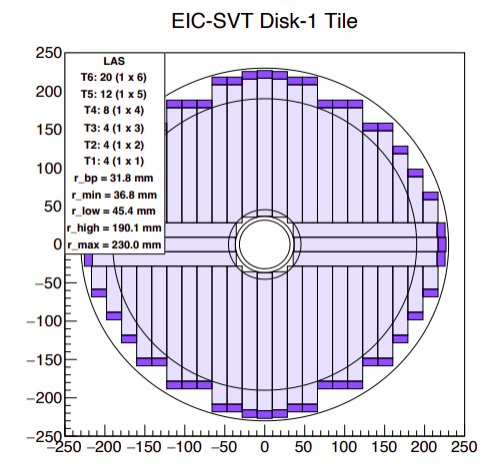


Same trend at forward pseudorapidity

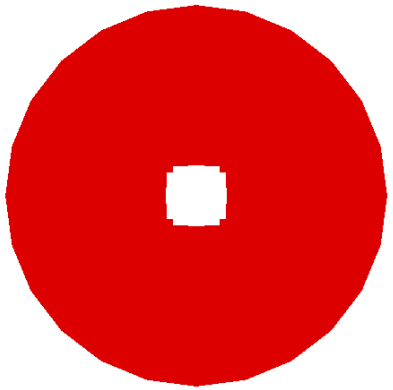
WP1.4 - Detector layout simulations

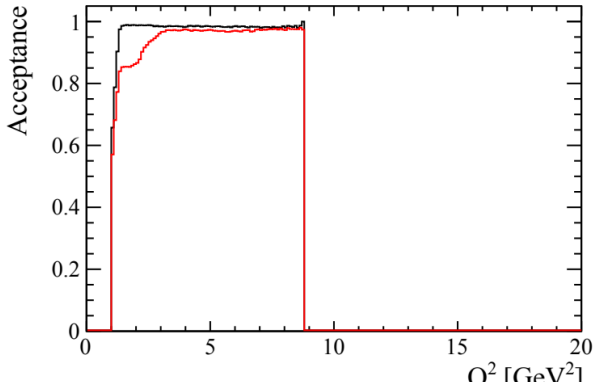
- Study of acceptance at large eta
- Realistic disk design implemented in simulation
- Higher x lower Q^2 bins lose acceptance
- Acceptance > ~80% for all bins Q2>1GeV² for 100% efficient disks

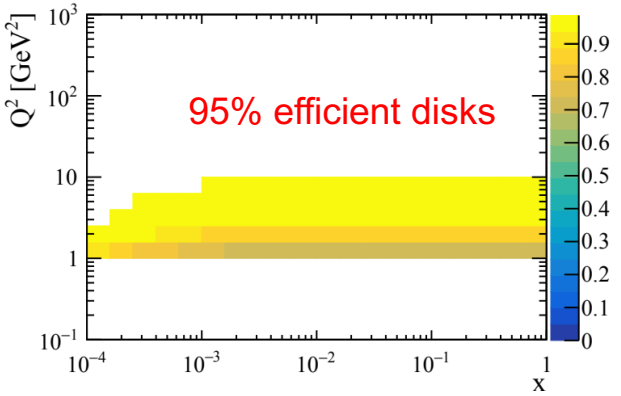
Example of disk configuration in tiling study

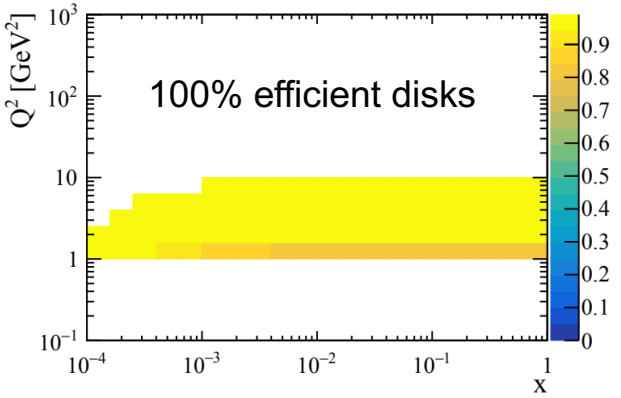


Disk implementation in simulation









WP1.4 - Detector layout simulations

- Study of barrel MPGD layer contribution to tracking

  Different combinations of active silicon, MPGD and Time of Flight (TOF) layers

  Momentum and vertex resolution fully defined by SVT, with small improvement by TOF layer; no recovery in performance with the MPGD layer active in case of failure of one silicon layer; barrel MPGD layer contribution in pattern recognition only