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U.S. DEPARTMENT OF ENERGY

Interests and planned contributions to the ePIC SVT

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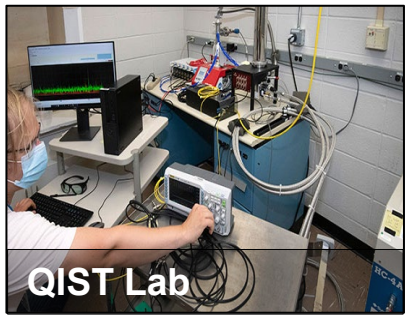
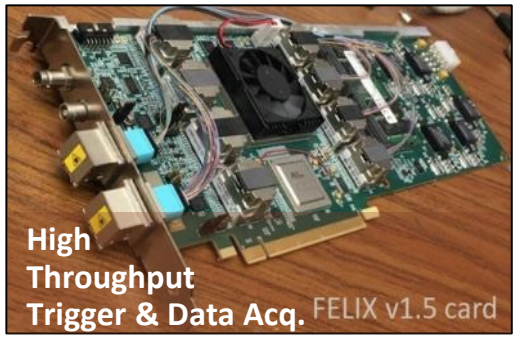
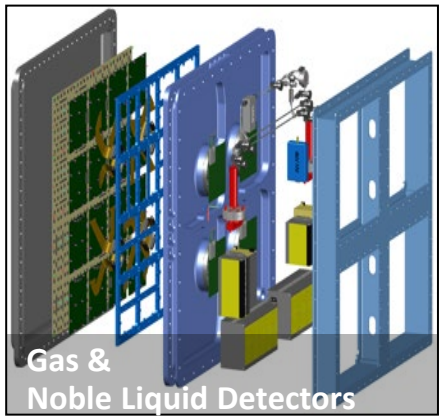
Instrumentation Division
Radiation Detectors Platform

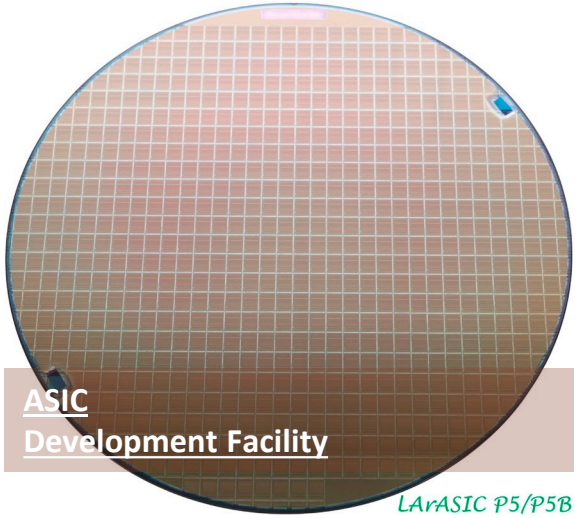
key capabilities enabling BNL Science Programs:

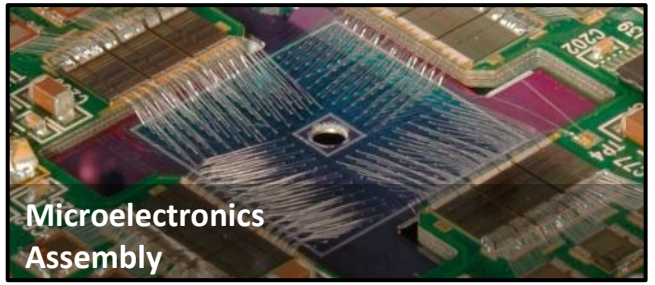
- Sensors Si – CdTe – CdZnTe – Ge – Se – Perovskyte
- Gas & Noble Liquid Detectors
- Application Specific Integrated Circuits (ASICs)
- CAD for Device & Board Level Circuit Design
- Microelectronics Assembly and High-Density Interconnect
- High Throughput Trigger and Data Acquisition
- Photocathode Development & Production (for detector and accelerator applications)
- Quantum Information Science Laboratory











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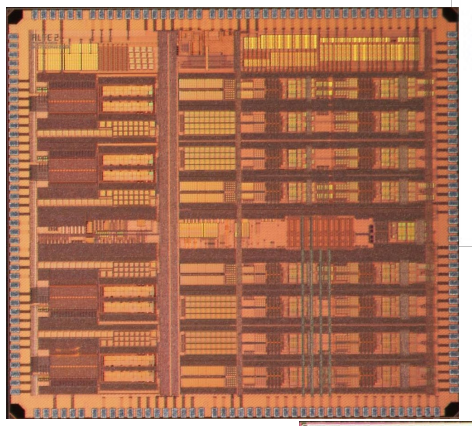
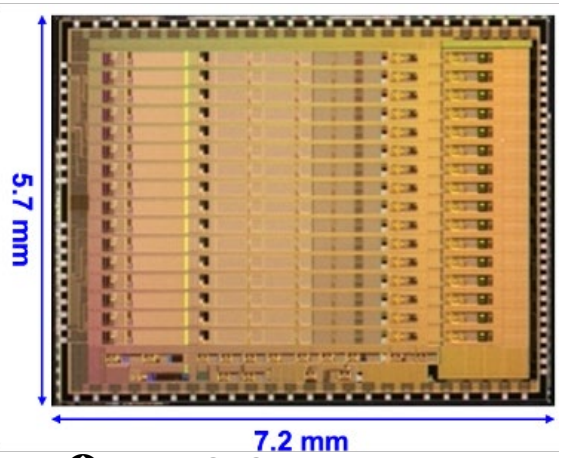
https://www.bnl.gov/instrumentation/

ASIC People and CAD/EDA Tools

Expertise in low-noise, low power, large mixed-signal designs

- 8 full time ASIC designers
  (5 PhDs + 2 in PhD program, including industrial background)
- ongoing targeted hiring for satisfying needs across multiple programs
- open for hosting guest/visitors and grad/post-grad students
- hand-in-hand with in-house TDAQ, PCB, sensors and other groups

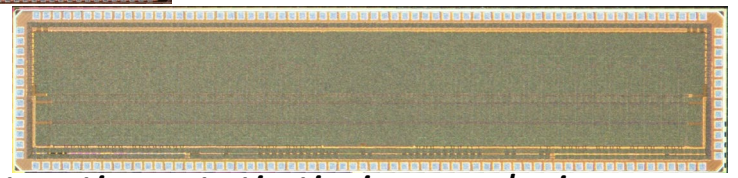




LArASIC_P5B 180 nm

ALFE2 130 nm

AVG_DEV 65 nm



Design tools and methodologies

- industry-standard tools from Cadence, Siemens (Mentor), etc.
  (analog on top or digital on top flows)
  analog: full custom flow (VSE, VLE, ADE/Spectre, AMS, PVS, XACT3D-PEX)
  digital RTL2GDS: functional simulation, logic synthesis, automated P&R, parasitics extraction, static timing analysis (XCELIUM/GENUS/INNOVUS/QUANTUS QRC/TEMPUS)
  library characterization: custom standard cell libraries for designs for extreme environments: cryogenics and radiation
  verification: IR drop (VOLTUS/ VOLTUS-fi), functional (SV), physical (PVS, Calibre DRC/ERC/LVS)
  device modeling: TCAD, FEM solvers, transistor model parameter extraction (Silvaco ATHENA-ATLAS-VICTORY, Maxwell, UTMOTS4)
- foundry PDK's: *TSMC CMOS 350nm - 65nm, GF CMOS and BiCMOS SiGe 130nm, 90nm, + specialized processes: monolithic CIS on HR TPSCo, sensors co-design, High-Voltage etc.*
- access to foundries via: MOSIS, CERN-IMEC Foundry Services, IMEC and directly
- packaging: in house custom and through commercial sources

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EIC-SC ➡ ePIC SVT (2023)

Transfer of the current scope of contributions carried out under EIC SC to ePIC SVT

- **Implementation of the scope included in the current eRD113 (sensor development and characterization) in accordance with the capabilities and limitations of the TPSCo 65 process:**
  - selected project contributions to be included in ALICE ITS3 sensors,
  - oriented specifically to the ePIC SVT.

Currently 3 ASIC designers involved.

eRD113 proposal
https://wiki.bnl.gov/conferences/index.php/ProjectRandDFY23

eRD113 report
https://indico.bnl.gov/event/19740

- **Contribution to other areas across coverage of eRD104 and eRD111 areas:**
  - powering and grounding including system aspects of the sensors,
  - data acquisition interfaces,
  - mutual impact mechanics and sensor concept,
  - testing and characterization infrastructure.

growing efforts

Currently 2 people part time involved.

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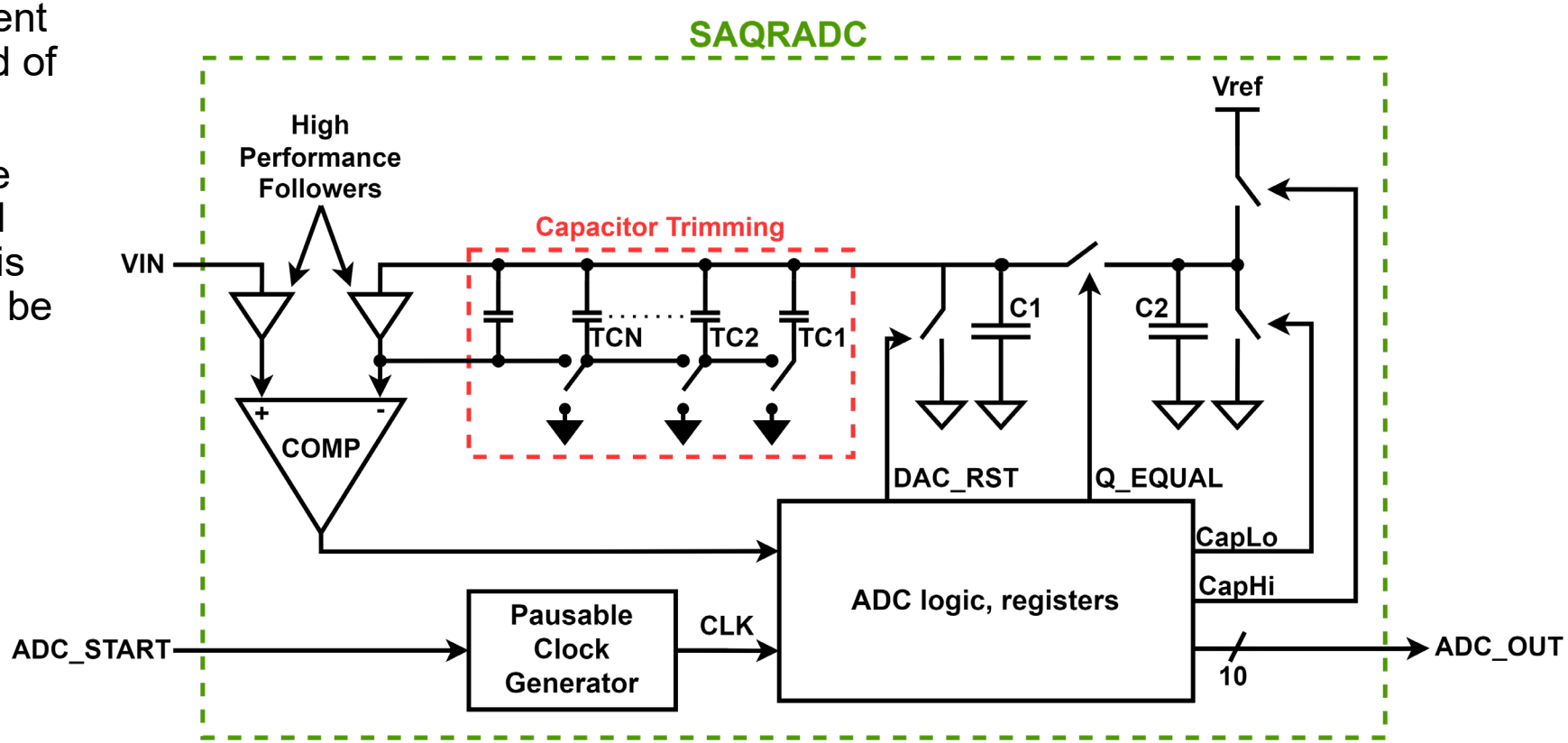
Contribution: VFM_ADC

- Monitoring of essential signals and levels within an ASIC (temperature, bias voltage/current values, etc.) requires some kind of processing on analog,
- Standard ADC architectures are large, power-hungry, and suited for running continuously which is not necessary as the signals to be monitored need to only be checked on occasion,
- Compact, low-power ADC that can run on command while shutting itself down while not in use is pursued.

Key Features:

- 10-bit resolution
- Pausable clock generator
- DAC with 2 sampling capacitors of ~220fF

A compact Succesive Approximation Charge (Q) Redistribution (SAQRADC) ADC running off of a pausable clock generator



- Capacitor trimming to tens of attofarads
- High gain comparator with \high performance source followers with gain > 0.999 and Cin < 0.1fF

IEEE JSSC, 10(6), 379–385

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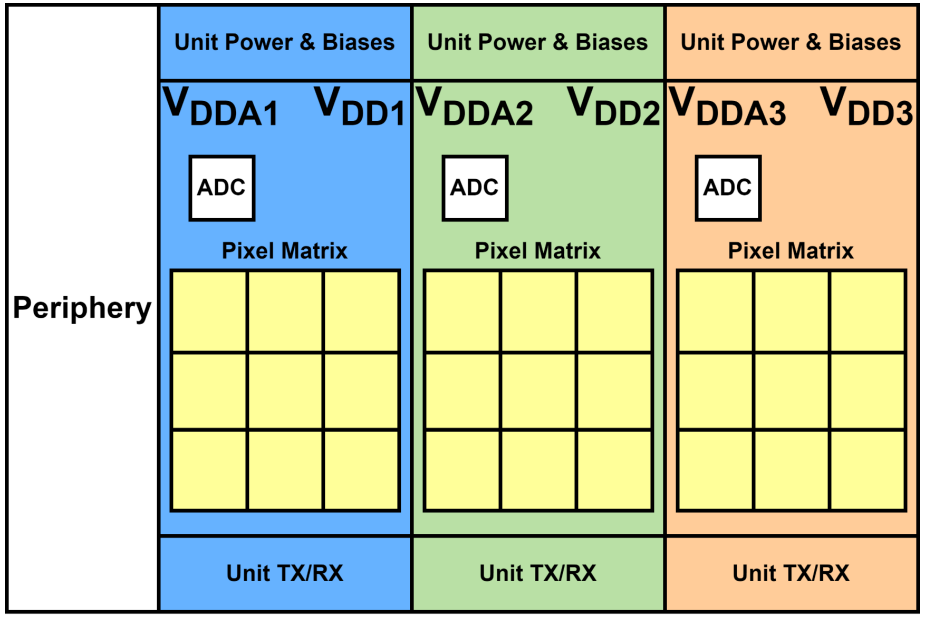
Presented at:
https://indico.cern.ch/event/1285331/contributions/5401017/attachments/2645783/4579639/ER2_Presentation.pdf

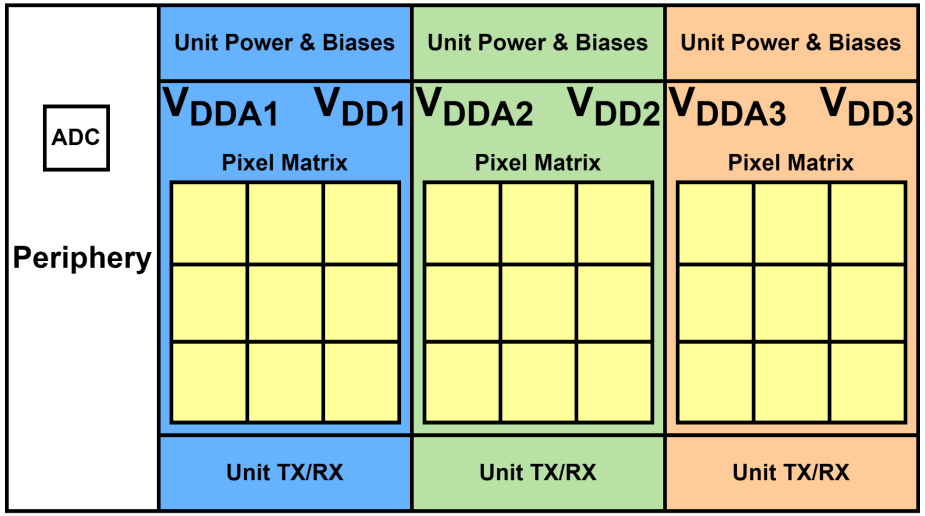
Placement of ADC

- The area in which the ADC is placed is a critical decision
- There are two proposed options to consider:
  - **Option 1:** Place an individual ADC within each repeated sensor unit (RSU)
  - **Option 2:** Place ADC within the periphery

design of VFM_ADC is heading towards completion as a standalone, insertable block.



Option 1



Option 2

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EIC-SC ➡ ePIC SVT (2024)

- **Continuation of eRD113 with the scope adjusted through**
  ASIC:
  - Continue on started design contributions (VFM_ADC, LDoC_ULVS, LP_StCells, etc.),
  - Extend on elements decided as needed in the past year, e.g., TDMA at the interface to high-speed links,
  - Maintain database and coordinate design assembly/integration of design of ePIC SVT for fabrication submission,
  - Develop technology suitable for operation with improved timing (FE + ReadOut) and layout arrangements [start with generic R&D].

  Leverage capabilities in HDI/DAQ/Sensors
  - Progress (facility open for use) Large Area Sensor testing and characterization-oriented capabilities, including 12” wafer probe testing,
  - Postprocess Large Area Sensor slabs driving resources and powering using Al redistribution layers.
- **Strengthen contribution to:**
  - powering and grounding, data acquisition interfaces, mechanics v.s., sensor concept (…),

Target:

Maintain 3 ASIC designers (≥3), 3 people (1 person per each area) powering and grounding, data transfer, mechanics

- definitively activity in WPs, and contribution to other dependent upon funding
- share and work with collaborating institutions

- WP1 – Sensor development
- WP3 – Sensor and electrical interfaces
- WP4 – Readout and powering
- WP5 – Integration

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Reserve Slides

ALICE ITS3 – ePIC MAPS development

Areas highlighted as desired contributions to the ALICE-ITS3 MAPS (04/25/2023):

- (**SRAM**) Development of dual-port Static Random Access Memory (SRAM), either as a compiler code or at least as full custom block (TPSCo 65nm contains single port SRAM compiler and it does not use DFM recommended rules) for buffering data for data transmission at the Repeated Sensor Unit (RSU) peripheries.
- (**LP_StCells**) Development of standard cells library (take care of the subset of cells) oriented on Low-Power (non-minimum Lengths of FETs) and respecting recommended rules, target 9T version, including timing characterization with Liberate (**BNL/RAL interested**).
- (**HV_StCells**) Development of standard cells, minimal subset, suitable for operation at HV (required for power management, i.e., operation when no core power is ON).
- (**VFM_ADC**) Development of small footprint ADC for Vital Functions Monitoring (VFM) with interfacing circuitries suited for connecting signals to be monitored and interfacing to slow control and fetching data to output through slow control of data stream interface (**BNL started**).
- (**LDoC_ULVS**) Development of Long-Distance on-Chip (LDoC) Ultra-Low-Voltage Signaling (ULVS) data transmission for sending data from stitched Repeated Sensor Units (RSU) to the peripheral area, where Time Division Multiple Access (TDMA) interrace connects to the lpGBT IP for data aggregation of high-speed links for data transfer off MAPS sensors (**BNL interested**).
- (**F_D/R**) Development of fast driver/receiver blocks (**RAL already involved**).