INFN interests for ePIC SVT

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- Participating groups (contacts): Bari (D. Elia), Trieste (G. Contin), Padova (R. Turrisi)

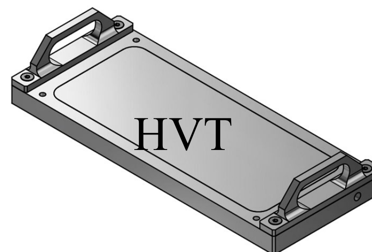
- Ongoing activities for ALICE ITS3:
  - ✓ Bari: bending and interconnection studies, development of super-ALPIDE prototypes, test of APTS OP-AMP
  - ✓ Trieste: bending, test and characterization of flat and bent DPTS, preparation of bent APTS SF samples
  - ✓ Padova: test and characterization of APTS SF, setup for testing DPTS in preparation
  - ❖ Bari and Trieste coordinating the ITS3 - WP4 “Bending, thinning and interconnections” (D. Colella, G. Contin)
  - ❖ Trieste coordinated the DPTS characterization campaign within ITS3 so far

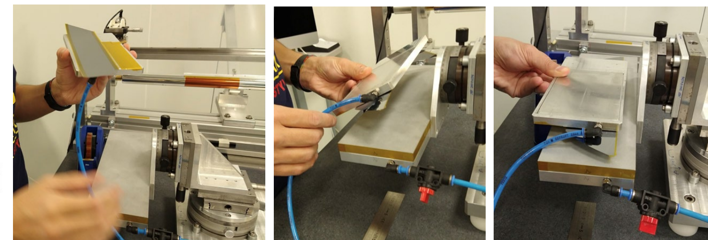
- Current involvement/activities in EICSC and tracking WG:
  - ✓ eRD111 (since FY22): *Forming modules from stitched sensors* ➔ *30 k$ for FY23*
  - ✓ eRD113: *Progress in testing and characterization* ➔ *30 k$ for FY23*
  - ✓ gen. R&D: *Additive manufacturing of power&data redistribution layers on thin large-area silicon* ➔ *49 k$ for FY23*
  - ✓ simulation studies with Fun4All/DD4HEP vs fast simulation, development of Root-based event display (S. Kumar)

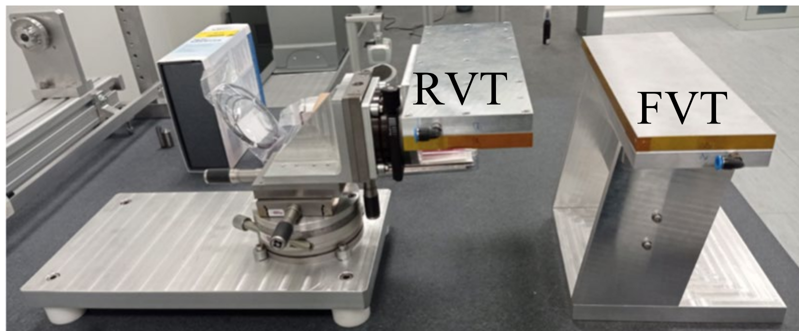
Activity for vertex layers
Silicon bending procedure and tooling

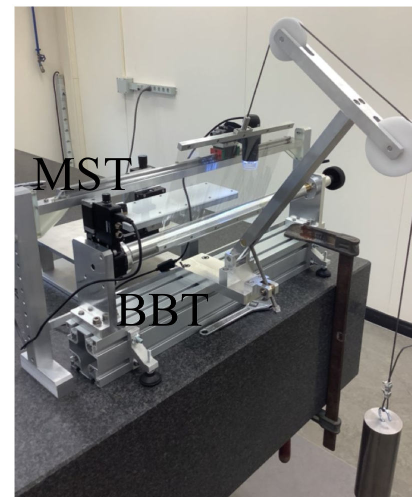
LIST OF TOOLS

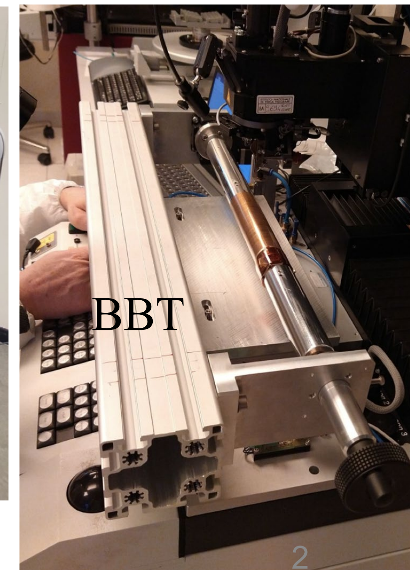
1. Fixed vacuum tool (FVT)
2. Rotating vacuum tool (RVT)
3. Handling vacuum tool (HVT)
4. Microscope tool (MST)
5. Bending Bonding tool (BBT)











Activity for vertex layers
Silicon interconnection to flex

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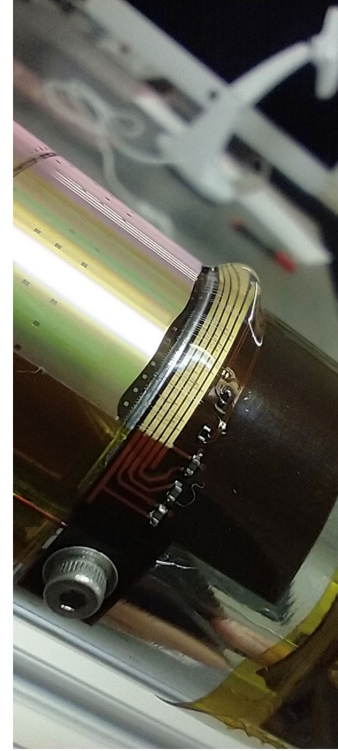
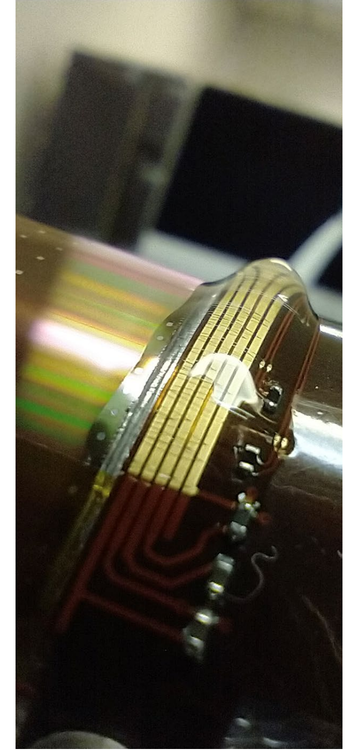

Activity for vertex layers
Support structures gluing to the sensor

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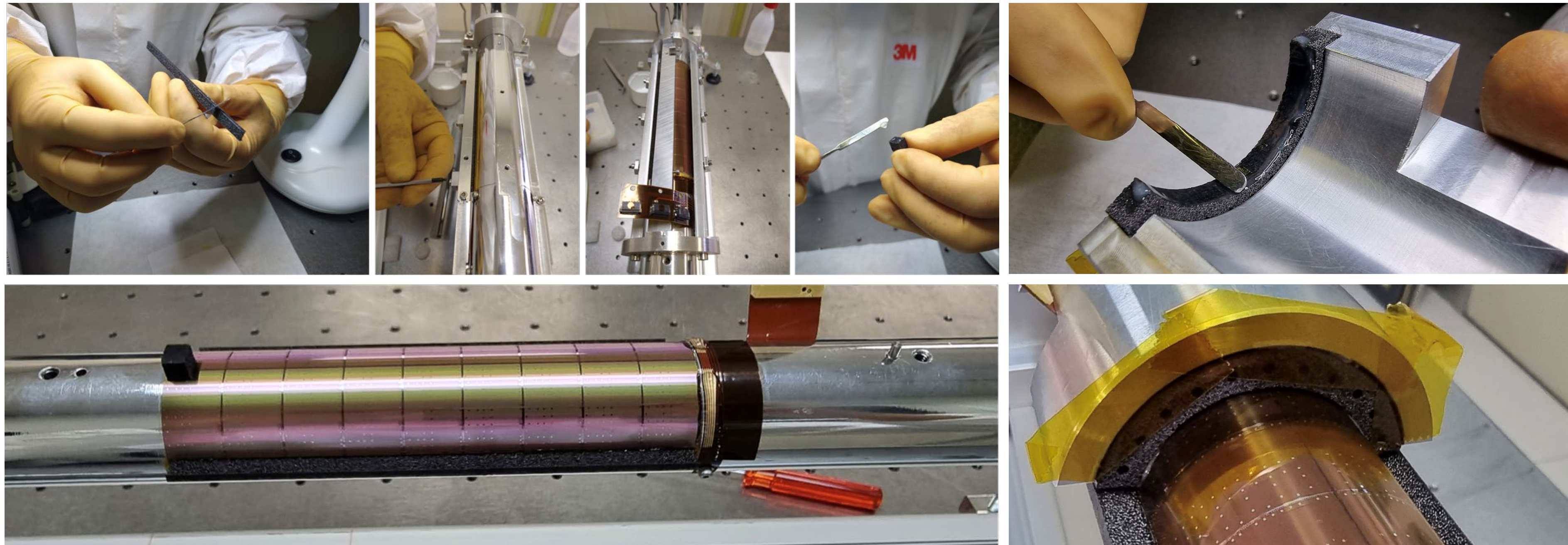

Bending and testing 65 nm CMOS chips

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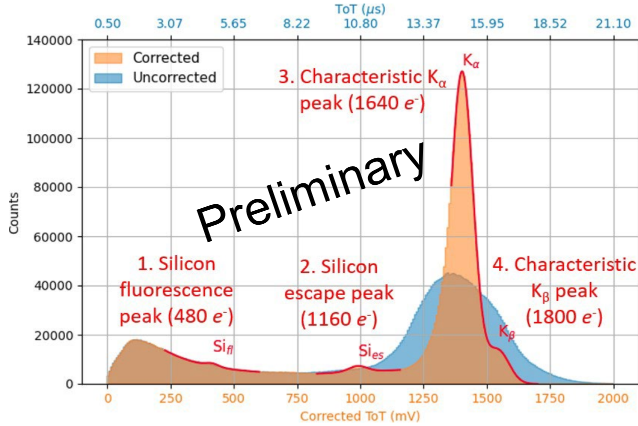
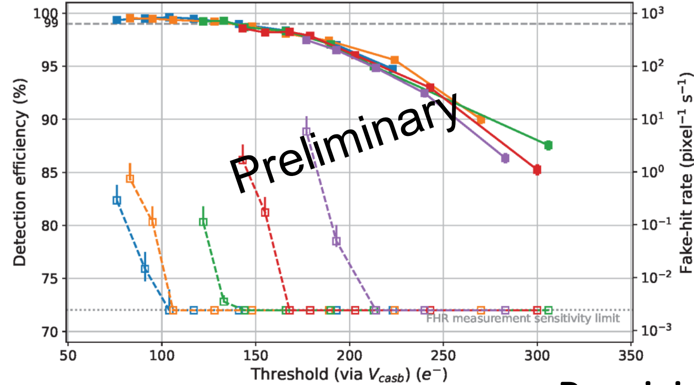
- Response to Fe55

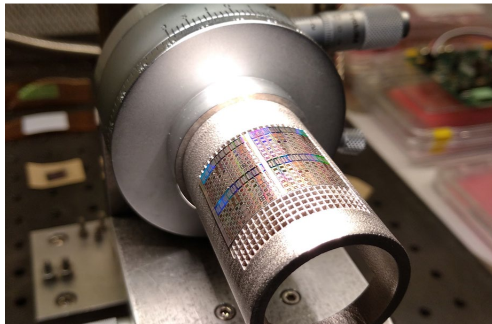


- Efficiency measurement with MIPs

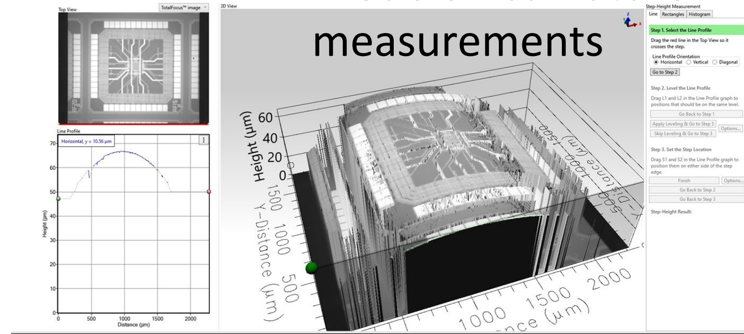


DPTS paper pre-print: https://arxiv.org/abs/2212.08621

- Reticle Bending



- Precision curvature measurements



Planned contributions to the ePIC SVT

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- Funding and labor force
  - ✓ Project not officially funded yet, ~1M$ in-kind contribution to SVT is foreseen for construction phase
  - ✓ Scientific staff ramping up to 3-5 FTE during R&D phase + technical personnel. Expected to grow for construction, to be defined

- R&D for vertex layers
  - ✓ **Bending and interconnections** based on bending/interconnection/prototyping activites for ITS3
  - ✓ General contribution on **sensor test and characterization** (also connected to the eRD111 targets for this year)
  - ✓ Contribution to **FPC development and testing**

    ➔ overall effort **to be better defined** based on effective dedicated labor force growing in the groups

- Construction of vertex layers
  - ✓ Possible **in-kind** contribution to **silicon production runs, thinning and dicing**
  - ✓ Considering specific construction items compatible with ongoing R&D and available labor force, for example:
    - ✓ On-wafer large-area **sensor probe testing**
    - ✓ **FPC** production and integration
    - ✓ Participation in **chip bending and layer integration**
      - ➢ **To be decided** based on the other groups' interests and the available resources