	Present design	First five EIC tiles	Final EIC tiles	Comments
Size, active area, material budget				
Sensor size	~120 mm	~120 mm	120 mm$^{+0\mu m}$	Should stay the same, but meet the increased active area requirement, see below
Active area size	100 mm	104 mm	108 mm	Geometric efficiency optimization; final goal: achieve >80% *fully efficient* active area fraction
UV Grade Fused Silica window thickness	5.0 mm	5.0 mm	4.0 - 5.0 mm	As requested based on Monte Carlo studies
Anode base plate thickness	3.3 mm	3.0 - 3.3 mm	3.0 mm	Minimized to the extent technologically possible
Transfer gaps	no specs	1.0 - 2.0 mm	1.0 - 1.5 mm	Minimized to the extent possible
Side wall width	>4 mm	>4 mm	~3 mm	Optimized for 80% active area requirement
Window tapering	straight	straight	with edge facets	If requested based on Monte Carlo studies
Window edge coating	none	none	reflective	If required by the detector design
Window to Lower Tile Assembly to Anode Alignment	no specs	no specs	< 200 μm	Assume placing tiles in the ~121mm size pockets
MCP configuration				
MCP stack (chevron)	no gap	with a gap	with a gap	Higher gain, more flexible operating voltage choice
MCP pore size	10 μm	10 μm	10 μm	
MCP pore pitch	13 μm	13 μm	13 μm	
MCP thickness	600 μm	600 μm	600 μm	
MCP pore bias angle	13^0	13^0	optionally considered up to 30^0	In case further optimization for a particular magnetic field configuration is required
Resistivity	no specs	no specs	Narrow range to be specified	Given at a gain of $5*10^6$; minimization of a single pore recovery time is a consideration
Internal HV connections				
Spring loaded interface between anode base plate and MCPs	no specs	new robust interface	new robust interface	Design to pass inspection by an authorized EIC electrical engineer
External connectivity				
Anode base plate design	uniform outer pixellation	matching the selected readout PCB	matching the selected ASIC PCB interface	A configurable multi-layer Low Temperature Co-fired Ceramic solution matching the PCB design
ASIC PCB interface	none	optimal out of options (1) … (2)	optimal out of options (1) … (2)	Identify and implement the best option out of: (1) high density compression

				interconnect, (2) conductive epoxy screen printing
Ground and MCP HV connection	rear side pads	rear side pins or a similar solution	rear side pins or a similar solution	Matching 24 AWG 1.27 O.D. Teflon isolated wire interface
Photocathode HV connection	side wall spot	side wall spot	rear side pin	Same as the MCP HV pins
Electrical safety				
Indium seal electrical isolation	none	none	isolated	Design to pass EIC safety inspection
Active area pixellation	32x32	32x32	on demand, up to 2.5-3.0 mm pad size	Develop capability to implement application-specific pixellation in case EIC RICH and DIRC detectors require different granularity of the anode plane
Environmental & lifetime specs				
Indium alloy melting point	72^0 C	72^0 C	$>100^0$ C	QA thermocycling procedure to be worked out by EIC personnel
QE and gain loss at the extracted charge of 10 C/cm^2	no specs	<10% relative to the initial value	<10% relative to the initial value	Procedure used at UT Arlington to be verified as a reliable non-invasive technique
Performance				
Gain at the photocathode (PC) voltage of 100 V or higher (as required for a high timing resolution)	no specs	$>5*10^6$	$>5*10^6$	Maximum gain at a stable operation; to be used mainly as an indirect quality indicator, since the actual gain in the experiment will most likely be much less than 10^6
Gain non-uniformity across active area	no specs	<20 % RMS	20% with goal <15% RMS	The uniformity is less critical for DC-coupled sensors with a very limited charge sharing
Single photon transit time spread (TTS)	no specs	<60 ps	< 50 ps	As measured at BNL using a femtosecond laser and a high analog bandwidth scope, or a similar equipment
Dark count rate (DCR)	no specs	<2 kHz/cm^2	<2 kHz/cm^2	Evaluated at the PC voltage of 100 V or higher and a gain of 10^6
Quantum efficiency (QE)	no specs	peak value above 27%, with a goal of 30% average across the five sensors	peak value 28-30% or higher across the produced batch	At 330-370nm, measured as an **average value across** the whole active area, using photocathode current against a calibrated photodetector equivalent
QE non-uniformity across active area	no specs	<10% RMS	<10% RMS	Relative to peak value; less important than a high *average* QE across the whole active area
Collection efficiency (CE)	no specs	>80%	>80%	At a threshold used to evaluate the DCR metric, see above; measurement procedure to be worked out in the design phase

(Peak QE)*CE product	no specs	>25%	>25%	An alternative metric, ultimately critical for the experiment, in case individual QE or CE parameters are below the specifications above

Table outlining the detailed specifications for the HRPPDs, in various categories. The column with "First five EIC tiles" is the subject of the PED contract. The column with "Final EIC tiles" is illustrative only to outline what is envisioned as the final HRPPD requirements for the EIC detector.