EIC AC-LGAD R&D Proposal: FY22 report & plans for 2023 and beyond

IJCLab, CEA-Saclay/Irfu/DEDIP and OMEGA, France

September 30, 2022

1 Motivation and requirements for EIC Roman Pots

The future Electron Ion Collider (EIC) [1], which is being built at Brookhaven National Laboratory (New York, USA), aims at studying the internal structure of nucleons and nuclei in terms of their subconstituents and represents a unique opportunity to unravel the role of the gluons that bind the building blocks of visible matter in the Universe.The EIC will start operations in the early 2030s.

The high luminosity of the EIC will allow studying the three-dimensional structure of hadrons through hard exclusive processes, such as deeply virtual Compton scattering (electron proton $\rightarrow$ electron proton gamma). This kind of process allows not only to access the longitudinal momentum fraction of the partons inside the hadron but also their transverse position with respect to the virtual photon that mediates the interaction. Exclusivity demands that all final state products are detected. Typically, the recoil proton (or ion) from these reactions is scattered at very low forward angle (< 5 mrad) with respect to the beam. An excellent time resolution of the order of 30 ps for a 10 fC charge deposited by a Minimum Ionizing Particle (MIP) is mandatory to resolve event-by-event a collision that occurred at the head or at the tail of the proton bunch. In addition, an excellent spatial (< 50 μm) resolution is required to ensure a resolution of 10 MeV/c in the transverse momentum measurement of the detected particles.

Thus, at EIC, a fundamental forward detector system has been suggested consisting of Roman Pots holding novel silicon pixelated sensors and located very close to the hadron beam line and far forward (30 m) from the interaction point in order to detect particles scattered at extremely small angles.

The foreseen sensors are a new generation of LGAD (Low Gain Avalanche Diodes) sensors with a capacitive coupling between the electrodes and the substrate, known as AC-LGAD. As DC-LGAD sensors, AC-LGAD show an excellent time resolution but relying on charge sharing between neighboring pixels a very good spatial resolution can also be achieved.

Signals produced by charged particles in the AC-LGAD sensor active volume are amplified via an internal p+ gain layer near the sensor surface. Signals induced on a continuous resistive n+ layer on top of the p+ gain layer, are AC coupled to patterned metal readout electrodes, which are on the sensor surface and separated by a dielectric layer from the n+ layer. The internal signal amplification and thin active volume enables precise timing measurement, while charge sharing among neighboring electrodes can provide precise position measurement. The AC-LGAD technology has been suggested to use for particle identification, tracking, and far-forward detectors at EIC where precision timing and spatial measurements are needed.

Within the framework of ATLAS (High Granularity Timing Detector, HGTD) and CMS (Endcap Timing Layer, ETL) detector updgrades for HL-LHC (High Luminosity runs at the Large Hadron Collider), large-area DC-LGAD detectors with 1.3×1.3 mm^2 pixel electrodes are being designed and tested.

For EIC, the goal is to produce and instrument large arrays of AC-LGAD sensors with pixel size down to 0.5×0.5 mm^2.

Past and ongoing efforts, as well as R&D needs and budget request to develop AC-LGAD-based full detector designs for EIC are detailed hereafter considering the 3 main R&D areas: sensors, electronics, and system design (including cooling, engineering, and construction).

2 “Electronics”

In term of electronics, The goal of the EICROC team is to develop an ASIC with a pitch size of 0.5×0.5 mm^2 to readout AC-LGAD sensors and to characterize the integrated sensor+ASIC detector system in an environment close to the experimental conditions.

The EICROC project relies on complementary teams with expertise in micro-electronics, instrumentation and semi-conductor detector characterization from French institutes (IJCLab, CEA-Saclay/Irfu/DEDIP and OMEGA) and from Brookhaven National Laboratory (BNL) also involved in the design and the production of AC-LGAD sensors for EIC.

While specific ASICs have been designed to readout DC-LGADs of ETL and HGTD, respectively ETROC [2] and ALTIROC [3, 4], the development of a dedicated ASIC optimized to readout novel fine pixelated AC-LGAD sensors is mandatory to fully exploit their potential in terms of time and spatial resolutions, taking into account their intrinsic properties (lower capacitance) and the signal sharing (sensitivity to small charges).

The needs for fast timing performance and finer granularity pose significant chal- lenges to the readout electronics and specifically to the ASIC readout chips. Present ASIC chips designed for CMS and ATLAS timing detectors have a jitter on the order of 20–30 ps, and a pixel granularity of 1.3×1.3 mm^2. Reduced granularity and better timing resolution requirement will make it more challenging to fit all the circuit components within the available space, and also likely lead to significantly increased power consumption due to increased total number of channels. The EIC Consortium is closely collaborating on addressing all these challenges.

2.1 FY22 report

While specific ASICs have been designed to readout DC-LGADs of ATLAS HGTD and CMS ETL, namely ALTIROC [3, 4] and ETROC [2], the development of a dedicated ASIC optimized to readout novel fine pixelated AC-LGAD sensors is mandatory to fully exploit their potential in terms of time and spatial resolutions, taking into account their intrinsic properties (lower capacitance) and the signal sharing (sensitivity to small charges). The goal of the EICROC team is to develop an ASIC with a pitch size of 0.5×0.5 mm^2 to readout AC-LGAD sensors and to characterize the integrated sensor+ASIC detector system in an environment close to the experimental conditions.

The needs for fast timing performance and finer granularity pose significant challenges to the readout electronics and specifically to the ASIC readout chips. Present ASIC chips designed for ATLAS and CMS timing detectors have a jitter on the order of 20–30 ps, and a pixel granularity of 1.3×1.3 mm^2. Reduced granularity and better timing resolution requirement will make it more challenging to fit all the circuit components within the available space, and also likely lead to significantly increased power consumption due to increased total number of channels.

The EICROC project relies on complementary teams with expertise in micro-electronics, instrumentation and semi-conductor detector characterization from French institutes (IJCLab, CEA-Saclay/Irfu/ DEDIP and OMEGA) and from Brookhaven National Laboratory (BNL) also involved in the design and the production of AC-LGAD sensors for EIC. In 2022, in close collaboration within the consortium (weekly meetings), the electronics activity was many folds:

- Measurements and data analysis by the BNL team of a system consisted of an AC-LGAD sensor wire-bonded to an **ALTIROC0** chip using a Beta source (^{90}Sr) and exploiting an infrared laser test bench,

- Measurements and data analysis by the IJCLab team of a system consisted of an AC-LGAD sensor wire-bonded to an **ALTIROC1_v2** chip using a Beta source (^{90}Sr). Based on the BNL IR laser test bench, all equipment have been ordered to set-up an IR laser test bench at IJCLab,

- Relying on simulations developed at IJCLab and OMEGA, an ASIC prototype has been designed involving the CEA-Saclay/Irfu team for the TDC and collaborators from AGH University of Science and Technology (Krakow, Poland) for the 8-bit ADC (Analogical to Digital Converter). The chip design has been submitted for fabrication at the end of March 2022 and EICROC0 chips have been received at the end of July 2022.

- The dedicated printed circuit board (PCB) which holds the EICROC0 and the AC-LGAD sensor has been designed by the OMEGA team, fabricated and 10 pieces were received at the end of July 2022. The PCBs have been cabled at IJCLab. PCBs and EICROC0 chips have been shipped to BNL for the wire-bonding.

- A ZC706 Xilinx board acting as the interface board to control EICROC0 parameters has been provided and the associated firmware has been developed by IJCLab team.

All the FY22 costs have been covered by funds granted by the LabEx P2IO [6] (Université Paris-Saclay, France) for the period 2020-2022 within the call "Projets Emergents" (AC-LGAD Project), French institutions has thus provided in-kind labor and material contributions during 2022. Below we present these works.

2.1.1 Studies based on (HGTD) ALTIROC0 chip (BNL)

Publication and presentations. To be completed by BNL

2.1.2 Studies based on (HGTD) ALTIROC1_v2 chip (IJCLab):

ALTIROC1_v2 is a 5 × 5 pixelated ASIC designed by OMEGA in 130 nm node technology for ATLAS HGTD [5]. It holds 2 kinds of Pre-Amplifiers, 15 Voltage Pre-Amplifiers (VPA) and 10 Trans-Impedance Pre-Amplifiers (TZ). Each channel uses two Time Digital Converters (TDCs), one measuring the Time-Of-Arrival and the other the Time-Over-Threshold (TOT) as an estimate of the signal amplitude to correct for time-walk effect. This ASIC which was designed to read out HGTD DC-LGAD sensors with 1.3 × 1.3 mm^2 pixels is used as a stepping stone to read out AC-LGAD sensors and to constrain the design of a proper ASIC prototype.

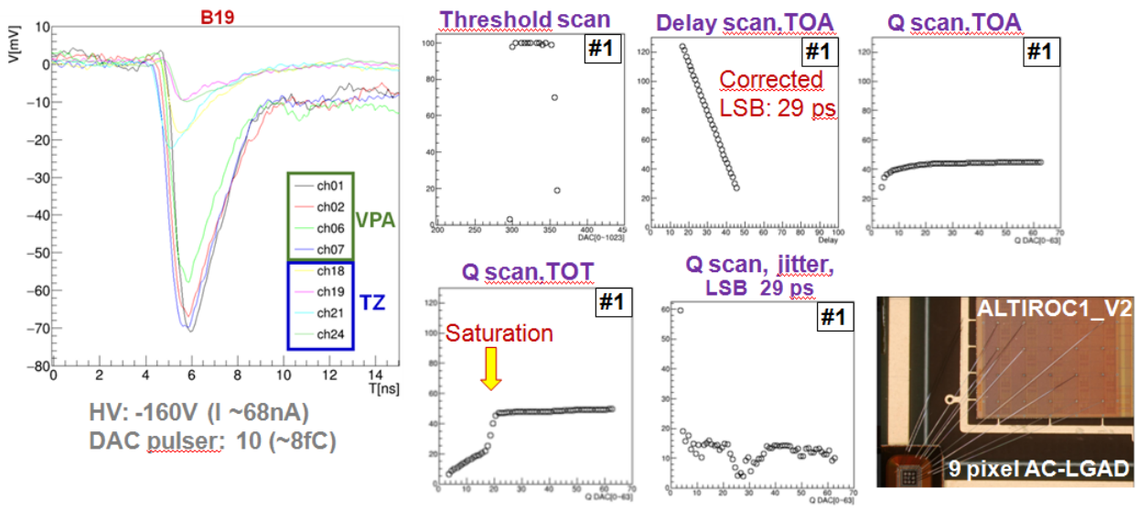

Figure 1: Left: observed ALTIROC1_v2 pre-amplifier signal amplitudes corresponding to a ∼ 8 fC input charge for each channel connected to a pixelated 3 × 3 AC-LGAD sensor biased at -160 V. Right: results from threshold scan, delay scan, and injected charge scan (TOA and TOT). The picture on the bottom right shows a 3 × 3 AC-LGAD sensor wire-bonded to an ALTIROC1_v2 chip.

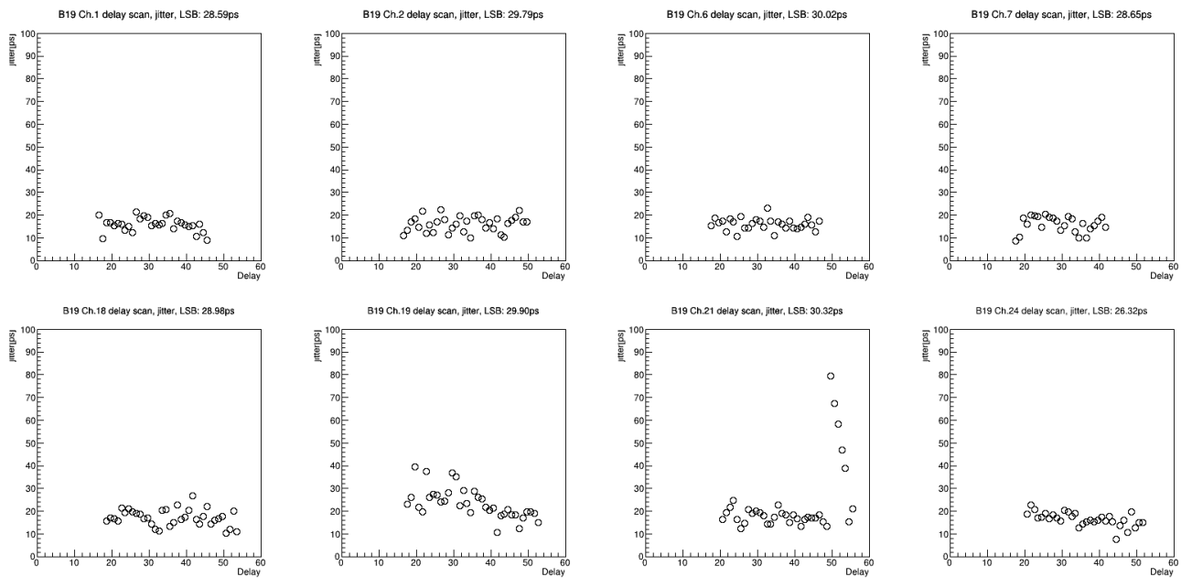

Figure 2: Measured jitter as a function of the delay in arbitrary units for each channel connected to the AC-LGAD sensor.

After each individual ALTIROC1_v2 channel on the printed circuit board #19 (B19) has been characterized using HGTD test bench at IJCLab to identify best working channels (TOA and TOT), the circuit has been shipped to BNL where 8 channels of a 3×3 pixelated AC-LGAD sensor have been wire-bonded to the ASIC and sent back to IJCLab in July 2021 where a characterization of each connected channel of the system ALTIROC1_v2 + AC-LGAD sensor has been performed.

Figure 1 shows on the left the observed pre-amplifier signal amplitudes from each AC-LGAD connected channels corresponding to an input charge of ∼8 fC when the sensor is biased at -160 V. The other plots concern channel 1, as an illustration, and have been obtained after scanning

the threshold, the delay (TOA), the charge (TOA and TOT). From the delay scan (TOA), the corrected Least Significant Bit (LSB) is found to be of the order of 30 ps for each connected TDC channel showing a uniformity among all channels (see Fig. 2). For TOT, while scanning the injected charge, an effect looking like a saturation is observed for most channels above an injected charge of 21 fC. After investigation, this "saturation" effect, already mentioned in [4] is due to afterpulses observed on the discriminator falling edge signal.

The threshold of each channel has been measured and the lowest detectable charge being about 2.5 fC makes us confident that the goal of 2 fC for EICROC can be achieved. The average jitter for each channel is of the order of 20 ps for an injected charge higher than 5 fC, which is in agreement with measurements and simulations performed earlier by ATLAS HGTD team, see Fig. 3 and [5].

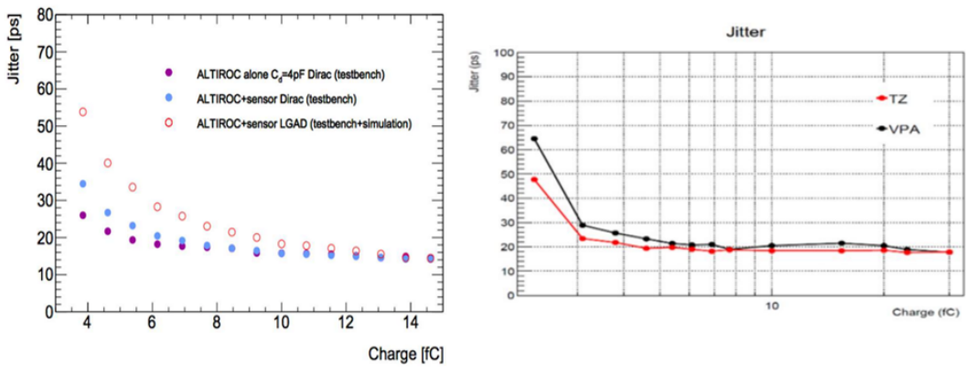

Figure 3: Left: ALTIROC1 measured and simulation-extrapolated total hit jitter for increasing input charges [5]. Right: jitter measured from VPA and TZ pre-amplifier AC-LGAD wire-bonded channels (HV -190 V) as a function of the injected charge.

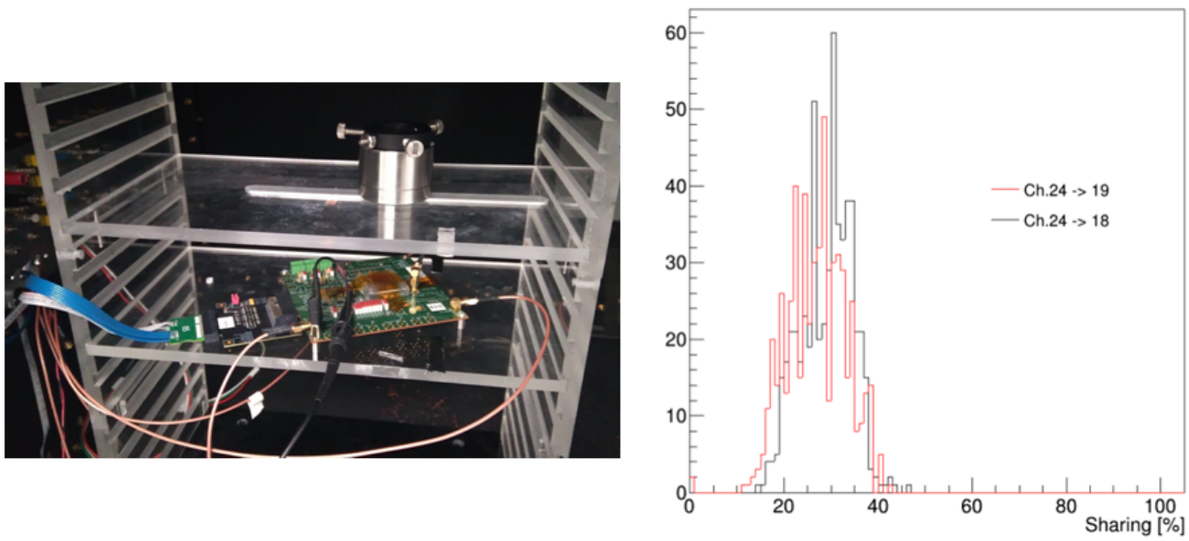

Figure 4: Left: experimental Beta source set-up. Right: amplitude distributions of channels #18 and #19 versus the charge sharing selecting #24 as the highest measured amplitude.

The charge sharing between pads/pixels has been studied exploiting ALTIROC (self) charge injection, using a beta source (^{90}Sr) and through simulations.

Using the ATLAS HGTD electronic test-bench, a study has consisted in injecting a 8 fC charge in one ALTIROC1_v2 channel and measuring pre-amplifier output signal amplitude in the neighboring pads placing the whole system in a black box. The resulting sharing was found to be of the order of 15% of the injected channel for 2 clusters: one involving VPA channels and one involving TZ channels.

A beta source (^{90}Sr, 37 MBq) has been used to acquire data with the system (ALTIROC1_v2 + 3 $\times$ 3 AC-LGAD sensor 8 channels wire-bonded) placed in a black box to screen from light. The experimental set-up is presented on Fig. 4 (left). Considering TZ connected neighboring channels (#18, #19 and #24), AC-LGAD biased at -170 V, the charge sharing was found to be of the order 30% for neighboring channels (#18 and #19) with respect to #24 selected as the highest measured amplitude (see Fig. 4 (right)). This result includes the TOT issue due to afterpulses observed at the falling edge of discriminators signals.

To study the charge sharing among pads, an electronics simulation modeling the charge injection has been developed considering a matrix of 12 pads and TZ pre-amplifiers, as illustrated on Fig. 5

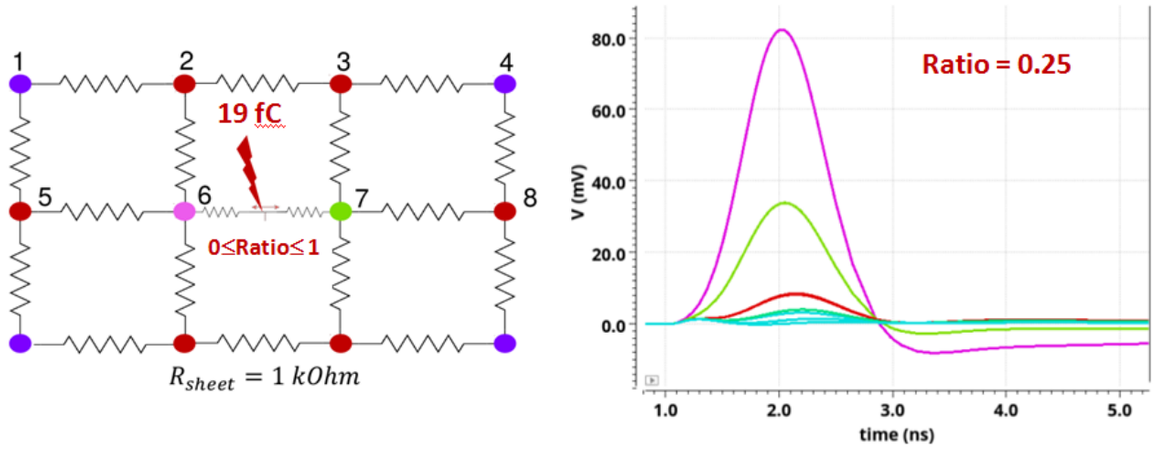

Figure 5: Left: schematic model of 12 pads on which rely the electronics simulation that has been developed to study charge sharing among pads. Right: pre-amplifier signal amplitudes corresponding to each pad according to the pad matrix model for a distance ratio of 0.25 and considering a LGAD sheet resistance (R_{sheet} of 1 kΩ.

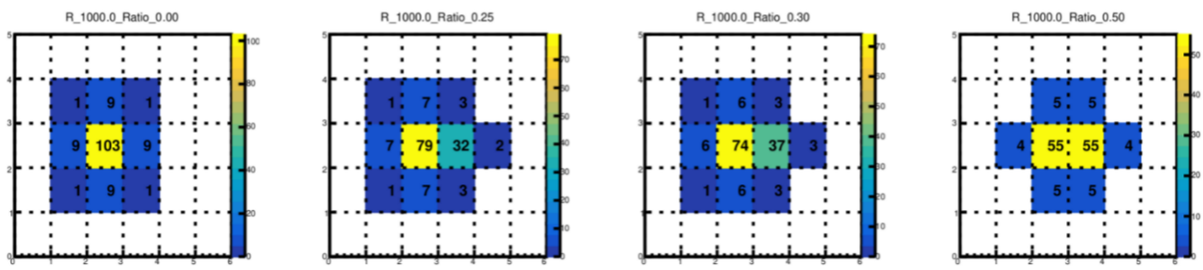

Figure 6: A 2D-representation of pre-amplifier signal amplitudes in mV obtained in each neighboring pad for a distance ratio of 0, 0.25, 0.30 and 0.50 (from left to right) considering a LGAD resistance sheet of 1 kΩ.

(left). The study consisted of comparing pre-amplifier signal amplitudes obtained at each pad after injecting a 19 fC charge at a distance ratio between pads between 0 and 1 (a ratio of 0.5 meaning that the charge is injected at equal distance between 2 pads, pads #6 and # 7). As an example, the pre-amplifier signal amplitudes corresponding to a distance ratio of 0.25 and considering a LGAD sheet resistance of 1kΩ are presented on Fig. 5 (right). In the simulation different values of LGAD resistance sheet have been taken into account: 0.1, 1, 2.5, 5 and 10 kΩ. The optimization of the sheet resistance layer is a trade-off between the best time resolution in the central pixel (requiring the largest amplitude, thus a large sheet resistance value) and the position measurement (requiring enough amplitude sharing in the neighbours, thus a small sheet resistance value). A few kΩ will satisfy both requirements.

The results of this electronics simulation have been exploited as inputs of another simulation which provides a 2D representation of the results obtained by the electronics simulation which is shown in Fig. 6 for distance ratios of 0, 0.25, 0.30 and 0.50 and a 1 kΩ AC-LGAD sheet resistance. In the context of the design of a specific ASIC prototype to readout AC-LGAD, due to the need of a threshold for precise position determination and the strongly nonlinear behaviour of the TOT, the goal of this simulation was to determine the position resolution which could be achieved relying on the barycenter method as a function of the dynamic range of the ADC to be used to measure the amplitude. This second simulation including the Landau(1,0.3)-distributed (smearing) deposition and a 1 mV gaussian noise has shown that a 8-bit ADC was sufficient to achieved a position resolution < 50 μm. On Fig. 7, one can see that 8 and 10-bit ADC are leading to an equivalent position resolution of the order of 4% (RMS) of the pixel size which corresponds to 20 μm when considering a 500 μm pixel size.

These studies have been presented at the 2022 EIC User Group Early Carreer [7] and allowed us to develop analysis tools which will be exploited in the next step consisting of the characterization of the system (EIROC0 + AC-LGAD sensor).

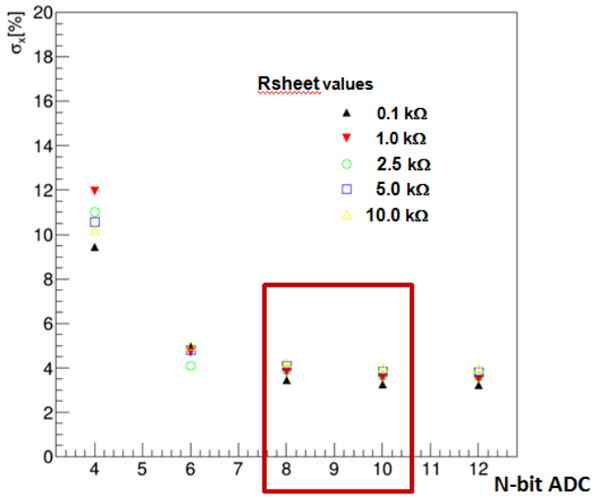

Figure 7: Position resolution in % of the pixel size as a function of the ADC dynamic range for several AC-LGAD sheet resistance.

2.1.3 EICROC0 Design

Based on the expertise in mircro-electronics of OMEGA (responsible for the design of HGCROC [8, 9] readout chip for the CMS High Granularity Calorimeter and the ATLAS ALTIROC ASIC) and from CEA/Irfu/DEPIP (responsible for the design of the TDC of HGCROC), the goal is to design a novel ASIC in 130 nm CMOS technology, EICROC, with a pitch size of 0.5 × 0.5 mm^2 that meets the requirements set by EIC providing a precise time measurement with a TDC combined with an Analog Digital Converter (ADC) for the amplitude measurement based on the simulations undertaken at OMEGA and IJClab.

For the EICROC ASIC associated to the EIC Roman Pots detector, due its location (in vacuum) and its proximity to the beam (limited space), one challenge is to reduce the power per channel to a fraction of mW, while ensuring GHz bandwidth, ultra-low noise (< 1mV) for the front–end, picosecond accuracy in the TDCs and good signal-to-noise ratio at the ADC level. Most common architectures dissipate only when the TDC is converting but the large currents drawn during conversion limit drastically the number of TDCs that can be placed on a chip and the voltage drop for large ASIC. In addition, fitting the current electronic blocks, such as the HGCROC-like TDC, in a smaller pixel area represents a second challenge while maintaining their performance. Therefore, the development of a pixel-like ASIC with a few picoseconds timing accuracy represents a technological challenge and requires several iterations that have to be characterized. Table 1 summarizes the specifications of existing ASICs developed to read silicon detectors and their time measurement capabilities as well as the EICROC0, the first EICROC iteration, that has been designed and delivered in July 2022.

	HGCROC	ALTIROC/ETROC	EICROC0
Sensor type	Si	LGAD	AC-LGAD
Pixel size [mm^2]	5 × 5	1.3 × 1.3	0.5 × 0.5
Pixel thickness [μm]	100-300	50	50
Pixel capacitance [pF]	50	4	0.5
MIP equivalent charge [fC]	4	5-20	10
Power per channel [mW]	20	5	1
TDC Least Significant Bit (LSB) [ps]	20	20	12
Threshold [fC]	12	4	2
Band width [MHz]	200	800	800
TDC (Time-Over-Threshold)		8 bits/10 bits	
ADC	10 bits@40 MHz		8 bits@40 MHz

Table 1: Comparison of specifications of existing ASICs developed to read silicon detectors and their time measurement capabilities. ALTIROC and ETROC are similar but in different technologies: 130 nm CMOS for ALTIROC and 65 nm CMOS for ETROC.

EICROC0 is a 4 × 4 pixelated prototype ASIC with a pitch size of 0.5 × 0.5 mm^2 based on ALTIROC front-end (TZ pre-amplifiers) and HGCROC ADC/TDC. Collaborators from AGH University of Science and Technology (Krakow) who designed the HGCROC 10-bit ADC provided an 8-bit version of the ADC for EICROC0. The purpose of EICROC0 is to evaluate the readout

of AC-LGAD sensors with a dedicated ASIC. The schematic and the design corresponding to one EICROC0 pixel are represented on Fig. 8 and 9. The main components in a EICROC0 channel are:

- TZ Pre-amplifiers and discriminators taken from ALTIROC,
- I2C slow control taken from HGCROC,
- TOA TDC adapted by CEA/Irfu from HGCROC to EICROC0,
- ADC taken from HGCROC adapted to 8-bits by AGH Krakow,
- digital readout: FIFO depth 8 (200 ns),
- 5 slow control bytes per pixel:
  - 6 bits local threshold,
  - 6 bits ADC pedestal,
  - 16 TDC calibration bits,
  - several on/off and probes

The TDC developed by CEA/Irfu/DEDIP and included in HGCROC has been fully characterized. It used an architecture inspired by [10], based on time residual amplification but with extended dynamic range and improved robustness against PVT (Process, Voltage, Temperature) variations. Its orientation for low power consumption is also a key point in a pixelated environment. Indeed, the power consumption of this TDC is only present during the conversion of an event. Therefore, the consumption of this part is directly proportional to the rate of events arriving on the pixels. This multichannel architecture is presented in Fig. 10. The TDC is driven by a 160 MHz clock (CLK). This clock sequences an 8-bit Gray counter which outputs are broadcasted to all the channels. When a hit occurs on a channel, the counter output is captured on an 8-bit register. To refine the measurement, a coarse TDC (CTDC) based on a 32- step Delay Line (CDL) provides 5 more bits. To extract the less significant bits, the time residue between the hit and the next step of the CDL is multiplied by 8 (optionally by 16) by a time amplifier (TA) before being coded by a fine DL (FDL) over 3 (optionally 4) bits. Then, a digital block decodes and combines the data from the counter, the CDL and the FDL to form the TDC data coded in the nominal TOA mode of operation and 10 bits are kept. In order to keep these performances stable in time and with the environment, a common block (called MASTER DLL) is used which allows to make a permanent calibration on all the TDC channels. There is therefore no dead time relative to the calibration. In addition, a fine calibration system per channel is added. Even if the common calibration is essential, a fine calibration is necessary to compensate for the mismatch effects of the channels. This calibration is currently included in the chip and is adjustable by channel. As an illustration of the performance of this TDC, Fig. 11 shows that the Integral Non Linearity (INL) is close to $\pm$ 2 LSB (Least Significant Bit) and the LSB is as low as 13 ps. Such a performance fulfills EIC requirements. This existing TDC (1 mm $\times$ 120 μm) needed to be adapted in terms of dynamic range and resolution as well as spatially optimized to fit within a pad of 500 $\times$ 500 μm^2. On the other hand, the trigger-less architecture of EIC allows some simplification of the digital part of the ASIC compared to ALTIROC, giving a larger available area for the TDC. To achieve an excellent time resolution, any coupling between the sensor input and the digital electronics activity in the ASIC or the bias voltage connection (inductance) needed to be carefully controlled, which implied constraints on the module design.

The printed circuit board (testboard) associated to EICROC0 has been designed by OMEGA, was received and cabled at IJCLab in July 2022. Main components are level translators (1.2V and 2.5V), on-board regulators for low voltage, 4 SMA connectors for pre-amplifier signal output. Space have been left near the chip location to accomodate for AC-LGAD sensor wire-bonding. Pictures of an EICROCO chip placed on the bare printed circuit board are shown on Fig. 12.

As a first step, in September 2022, an EICROC0 has been wire-bonded by BNL. PCBs holding an EICROC0 are available at BNL and IJCLab. In order to control the parameters of the system, a Xilinx ZC706 (interface board) was purchased and the dedicated firmware has been developed at IJCLab. The connection between the interface board and the test board is made through a FMC connector. A picture representing a bare printed circuit board connected to the Xilinx ZC706 is shown on Fig. 13.

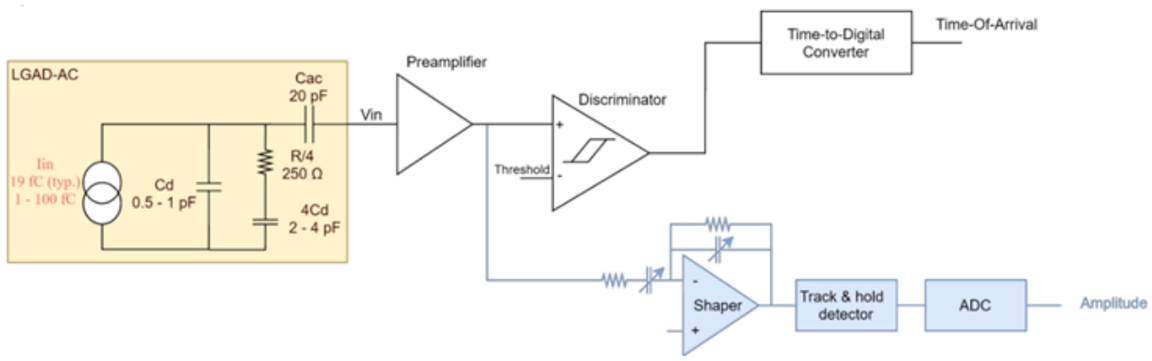

Figure 8: Schematic architecture of one channel of the EICROC0 ASIC prototype dedicated to the readout of an AC-LGAD sensor. A TDC is used to measure the time of arrival (TOA) of the charge and an 8-bit ADC measures the amplitude of the charge filtered by a shaper step.

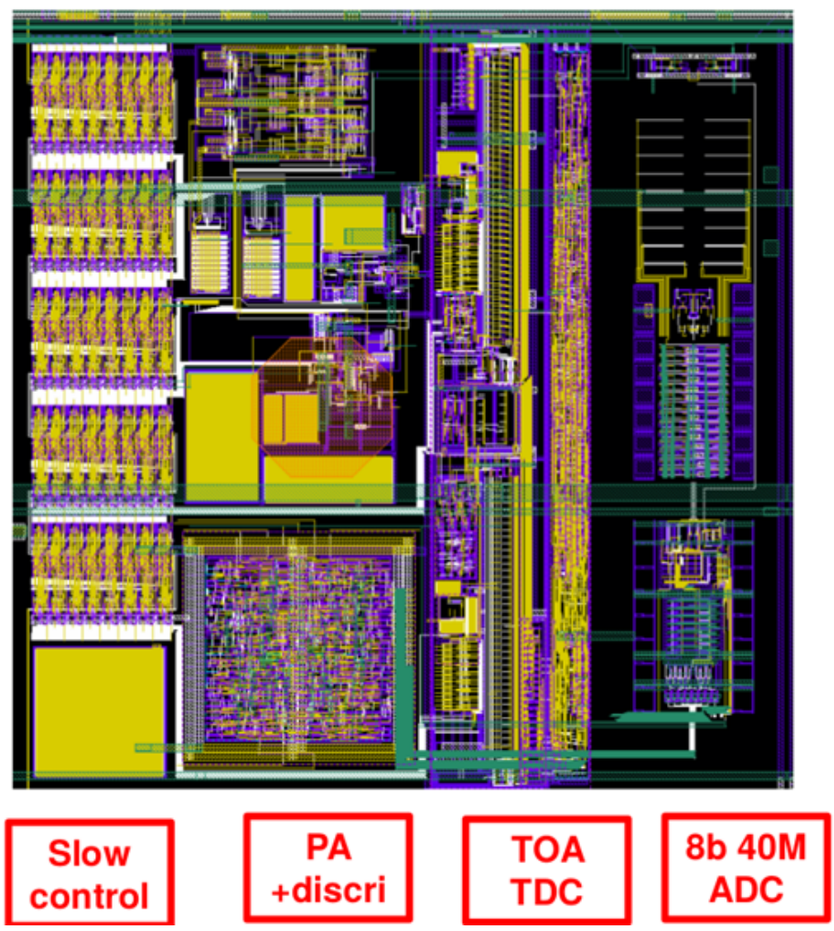

Figure 9: Design of one channel of the EICROC0 chip.

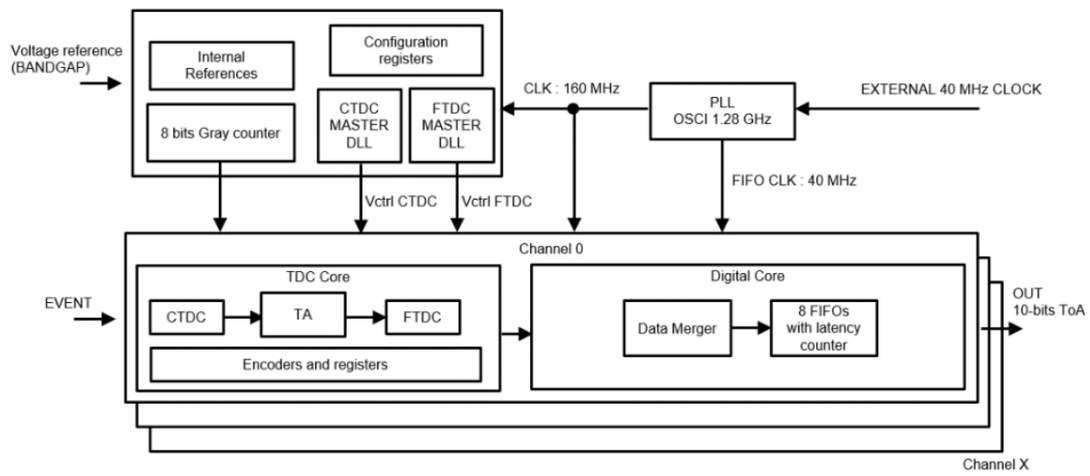

Figure 10: Block-diagram of the improved 3-steps multi-channel TDC.

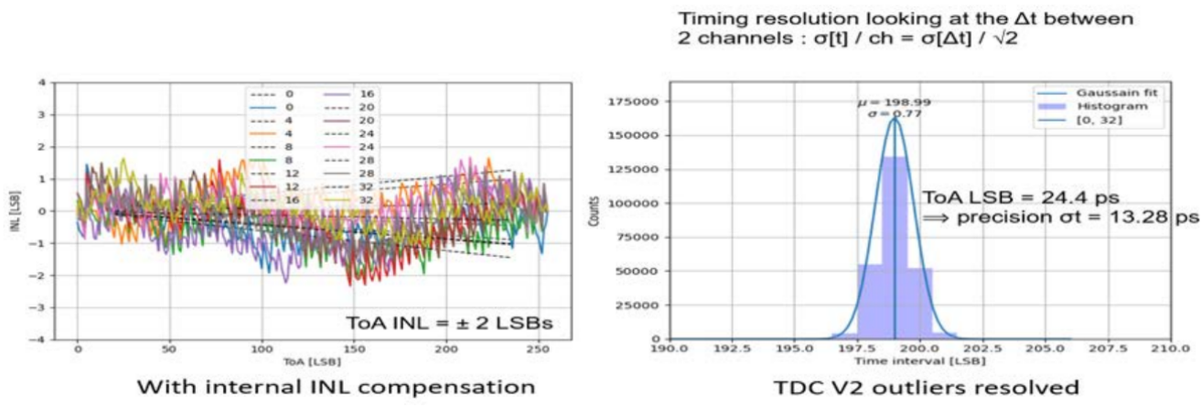

Figure 11: TOA channel INLs with internal compensation (left) and timing resolution histogram by difference between two channels (right). An individual temporal precision of 13 ps is extracted.

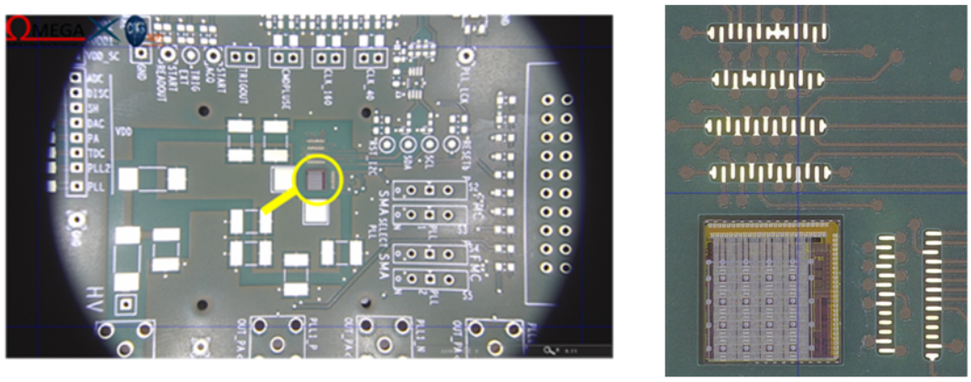

Figure 12: Pictures of an EICROC0 placed at its location on the bare printed circuit board. The picture on the right represents a zoom on EICROC0.

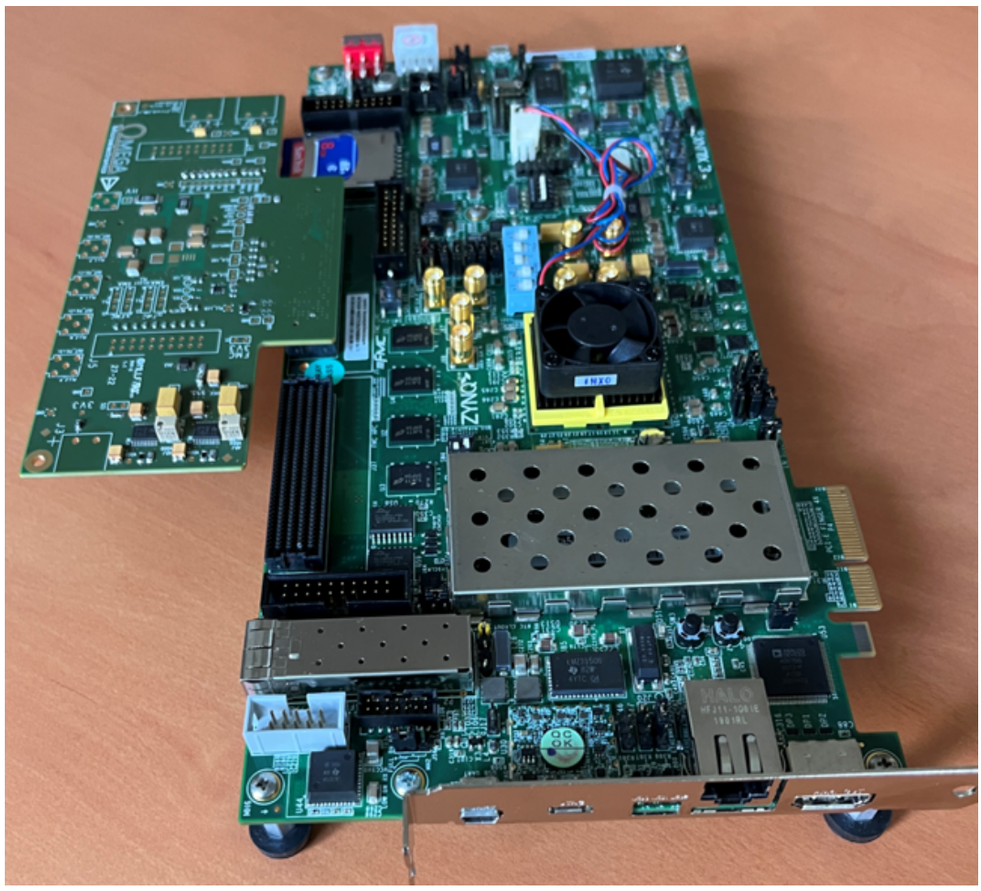

Figure 13: Picture of a bare printed circuit board connected trough FMC connector to a Xilinx ZC706.

2.2 Plans for 2023

The work planned in 2023 is organized into 2 workpackages:

- WP1: "Micro-electronics design" coordinated by Christophe de la Taille (OMEGA) involving CEA/Irfu/DEDIP, IJCLab and BNL.
- WP2: "Performance characterization" coodinated by Dominique Marchand (IJCLab) involving OMEGA, CEA/Irfu/DEDIP and BNL.

The EICROC timeline and project organization are displayed in Fig. 14.

Micro-electronics design (WP1)

WP1 is organized in 2 main tasks related to the design and the production of

- (Task 1.1) a small size 8× 4 (or 16×4 pads) ASIC prototype including a lower power ADC and adapted to EIC 100 MHz clock (**EICROC1**, Milestone 1.1, 3rd quarter of 2023),
- (Task 1.2) a full size 32×16 (or 32×32) ASIC (**EICROC2**, Milestone 1.2, mid 2025) to readout large area of AC-LGAD sensors.

The tasks associated to EICROC1 and EICROC2 are similarly organized in subtasks associated to all the stages mandatory to design, produce and test an ASIC, which include the design of each ASIC components (front-end electronics, TDC, ADC), the overall ASIC design layout and documentation, as well as the design of the dedicated electronics test benches.

OMEGA will be responsible for the overall design of the ASICs and the design of the front-end electronics (pre-amplifier and discriminator). In that context, OMEGA designers will closely collaborate with the CEA/Irfu/DEDIP team in charge of the design of the TDC and the IJClab electronics department, which is in charge of the design of the lower power ADC. The development of the test bench (specific boards for the ASIC, read-out boards and firmware) will be shared between OMEGA and IJCLab.

Task 1.1 which is the object of the FY23 budget request consists in the design, production and test of a small size prototype 8 (or 16) × 4 channels, called EICROC1, to study floorplanning.

Relying on the feedback of the measurements which will be performed with EICROC0, the goal of this prototype is to further optimize the very front-end and to include a lower power ADC and TDC fulfilling the 1 mW/channel EIC requirement.

The benefit of an ADC to measure the signal amplitude was explained in section 2.1.3. It is needed to correct for the time-walk for the timing measurement and to get a precise position with a barycenter technique.The free-running ADC adapted from a version developed by the AGH Krakow group which is implemented in EICROC0 is expected to work continuously and thus will be too much power-hungry.

The speed of 20-40 MHz and a resolution of 8 bits are not extreme, but it should be achieved with a lower power than the current state of the art (mW). In particular, the power budget should include the driving stage (shaper, buffer), which usually consumes several times more than the ADC itself. The study of a lower power ADC design has begun at IJCLab in close collaboration with OMEGA.

Task 1.1 is divided into 4 subtasks in order to explore several possible architectures for the sub blocks, probably including variants in columns to evaluate low-power front-end and digitization with a target of 1 mW power consumption per channel. The clock of 40 MHz will be also adapted to EIC (100 MHz input). Requirements serving EIC Roman Pots and ToF will be taken into account. The submission of EICROC1 design is scheduled for 3rd quarter of 2023 (Milestone 1.1).

Task 1.2 which will start in 2024 will be devoted to the design of a full size prototype of 32 × 16 (or 32) channels, EICROC2. Based on the tests of smaller arrays chips, a preferred architecture will be selected and extended to a full size matrix. At this stage, a whole column (32 pixels) needs to be implemented to investigate the power supplies and ground distributions along it and the possible voltage drops. In addition, a realistic implementation of all the digital blocks and clocks is mandatory as this is often a significant source of noise in detector systems. This task will therefore move more to digital design and integration. The tasks 1.2.1, 1.2.2 and 1.2.3 will implement corrections with respect to the corresponding tasks in 1.1 while more emphasis will be given to the task 1.2.4 regarding integration, simulation and validation steps. ASIC printed boards and interface boards will be re-designed according to the EIROC2 input/output signals in the task 1.2.5.

Characterization and performance measurements (WP2)

The ultimate goal being the demonstration that large size AC-LGAD sensors can be read by an ASIC and meet the EIC specifications, each component (sensor, ASIC) will be first characterized in a stand-alone mode to assess its intrinsic performance. In a second step, assembled devices (through wire bonding and bump bonding) will be tested to check any integration issue and finally be validated in realistic conditions with particles.

At IJCLab, in 2021 and 2022, relying on the ATLAS HGTD test-bench, characterization of ALTIROC1_v2 chip wire-bonded with a 3×3 pixelated AC-LGAD have been performed and measurements have been made using a ^{90}Sr beta source. The next stage is to expose this system to an infrared pulsed laser light (1056 nm) in order to study the charge sharing between neighboring pixels benefiting from a precise location of the light injection. This laser test-bench is inspired from the one exploited by BNL for measurements with the ALTIROC0 chip [11]. All equiments required to set-up the laser test-bench have been received. The commissioning of the test-bench is expected to start shortly and the measurements will follow. This laser test-bench will be also used for characterizing systems with each version of EICROC ASIC coupled with AC-LGAD sensors.

In parallel, since October 2022, the characterization of EICROC0 (Task 2.1) has begun with the commissioning of the EICROC0 test-bench. Then, the "channel by channel" electronics characterization of the chip wire-bonded on the PCB will be performed.

Tasks 2.1, 2.2 and 2.3 are associated to each iteration of the future EICROC, EICOC1 and EICROC2, and are subdivized in same subtasks:

Subtask #.1.1 consists in the stand-alone validation of the ASIC channels. The ASIC will be wire-bonded (or bump bonded) on a dedicated printed circuit and its characteristics, "channel by channel", will be studied using a calibration charge injection and an internal capacitance mimicking the sensor one. The main steps are the determination of the lowest threshold of the discriminator, the noise measurement and efficiency as a function of the charge. The TDC quantization steps will be measured by shifting the input calibration signal with a precise delay and the jitter extracted as a function of the charge. By injecting different charge input, the ADC quantification step and the ADC non- linearity will be extracted. The signal-over-noise at the output of the ADC is also a key measurement.

Subtask #.1.2 consists in reproducing the measurements done in subtask #.1.1 with a sensor connected at the input of the ASIC through wire bonding and bump bonding. The sensor voltage will also be supplied in order to deplete the sensor. This characterization of the system is a cornerstone step before starting to look at real energy deposits in the sensor as quite often integration issues/coupling are observed at this level and require a lot of time to be understood/solved. This subtask is a joint activity between IJCLab and BNL in close collaboration with OMEGA and CEA/Irfu/DEDIP.

Subtask #.1.3 consists finally in characterizing the module with realistic energy deposits. The module will be tested with particles, first with a radioactive beta (^{90}Sr) and it will be exposed to an IR laser light. Charge sharing and time resolution can be studied at this step. Eventually the module will be tested with hadron beam particles in a setup equipped with a precise beam telescope to fully assess the position and time resolution performance. Depending on the availability of the infrastructure, the beam test facility at FNAL (Chicago) with 120 GeV protons or at CERN-SPS with charged pions will be used. As teams from IJCLab and BNL are regular users of these beam lines for other projects, there will be no cost for testbeam.

Progress reports will be made at periodic meetings within the team and within the consortium. The resulting performances will be the object of presentations and publications (Deliverables D 2.1 and D 2.2).

2.3 FY23 EICROC budget request

The FY23 budget request presented in Table 2 relates to the submission of EICROC1 within a Multi-Project Wafer (MPW) and the purchase of associated components such as the fabrication of printed circuit boards and cabling. The labor of French institutions collaborators will be in-kind. For future developments, such as those related to EICROC2, IJCLab, OMEGA and CEA/Irfu/DEDIP team will keep seeking funds from French funding agencies but such funds are not secured.

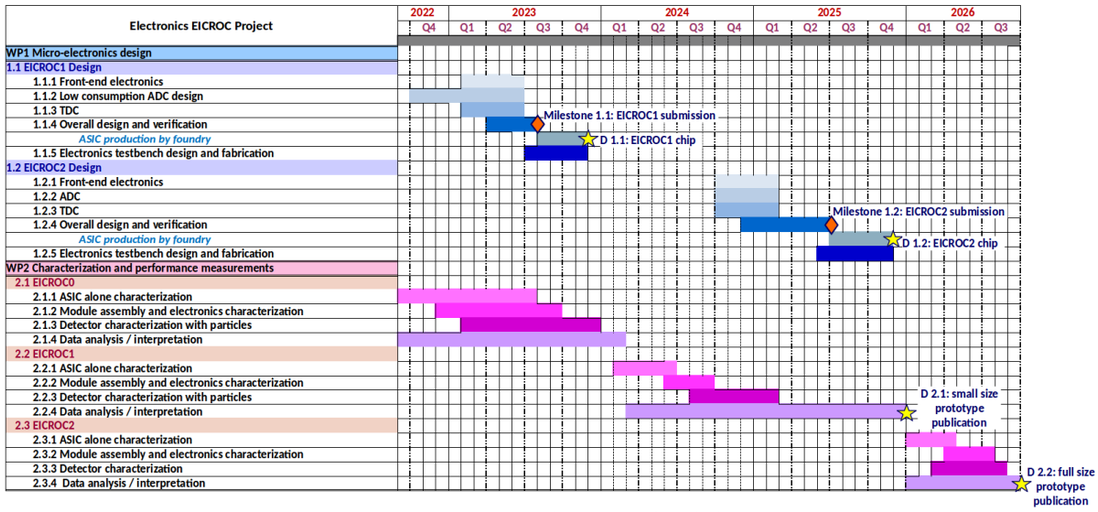

Figure 14: Timeline of the EICROC project.

Institution	Resource	Task	FTE (%)	Budget (k$)
IJCLab	Senior associate scientist	WP2	60	0 (in-kind)
	Senior scientist	WP2	35	0 (in-kind)
	Senior scientist	WP1&2	20	0 (in-kind)
	Research engineer	WP1&2	30	0 (in-kind)
	Research engineer	WP2	25	0 (in-kind)
	PhD student	WP2	50	0 (in-kind)
	EICROC1 [8 (or 16) $\times$ 4 channels] submission (MPW)	-	-	65
	Fabrication of testboards and associated components	-	-	10
OMEGA	Senior research engineer	WP1	25	0 (in-kind)
	Senior research engineer	WP1	20	0 (in-kind)
	Research engineer	WP1	15	0 (in-kind)
	Assistant engineer	WP1	20	0 (in-kind)
CEA/Irfu	Senior research engineer	WP1	30	0 (in-kind)
	Senior research engineer	WP1	10	0 (in-kind)
Total	-	-	-	**75**

Table 2: Budget request for FY23 on EICROC. All entries in thousands of dollars.

Acknowledgements

The EICROC0 project has received funding from the LabEx P2IO [6] (Université Paris-Saclay, France) for the period 2020-2022 within the call "Projets Emergents" (AC-LGAD Project).

References

[1] EIC at Brookhaven National Laboratory, Conceptual Design Report, J. Adam *et al.*, http://www.eicug.org/web/sites/default/files/EIC_CDR_Final.pdf; https://www.bnl.gov/eic/

[2] Quan Sun *et al.*, "The Analog Front-end for the LGAD Based Precision Timing Application in CMS ETL", FERMILAB-PUB-21-643-PPD, arXiv.2012.14526 [physics.ins-det], 2020, https://arxiv.org/abs/2012.14526

[3] The ATLAS Collaboration, "A High-Granularity Timing Detector for the ATLAS Phase-II Upgrade", CERN-LHCC-2020-007, ATLAS-TDR-031, CERN (2020). https://cds.cern.ch/record/2719855/files/ATLAS-TDR-031.pdf

[4] C. Agapopoulou, C. de la Taille, L. Serin *et al.*,"Performance of a Front End prototype ASIC for picosecond precision time measurements with LGAD sensors. Journal of Instrumentation, IOP Publishing, 2020, 15 (07), pp.P07007. https://dx.doi.org/10.1088/1748-0221/15/07/P07007 https://hal.archives-ouvertes.fr/hal-02497834 https://arxiv.org/pdf/2002.06089.pdf

[5] C. Agapopoulou *et al.*, "ALTIROC 1, a 25 ps time resolution ASIC for the ATLAS High Granularity Timing Detector", 2020 IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2020, pp. 1-4, https://ieeexplore.ieee.org/document/9507972

[6] http://www.p2io-labex.fr

[7] P.-K. Wang, "Simulation and instrumentation for the Roman Pot in the future Electron-Ion Collider", EIC User Group Early Career Workshop 2022, July 24-25, CFNS Stony Brook University. https://indico.jlab.org/event/485/contributions/10232/

[8] CMS Collaboration. Technical Proposal for a MIP Timing Detector in the CMS Experiment Phase 2 Upgrade. (2017). CERN-LHCC-2017-027 ; LHCC-P-009
https://cds.cern.ch/record/2296612/files/LHCC-P-009.pdf

[9] D. Thienpont and C. de la Taille for the CMS Collaboration, "Performance study of HGCROC-v2: the front- end electronics for the CMS High Granularity Calorimeter", JINST15 (2020) C04055, 3rd Conference on Calorimetry for the High Energy Frontier, Fukuoka, Japan, 25 - 29 Nov 2019, CMS-CR-2020-014.
https://cds.cern.ch/record/2712269/files/CR2020_014.pdf

[10] K. Kim, Y. Kim, W. Yu and S. Cho, "A 7 bit, 3.75 ps Resolution Two-Step Time-to-Digital Converter in 65 nm CMOS Using Pulse-Train Time Amplifier" in IEEE Journal of Solid-State Circuits, vol. 48, no. 4, pp. 1009-1017, April 2013, doi: 10.1109/JSSC.2013.2237996.
https://uma.ac.ir/files/site1/g_zare_3fd00a8/tdc2.pdf

[11] G. D'Amen *et al.*, "Signal formation and sharing in AC-LGADs using the ALTIROC0 front-end chip", Sept. 2022, arXiv:2209.07329 [physics.ins-det], https://doi.org/10.48550/arXiv.2209.07329