UNIVERSITY OF BIRMINGHAM

BILPA Birmingham Instrumentation Laboratory for Particle physics and Applications

ePIC

EIC-UK WP1 Face-to-face Meeting

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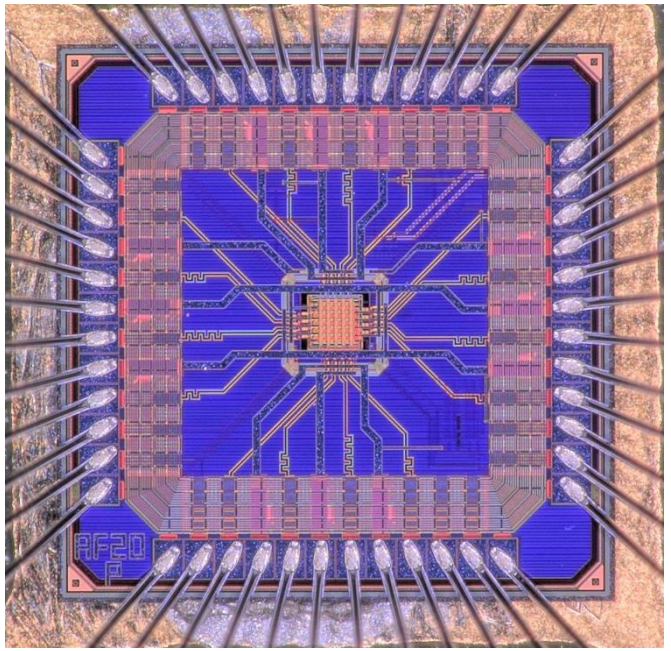
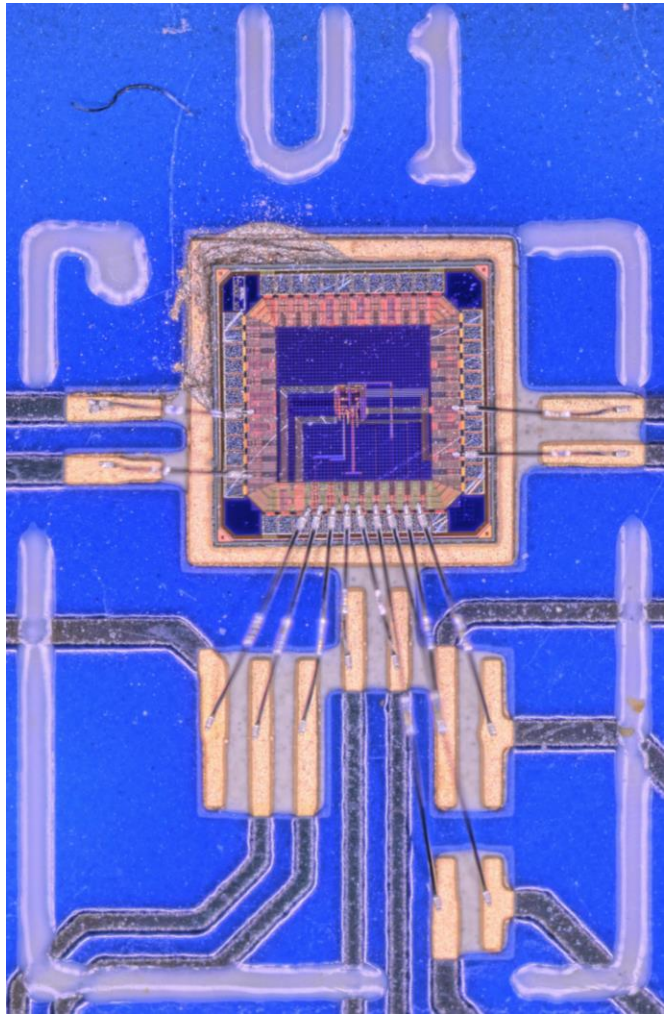
Wednesday, 28th June 2023

Recap: The last F2F

- MLR1 APTS-SF DAQ system obtained & commissioned. – link (old EIC-UK WP1 indico area, not public)
- MLR1 LVDS/CML test structures obtained, DAQ system commissioned (via Xilinx's Vivado suite). – link (old EIC-UK WP1 indico area, not public)
- Mounting and wire bonding procedures set up for both the above structures.





Since the last F2F

- Birmingham has been 1 of 4 APTS-SF chip mounting/bonding sites (others being CERN, Strasbourg & Liverpool).
- Characterising chips prior to mounting (resistance measurements, probed chips in GelPak).
  - Minimises chip failures post-bonding.
- Non-conductive chip mounting options (to reduce radiation length of test structures) have been explored in collaboration with CERN colleagues.

- Test site for APTS-SF split 2 & 3 devices.
  - Pulsing tests performed at B'ham, majority of Fe-55 testing performed at L'pool.
- Contributed split 1, 2, 3 & 4 comparison plots to the pool of plots approved for publication by ITS3.

- Options for serial powering scheme for the EIC-LAS.

- Detector layout simulations.

Characterisations of APTS - 1

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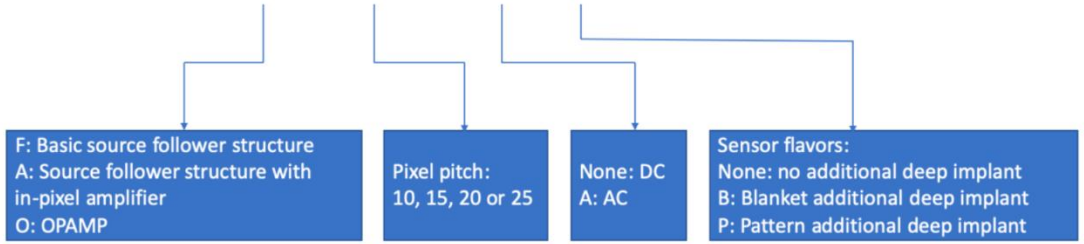
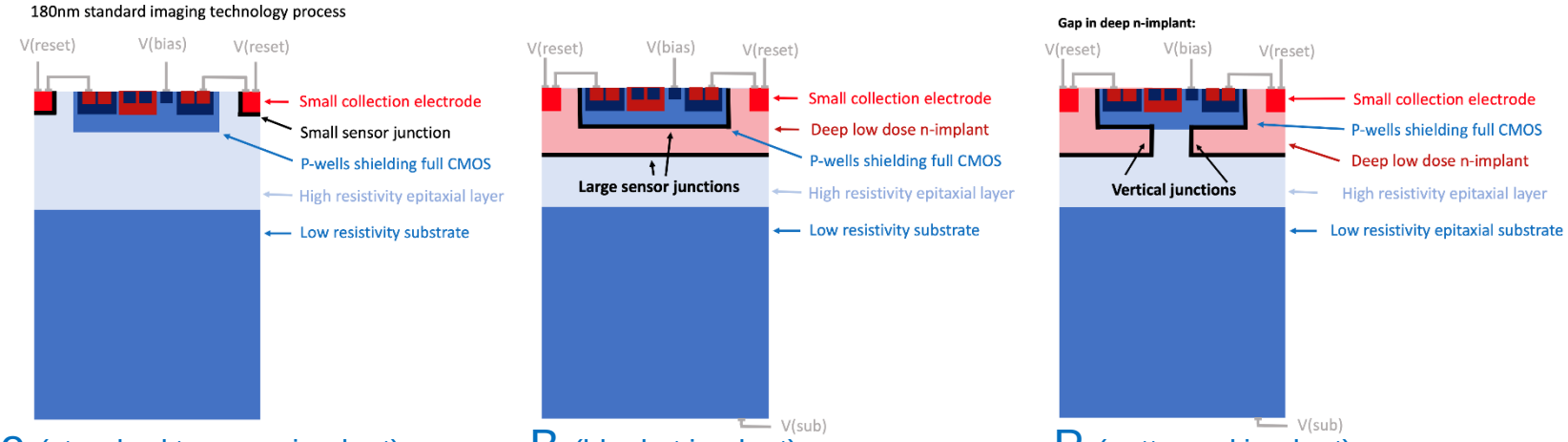


MAPS constructed in 65nm CMOS technology.

- 3 APTS structures: F (source follower), A (in-pixel amp) & O (OpAmp).
- 4 pixel pitches (in 4×4 pixel array).
- Both DC and AC coupled versions.
- 3 “flavors” of deep implant: None, B & P.
- Additionally, there have been 4 different wafers (“splits”) with small variations to the doping of the P-well and N-implant.

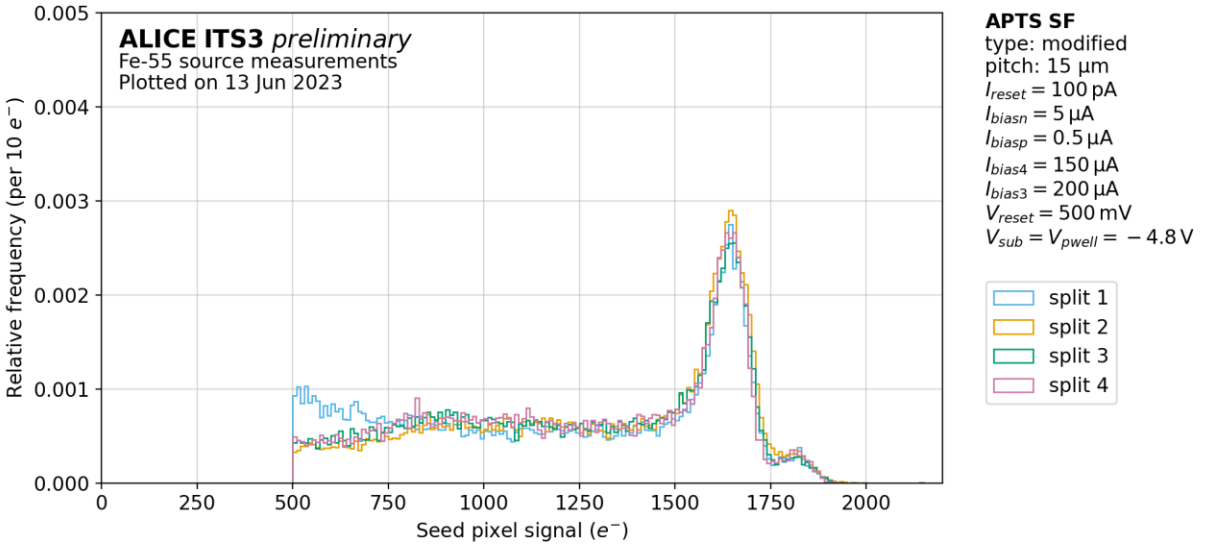
APTS flavours:



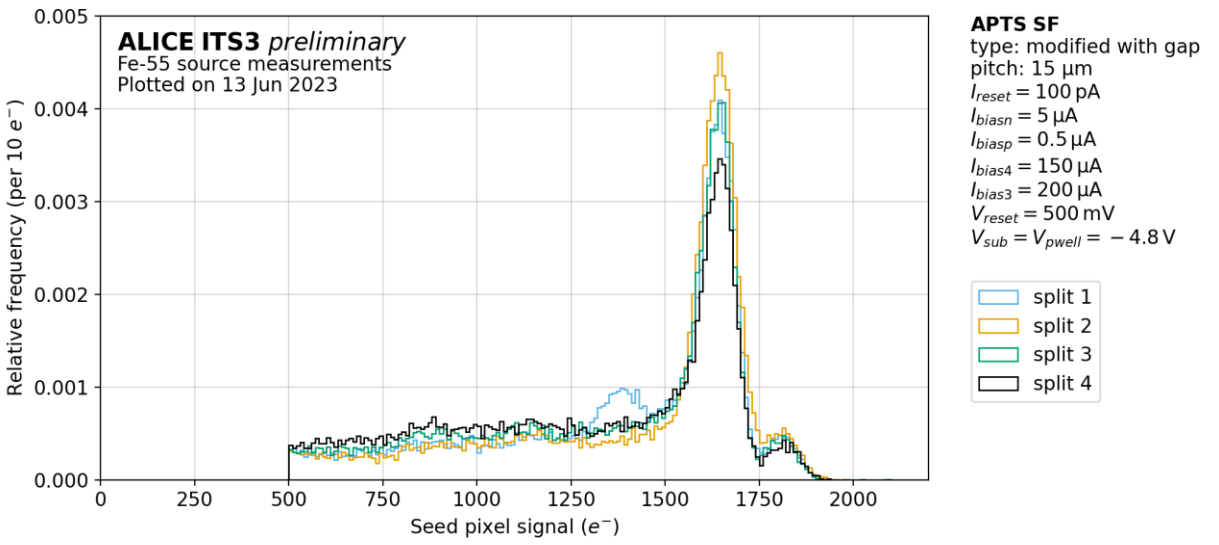
None (standard type, no implant) B (blanket implant) P (patterned implant)

Characterisations of APTS - 2

- Birmingham has investigated pitch, flavour and split variations of DC-coupled, source follower structures.
- Plots approved for publication during ITS3 June ‘23 approval session.



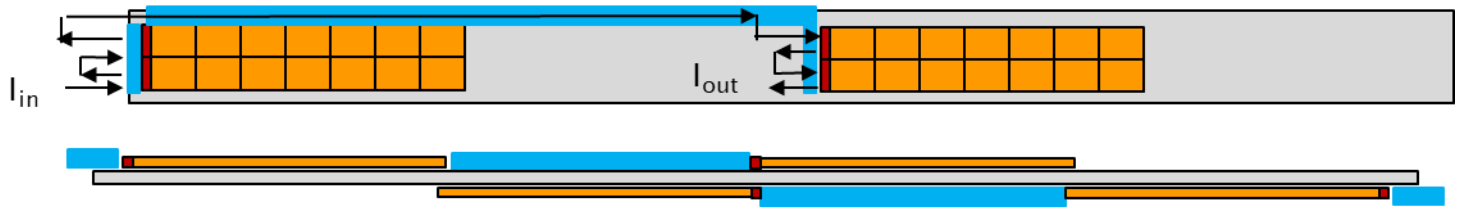
AF15B (split comparison)



AF15P (split comparison)

Serial powering

- Serial powering scheme chosen as baseline for the ePIC SVT
  - Provides lowest material option
- Shunt-LDO placement on a dedicated powering chip outside the sensor
  - Allows re-using of ITS3 sensor on-chip power distribution; Does not require modification of sensor periphery; Can be prototyped and fabricated in cheaper technology
- Serial powering scheme drafted for sagitta layers
  - Current flowing between sensor segments on each side of the stave
  - Factor 4 current reduction for L4, factor 2 current reduction for L3

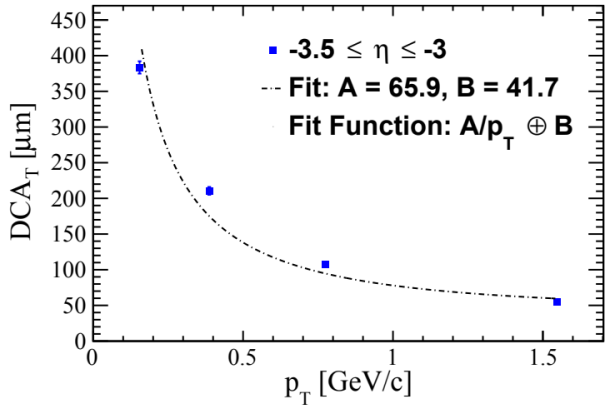


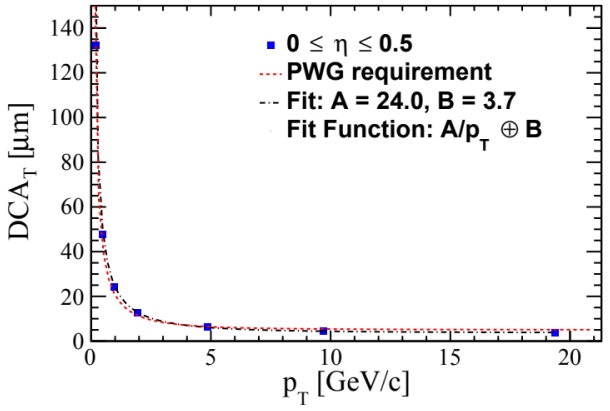
L4 serial powering scheme;
top – stave top view, bottom – stave side view

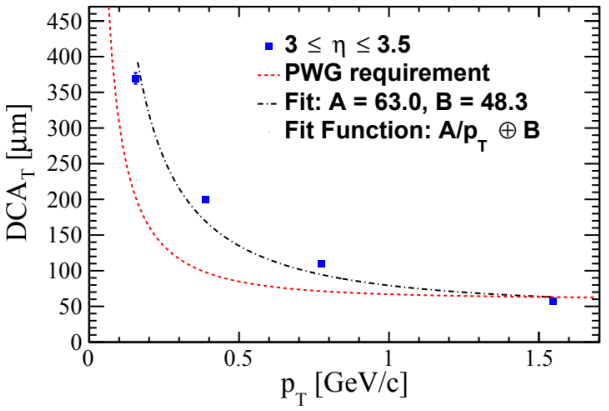
- Number of sensor low voltage and bias cables estimated and provided to EIC project engineers for integration exercise

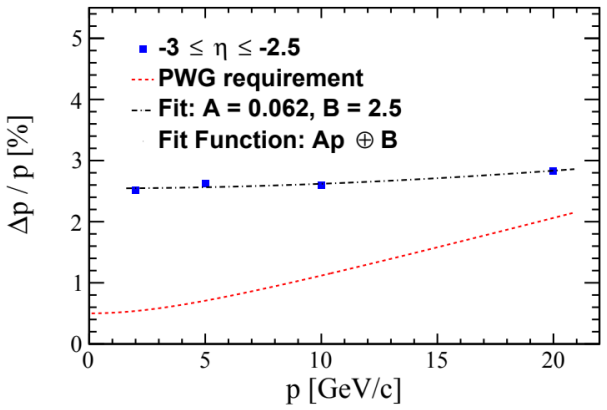
Detector layout simulations - 1

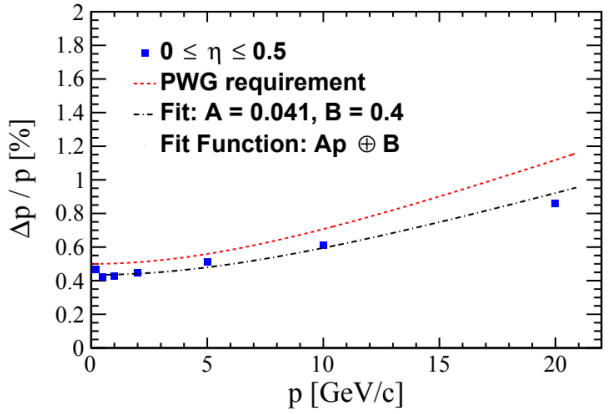
- Parametrised momentum and vertex resolutions with ePIC tracker configuration*.

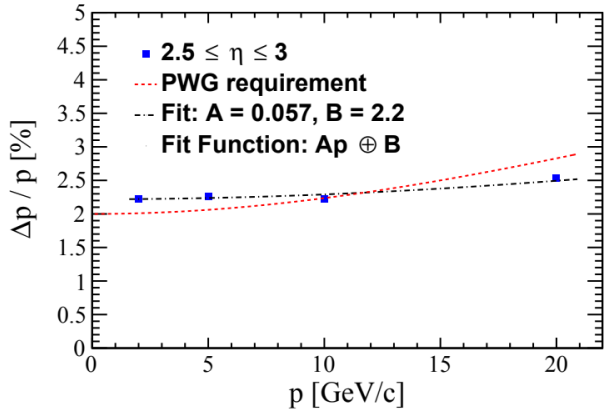








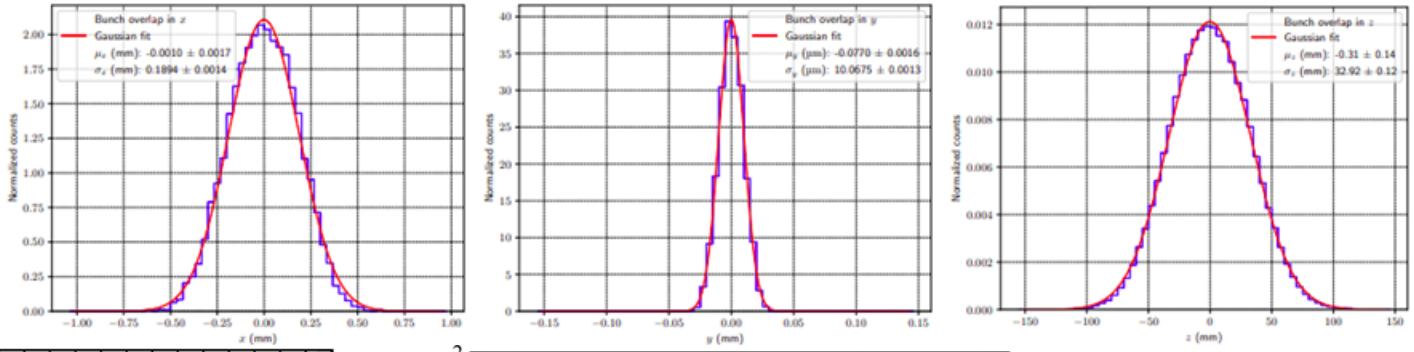


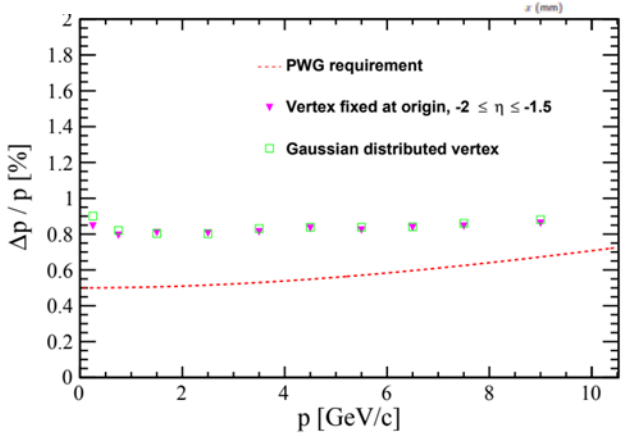


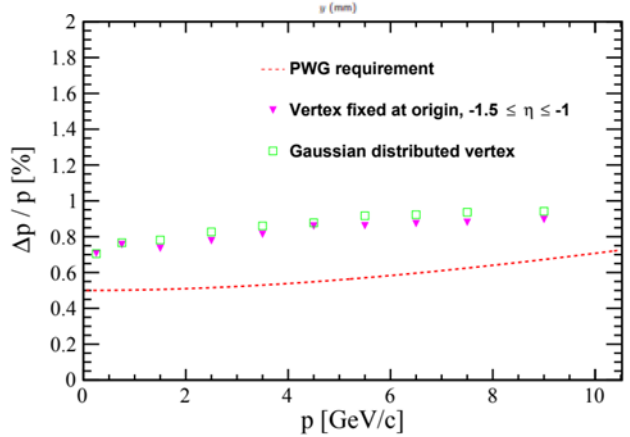
*Brycecanyon 22.11.2 (juggler)

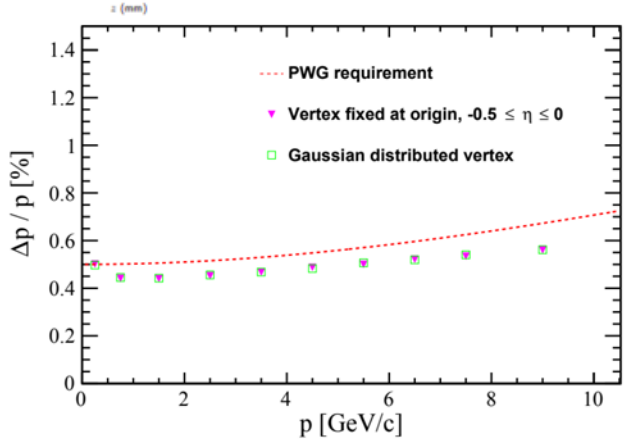
Detector layout simulations - 2

- Study of beam spot effect on the tracking performance .
  - Minimal degradation of momentum resolution in specific pseudorapidity intervals where particles traverse support material; no effect on the vertex resolution.





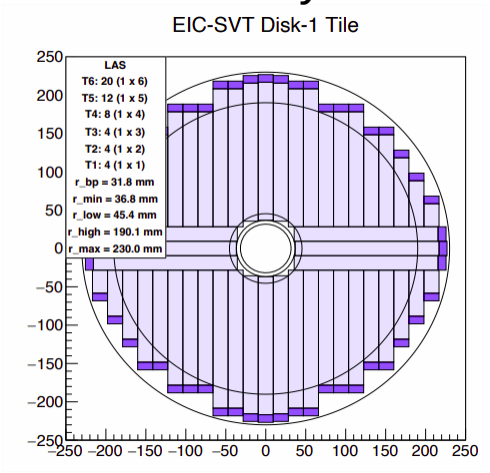




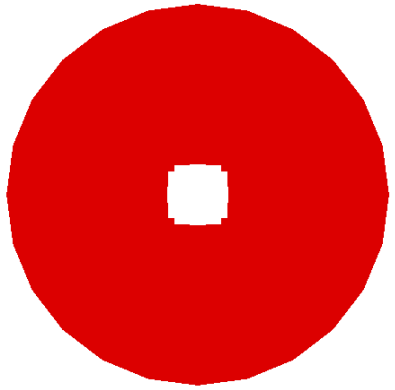
Detector layout simulations - 3

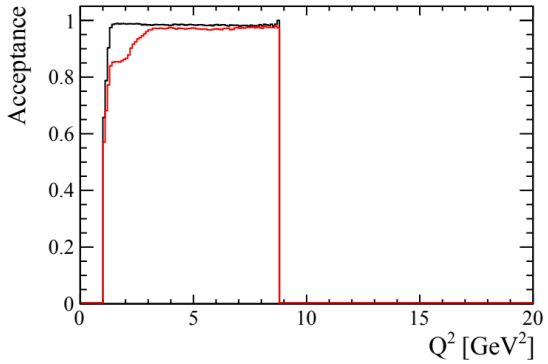
- Study of acceptance at large eta.
- Realistic disk design implemented in simulation.
- Higher x lower Q^2 bins lose acceptance.
- Acceptance > ~80% for all bins Q^2 > 1GeV^2 for 100% efficient disks.

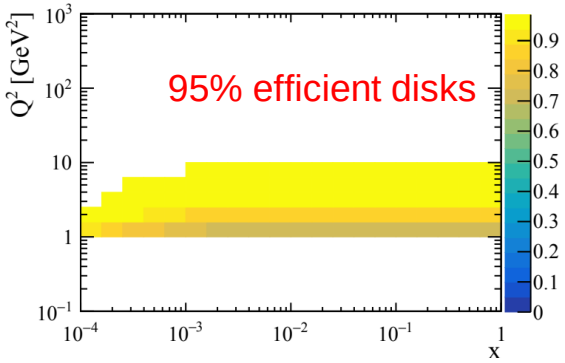
Example of disk configuration in tiling study

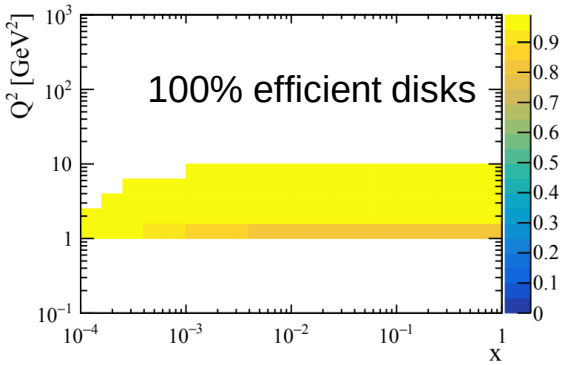


Disk implementation in simulation



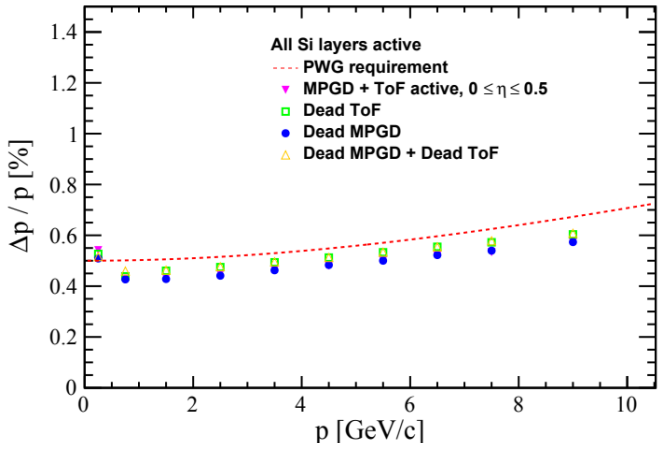


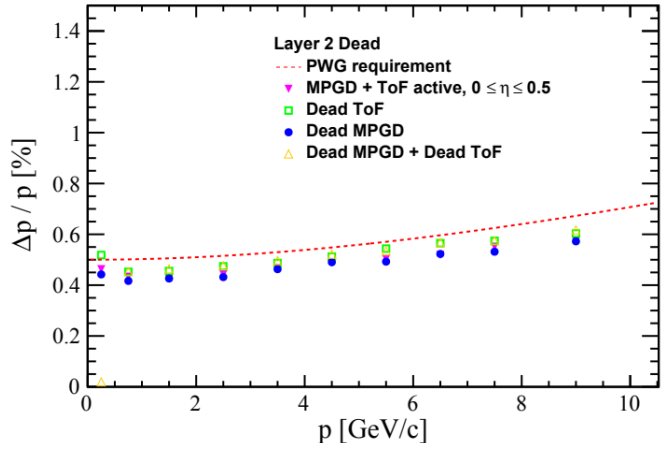


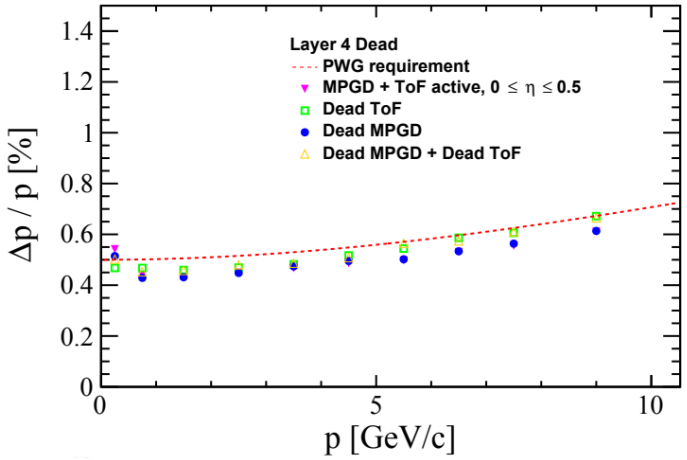


Detector layout simulations - 4

- Study of barrel MPGD layer contribution to tracking.
  - Different combinations of active silicon, MPGD and Time of Flight (TOF) layers.
  - Momentum and vertex resolution fully defined by SVT, with small improvement by TOF layer; no recovery in performance with the MPGD layer active in case of failure of one silicon layer; barrel MPGD layer contribution in pattern recognition only.







Going forward – short term plan

- Continue with MLR1 APTS-SF comparisons.
  - Look at leakage current comparisons (already started).
- Await ER1 chips.
  - Offer to help with chip mounting/wire-bonding again.
  - Commission ER1 DAQ set-up.
- Await ER1 RAL LVDS/CML test structures.
  - Again, happy to help mounting, bonding and testing.
    - Is KCU105 still to be used as the PRBS generator?
- Continue with conceptualisation of serial powering scheme.
  - Focus on Outer Barrel Layers (UK focus) but will also consider options for the disks.
  - Added complexity with the ER2 design confirmation of power required on both left and right endcaps.
- Detector layout simulations to continue/develop.

Going forward – final R&D and construction

Areas where B'ham wants to contribute:

- Sensor characterisation:
  - ITS3 ER2 and ER3
  - EIC LAS v1 and v2
  - Production testing QC/QA (incl. wafer probing)
- Modules (an assembly of sensors on an FPC):
  - Prototypes: assembly & testing
  - Pre-Production: assembly & testing
  - Production: assembly & testing (QC/QA)
- Tooling:
  - Module assembly tooling: prototypes, pre-prod, prod
- Powering (SP = Serial Powering):
  - Regulator characterisation
  - Data and grounding schemes development
  - Current source development and testing
  - Prototypes SP chain testing
  - Pre-production SP chain testing
  - Production SP chain validation
- DAQ (SW/FW/HW needed for testing of various objects) – in connection to SP:
  - Electrical staves: prototype testing
  - Electrical staves: pre-production testing
  - Electrical staves: production testing
  - L3 and L4 testing (after integration)

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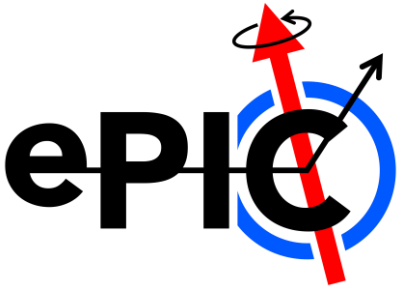

Additional slides