Technical overview of the ePIC SVT

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ePIC SVT DSC kickoff meeting

9 June 2023

Outlook – Part 1

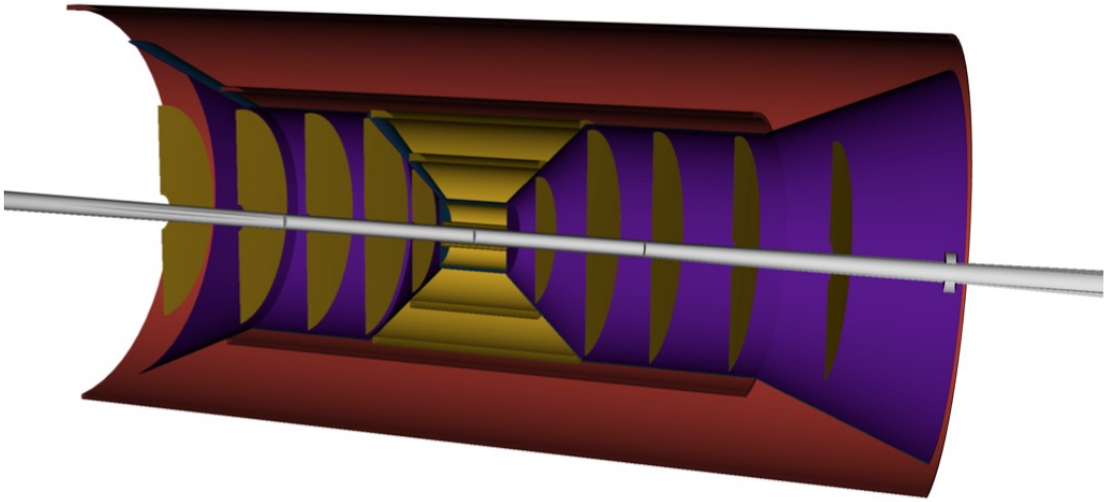
ePIC SVT layout & concept

ePIC SVT layout

- The current ePIC SVT layout (October 2022 geometry) comprises
  - 3 Inner Barrel (IB) layers (curved silicon layers)
  - 2 Outer Barrel (OB) layers (stave-based layers)
  - 5 disks on each side of the interaction point

- Total (active) area ~ 8.5 m^2

October 2022 geometry



Updated barrel reference geometry:
- 2 curved silicon vertex layers, r = 36, 48 mm, l = 270mm
- 1 curved silicon dual purpose layer r = 120mm, l = 270mm
- 1 stave-based sagita layer r = 270 mm, l = 540 mm
- 1 stave-based outer layer r = 420 mm, l = 840 mm

Updated disk reference geometry:
- 5 disks on either side of the nominal IP,
  - z = -250, -450, -650, -900, -1150 mm
  - z = 250, 450, 700, 1000, 1350 mm
  - inner radii >= 36 mm, outer radii <= 430 mm

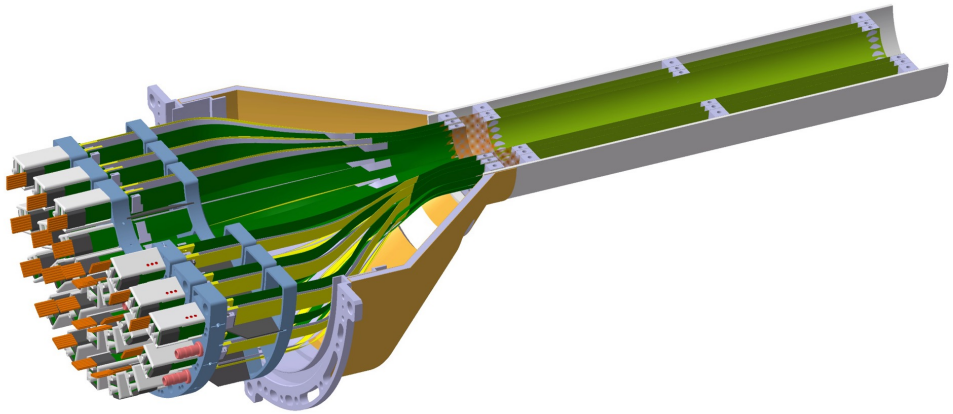
ePIC SVT concept in a nutshell

- ITS3-like Inner Barrel layers
  - Use the ITS3 wafer-scale sensor
  - Adapt ITS3 detector concept to the (larger) EIC radii
    - Mechanics, services and cooling of ePIC SVT inner barrel layers need specific development

- Outer Barrel layers and disks
  - EIC Large Area Sensor (LAS), i.e. ITS3 sensor size optimised for high yield, low cost, large area coverage
  - Conventional design of carbon fibre support structures (i.e. staves, disks), with integrated cooling and electrical interfaces

ITS3

- Vertex detector made of 3 truly cylindrical layers
  - Radii 18/24/30 mm, length 270 mm
- Half layers made of wafer-scale, single-die Monolithic Active Pixel Sensors (MAPS)
  - Thinned to <50 μm and bent around the beam pipe
- Position resolution ~5 μm

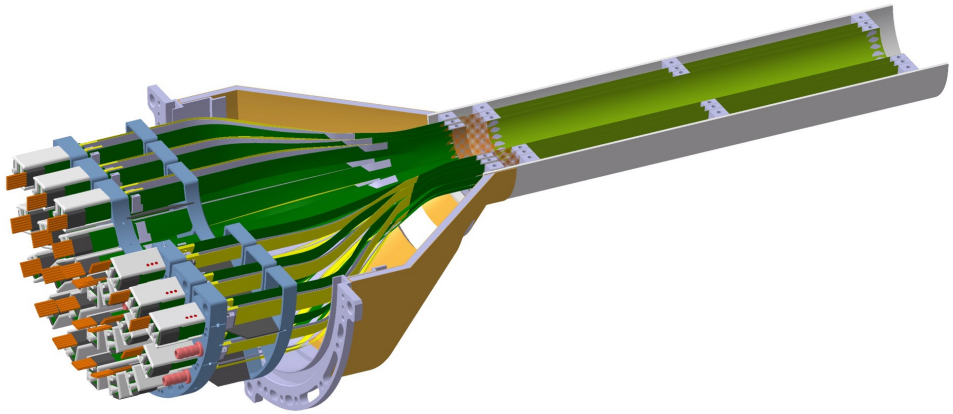


Pb-Pb Interaction Rate	50 kHz
Particle Flux	2.2 MHz/cm^2
Integration time	< 10 μs
TID	<10 kGy
NIEL	1×10^{13} 1 MeV n_{eq} cm^{-2}

ATLAS ITS3 LOI https://cds.cern.ch/record/2703140/
https://indico.cern.ch/event/1280150/

ITS3

- Minimised material budget, 0.05% X/X0 per layer
- No flexible circuits in the active area
  - Services connected to the short edge of the sensor
- Cooling by air flow
  - <20 mW/cm^2 in sensitive area
- Minimal support structure
  - Benefit from increased stiffness by rolling Si wafers



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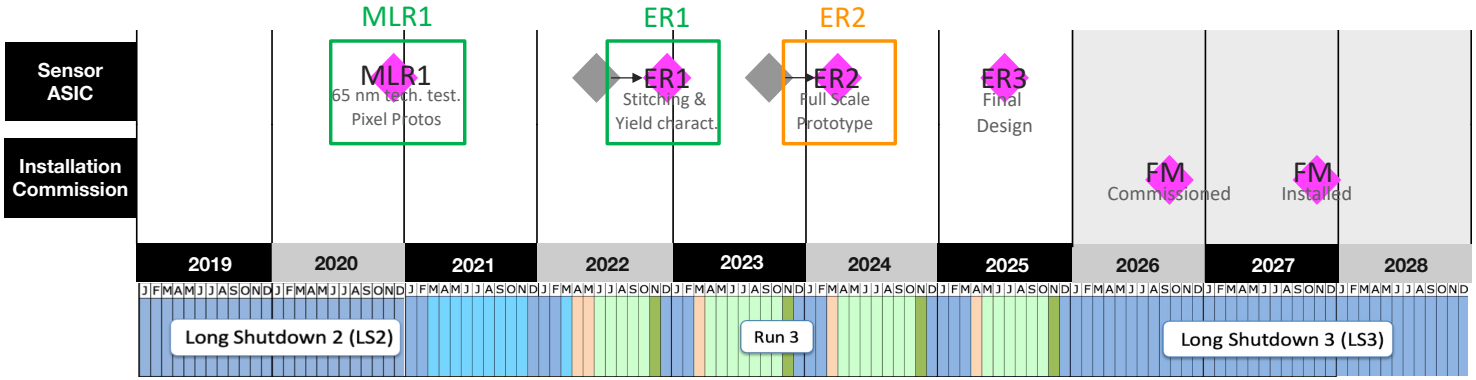
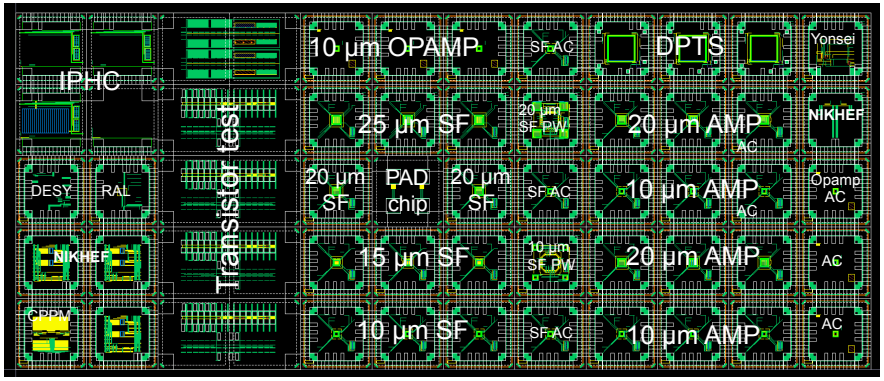
ITS3 sensor development

- TPSCo ISC 65 nm CMOS Imaging technology, 300 mm wafers + stitching



- MLR1 (Q4 2020)
  - Technology exploration and prototype circuit blocks for future sensors
  - Large number of test structures; including Analogue and Digital Pixel Test Structures (APTS, DPTS)



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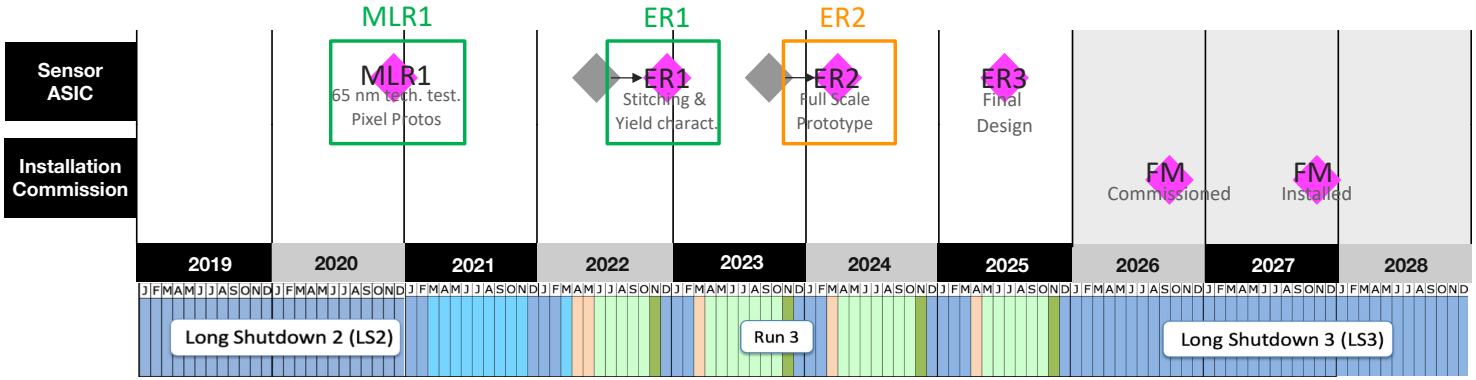
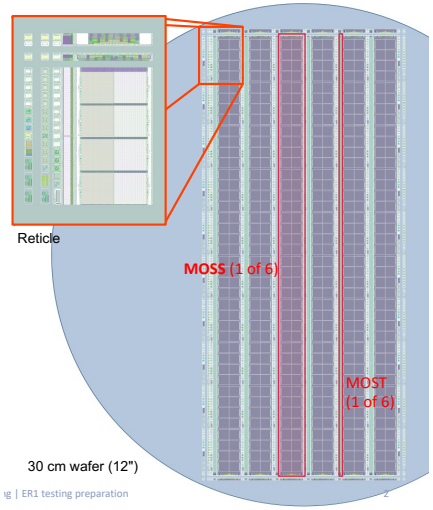
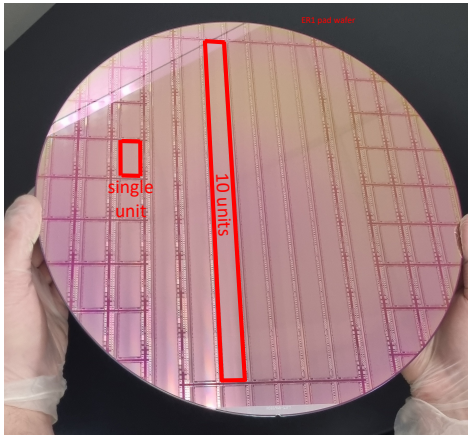


- ER1(Q4 2022)
  - MOSS and MOST sensors; exploratory designs for proof of principles and learning methodology and yield
  - Also, small prototypes and test chips
  - First, single unit MOSS can be powered and responds correctly to slow control commands





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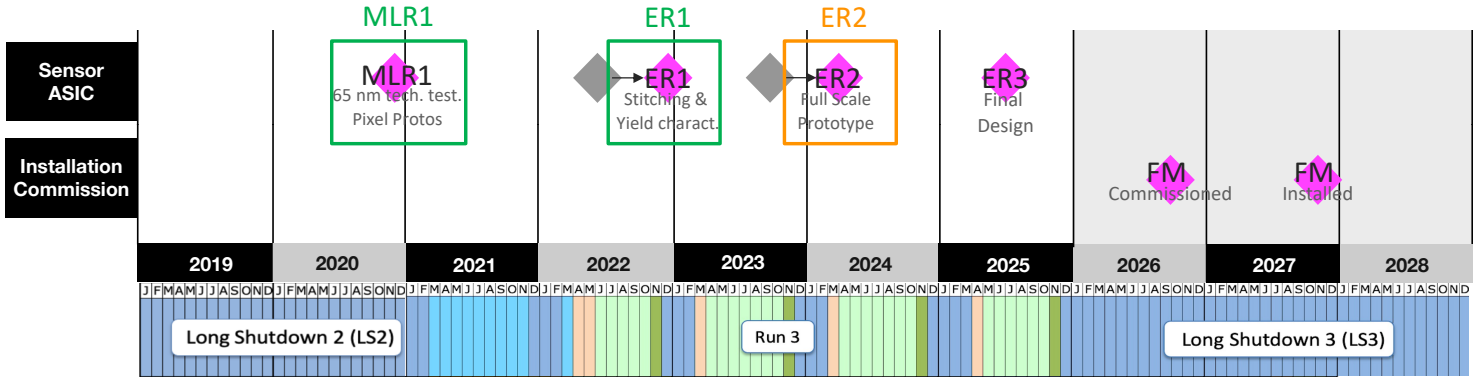

- ER2 (Q1 2024)
  - Sensor aims to satisfy ITS3 requirements
  - Not an evolution of MOSS/MOST; substantial redesign of existing circuits, new features

- ER3 (Q2 2025)
  - Final design/production

The EIC LAS sensor will be based off the ER2 and ER3 designs

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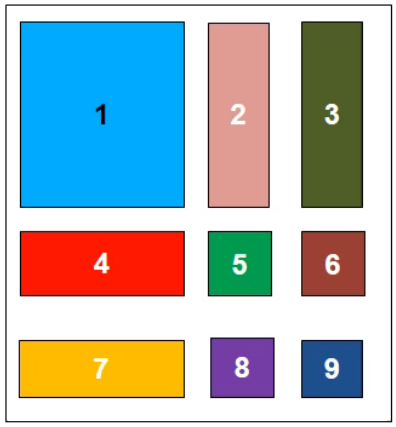
Stitching

- Stitching is an integrated circuit technology specifically designed to cover the large areas needed for image sensors

- In normal integrated circuit fabrication light is shone through masks with a size of ~3x3cm (reticle) to pattern circuits on a wafer

- In a stitching technology, the mask is sub-divided, and different sections are repeatedly exposed across the wafer to make devices that are larger than the mask (see video)

Courtesy of Iain Sedgwick (RAL)

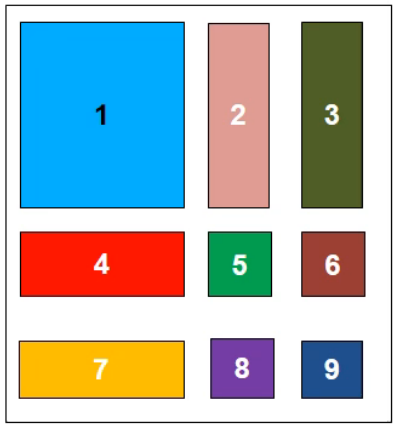


Stitching

- This has the advantage that a large area can be covered
  - Also (dependent on specific foundry rules) different sized sensors can be created by changing the number of repetitions without a new mask set

- The plan for the how different blocks are repeated is referred to as the stitching plan

Courtesy of Iain Sedgwick (RAL)



ITS3 ER2

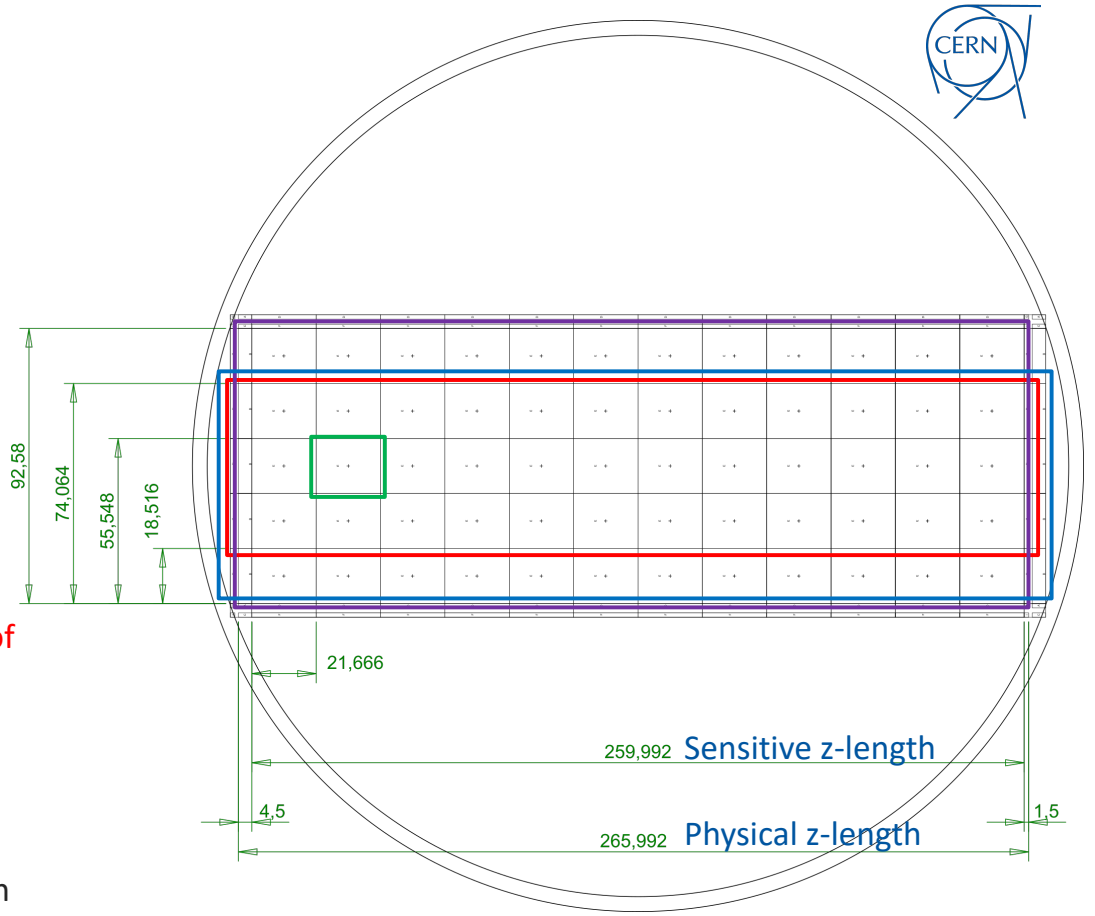
ER2 Stitched Sensor

Layer 0: 12 x 3 repeated units+endcaps

Layer 1: 12 x 4 repeated units+endcaps

Layer 2: 12 x 5 repeated units+endcaps

Repeated (Stitched) Sensing Unit



ER2 Stitched Sensor is **not** a direct evolution of MOSS +/- MOST

- MOSS and MOST were true exploratory designs for proof of principles and learning methodology and yield

ER2 Sensor aims to satisfy ITS3 requirements

- Existing circuits need substantial redesign
- New features to be added

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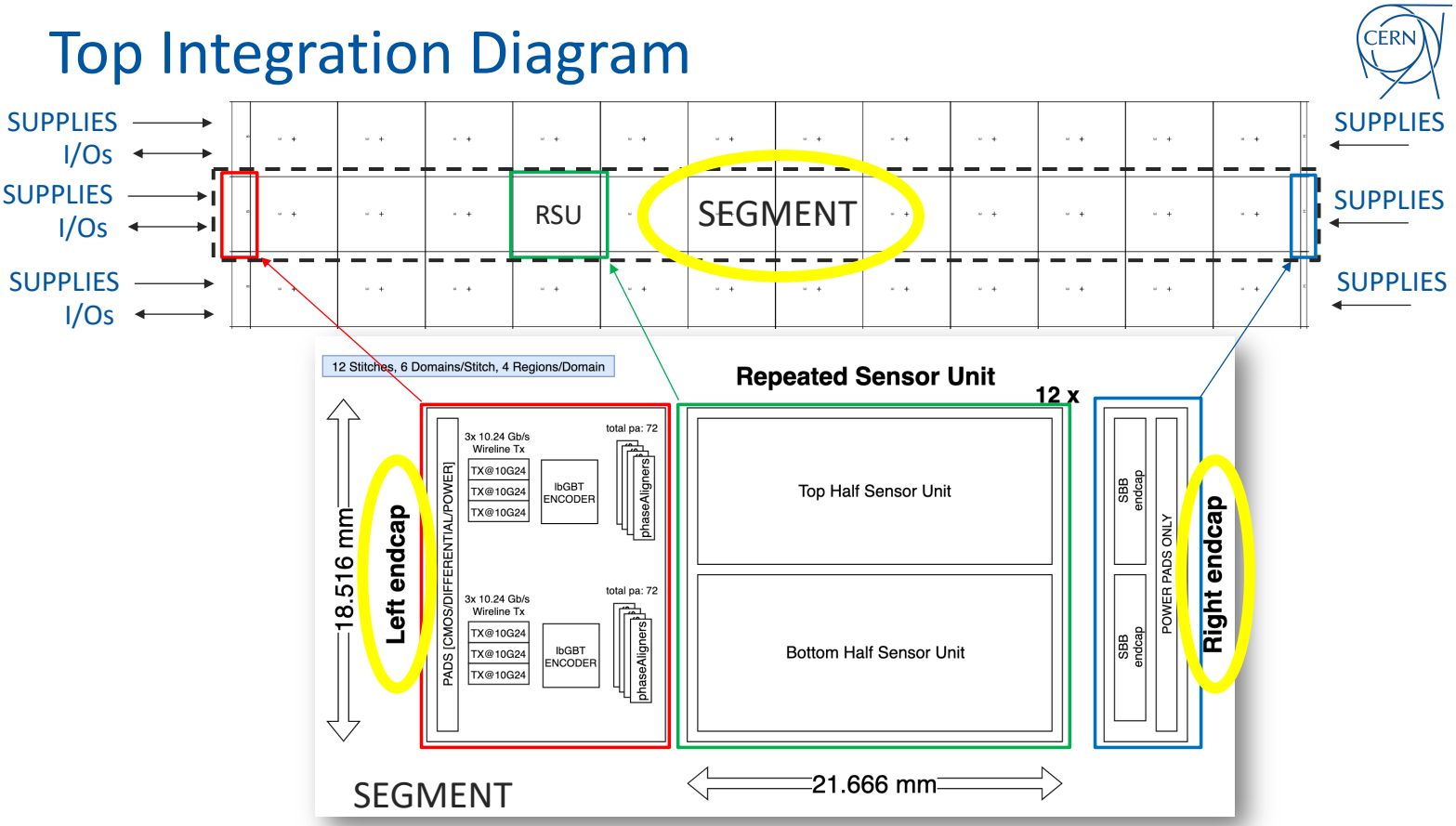
ITS3 ER2

Top Integration Diagram



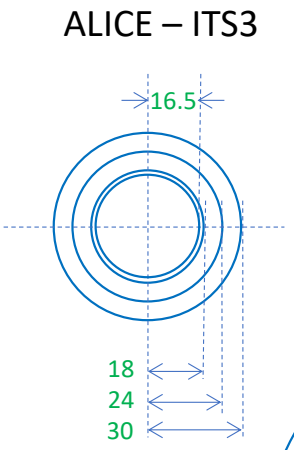
ITS3 L0/1/2 wafer-scale sensor made of 3/4/5 segments

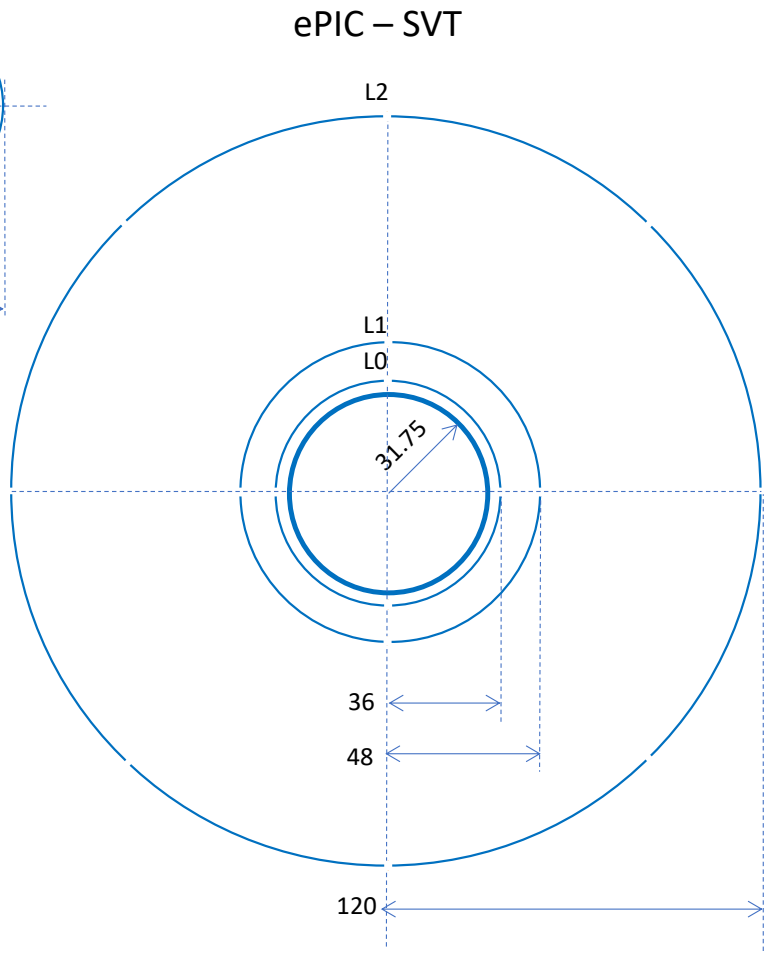
https://indico.cern.ch/event/1280150/

ePIC SVT Inner Barrel (IB) layers

- Re-use ITS3 wafer-scale sensor
  - L0: 3x12 RSU + endcaps
  - L1: 4x12 RSU + endcaps
  - L2: 5x12 RSU + endcaps

- Number of sensors per layer
  - L0: 4
  - L1: 4
  - L2: 8





ePIC SVT IB	r [mm]	l [mm]	X/X0 %
L0	36	270	0.05
L1	48	270	0.05
L2	120	270	0.05

ePIC SVT Outer Barrel (OB) layers and disks

- EIC-LAS sensor = 1 segment with N RSU + endcaps.
- N to be defined based on yield and cost, acceptance and coverage, manufacturing constrains.
- Possibly add some changes in the endcaps.
  - e.g. if needed for powering and data transmission.

ePIC SVT OB	r [mm]	l [mm]	X/X0 %
L3	270	540	0.25
L4	420	840	0.55

Disks nomenclature:
ED0 – ED4 in electron going direction (-z)
HD0 – HD4 in proton going direction (+z)

Disk inner opening:
beam pipe radius + clearance for beam pipe bake out (5 mm);
offset wrt disk center where beam pipe fans out

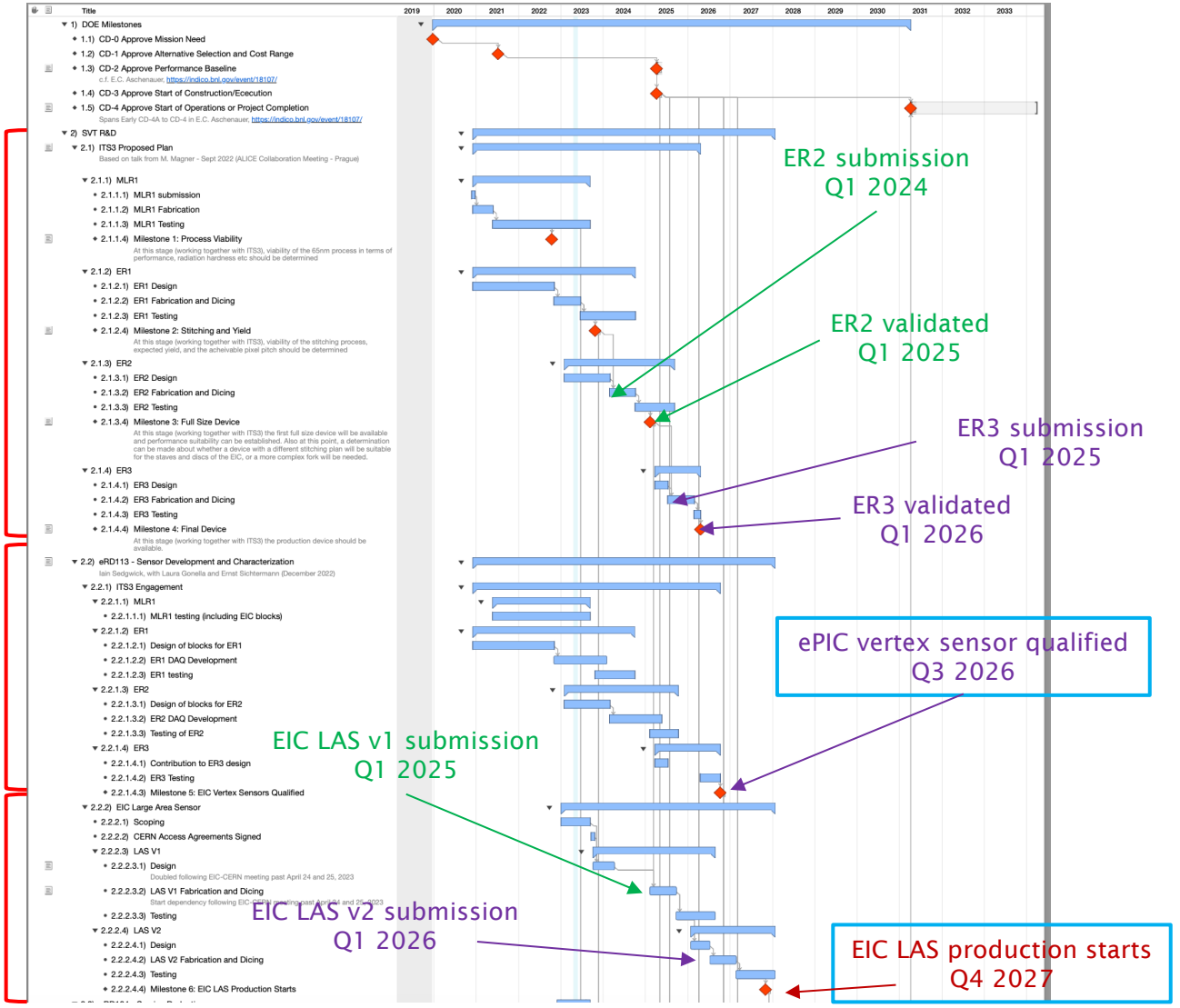
ePIC SVT Disks	+z [mm]	-z [mm]	r_out [mm]	X/X0 %
Disk 0	250	-250	240	0.24
Disk 1	450	-450	420	0.24
Disk 2	700	-650	420	0.24
Disk 3	1000	-900	420	0.24
Disk 4	1350	-1150	420	0.24

Schedule of ePIC sensor development

ITS3 schedule

EIC contribution to ITS3 submissions

EIC LAS design



Outlook – Part 2

Overview of ePIC SVT development technical aspects

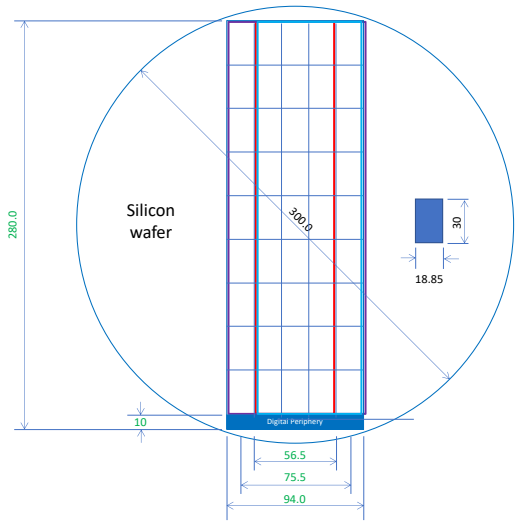
Foreword

- Progress on the development of the ePIC SVT up to now was based on a number of assumptions on the sensor design
- The significant progress on the ER2 design in the past few months has provided information on the sensor design that have an impact on the ePIC SVT development
- Many aspect of the SVT development will need to be updated or revised
- The remainder of the talk will discuss details of the sensor design and impact on the ePIC SVT development

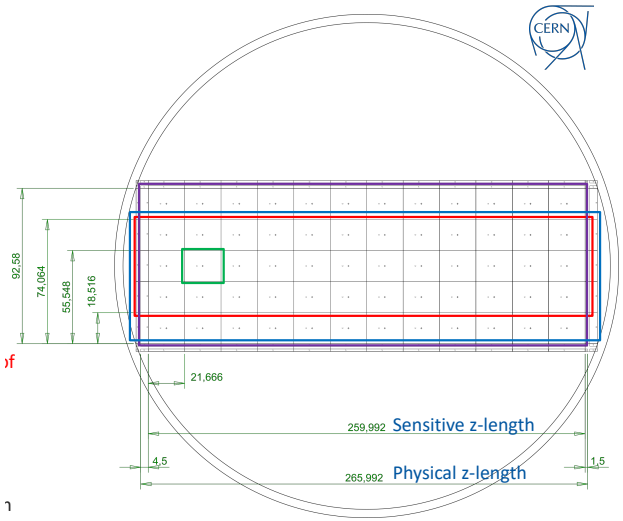
IB design

- Best insight into the dimensions of the RSU were 18.85 mm by 30.00 mm at the time when the October 2022 geometry was fixed
  - 9 RSUs were stitched and 3 to 5 of those 9 RSUs were grouped to form a wafer-scale sensor (see top sketch)
- At the time, endcap was thought to be only on one side of the sensor
- The current L0 – L3 (active) lengths and radii are derived from these RSU dimensions
- The size of the RSU has now been fixed at 18.516 mm x 21.666 mm
  - The active length in z of the wafer-scale sensor is projected to be approximately 260 mm and the physical length in z approximately 266 mm
  - Small(er) impact to radii

Assumed wafer-scale sensor dimensions



ER2 size



OB and ED, HD design

- For the OB and the ED/HD, the EIC LAS will be used
  - Reminder: EIC-LAS sensor = 1 segment made of N RSU + endcaps

- An initial study to define the EIC LAS size variants needed to tile OB layers and disks was carried out with the assumed RSU size and endcap on one side only
  - The study focused on finding the best coverage/maximise acceptance
  - Yield and manufacturing constraints unknown at the time

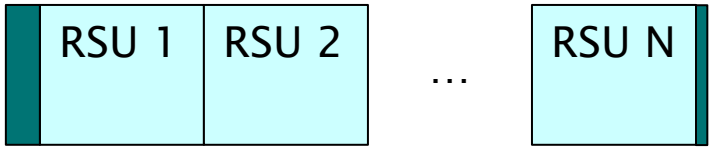
- This study resulted in up to 9 different EIC LAS sizes needed to achieve coverage of OB and ED/HD

- See details at https://indico.bnl.gov/event/17713/

OB and ED, HD design

- From recent ER2 developments
  - The size of the RSU has now been fixed at 18.516 mm x 21.666 mm
  - Endcaps on both sides of a segment (more on this later)
  - Discussions with ITS3 suggested that these many sensor variants might not be feasible based on current experience with the foundry
    - One sensor size per wafer accepted for ER1, i.e the 10 RSU long MOSS/MOST; foundry added single unit MOSS
    - NRE and production runs to be paid for each sensor size

EIC LAS sketch



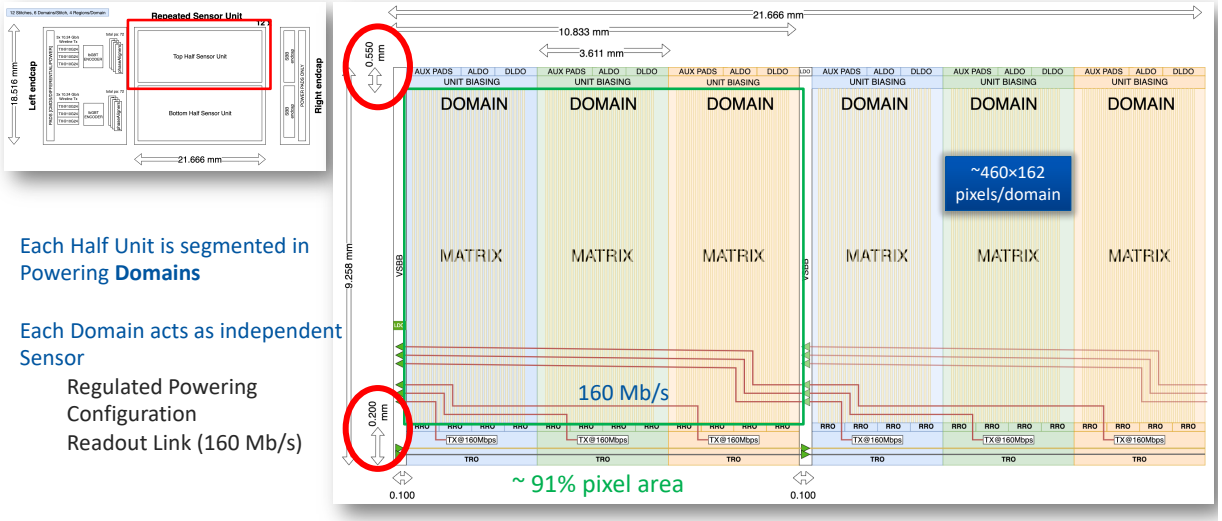
RSU: 18.516 mm x 21.666 mm
Left endcap: 18.516 mm x 4.5 mm
Right endcap: 18.516 mm x 1.5 mm

- OB and ED/HD conceptual design needs updating considering the new RSU size, the two endcaps and their dimension, the need to use 2 (at most 3) sensor variants

RSU architecture

- In ER2, each RSU is divided into a top half and a bottom half
- Each half RSU has 6 independent domains
- Circuitry for power regulation, config, data in each domain reduces the RSU sensitive area to ~91%
  - Needs to be considered in OB/ED/HD new conceptual design study
- Pixel size: 20 μm in r-phi, 22.5 μm in z

Half Sensor Unit Architecture



Each Half Unit is segmented in Powering **Domains**

Each Domain acts as independent Sensor

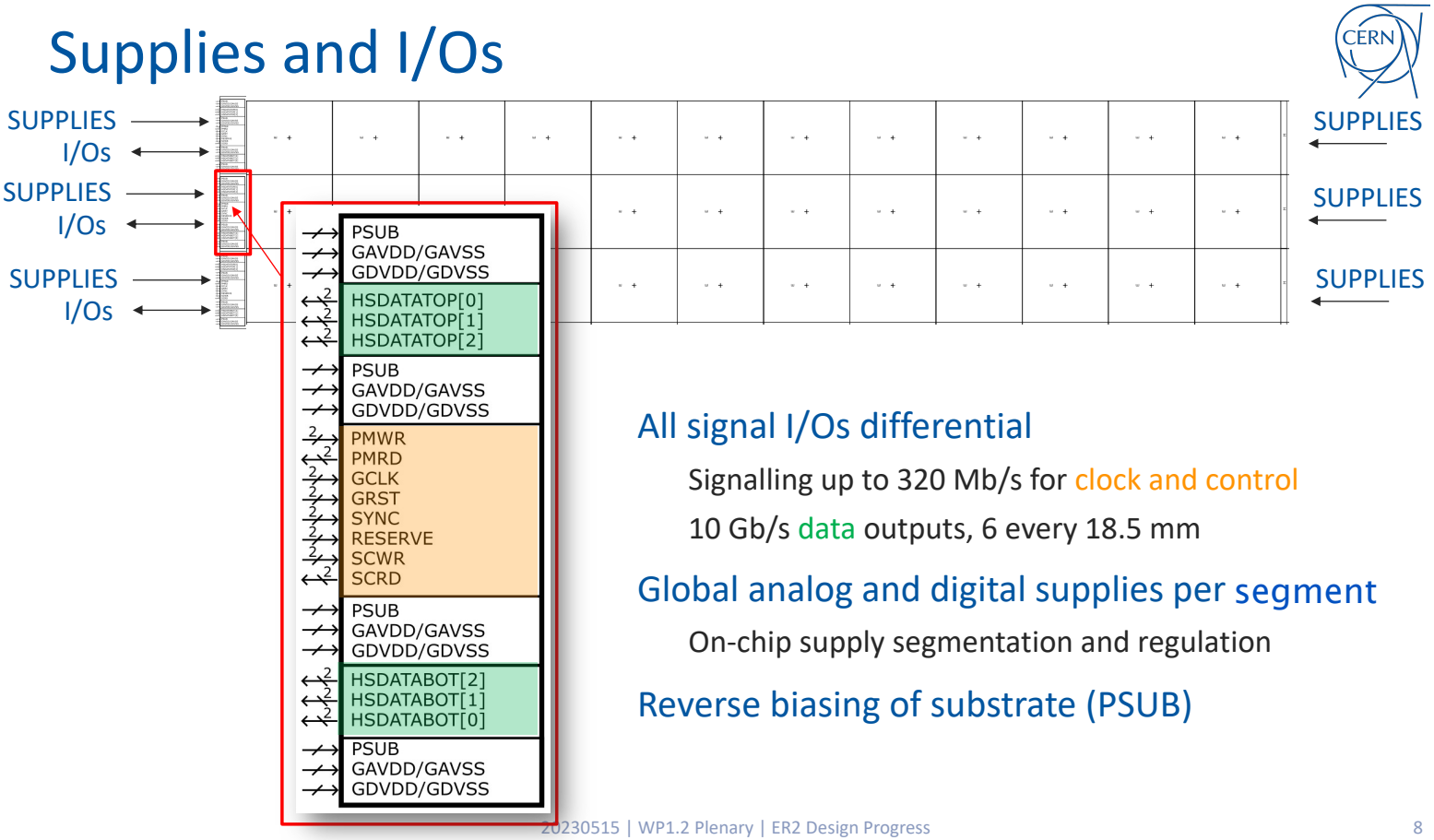
- Regulated Powering
- Configuration
- Readout Link (160 Mb/s)

460×162 pixels / domain
144 domains / segment
10.73 Mpixels / segment

https://indico.cern.ch/event/1280150/

ER2 supplies and I/Os

Supplies and I/Os



All signal I/Os differential

Signalling up to 320 Mb/s for clock and control

10 Gb/s data outputs, 6 every 18.5 mm

Global analog and digital supplies per segment

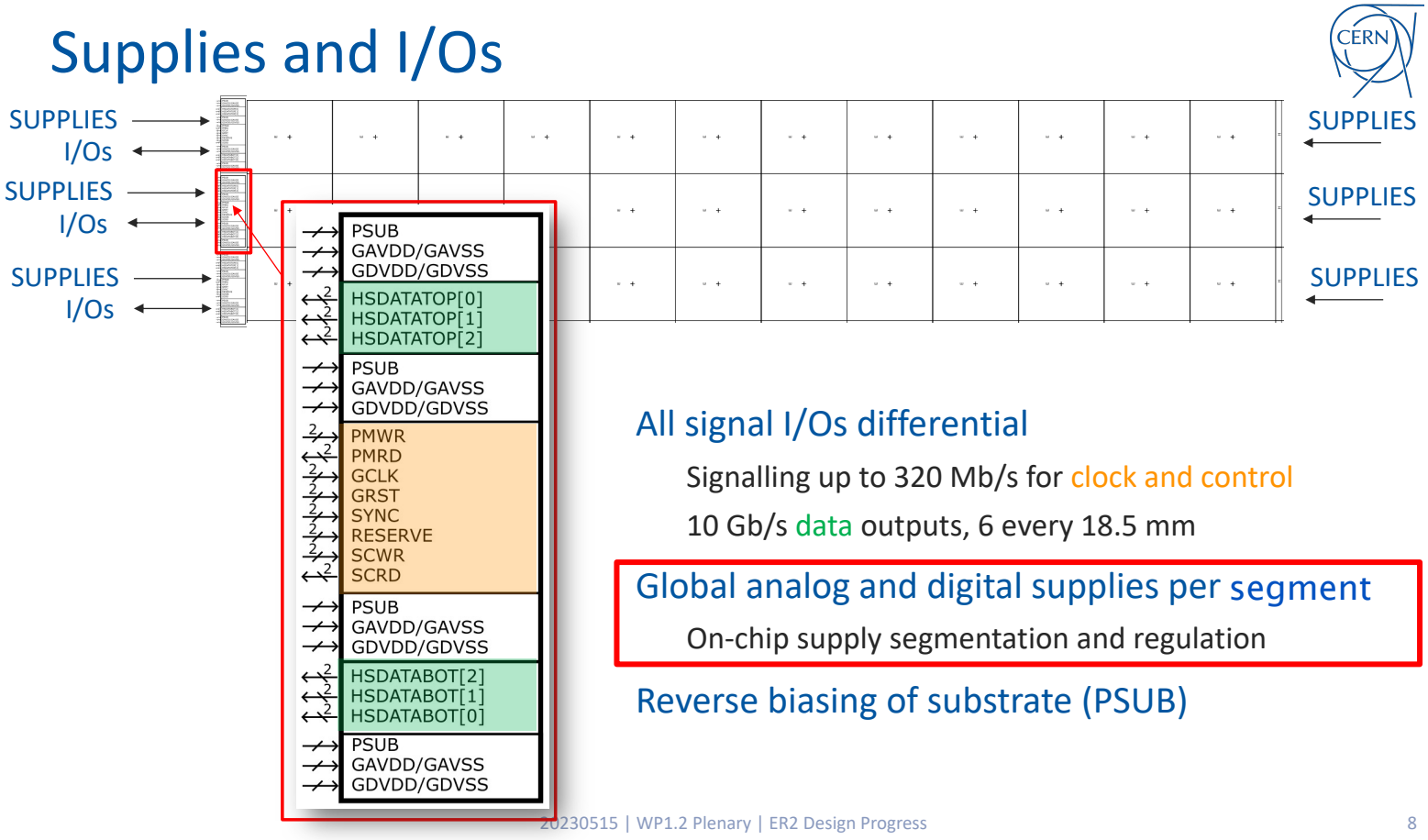
On-chip supply segmentation and regulation

Reverse biasing of substrate (PSUB)

- Reminder: MAPS sensors integrate both sensor and ASIC functionality in one silicon substrate, so they need both analogue and digital supplies for the electronics, and reverse bias for the sensor

https://indico.cern.ch/event/1280150/

ER2 supplies and I/Os



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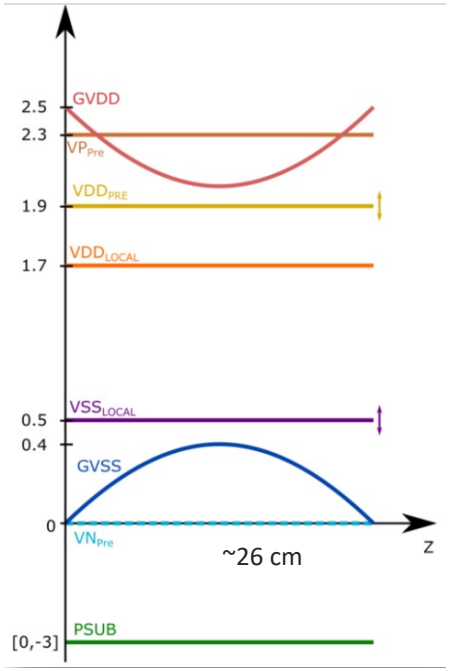
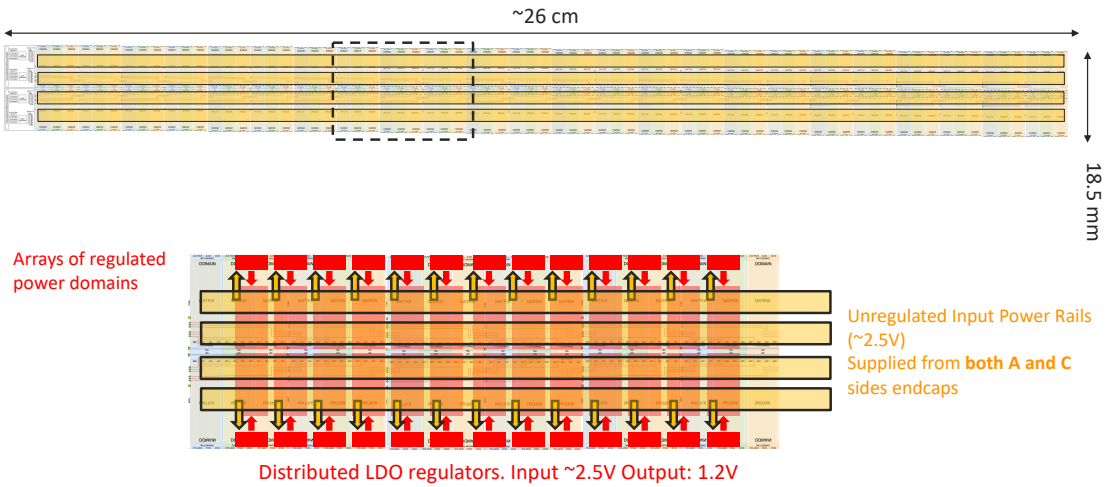
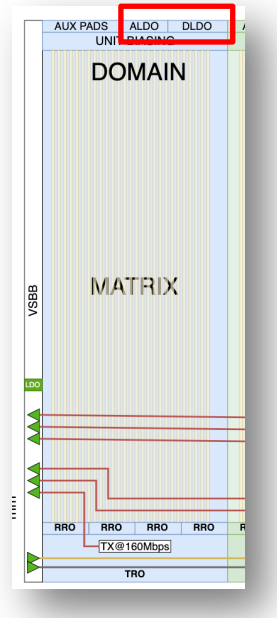
Power regulation on ER2 segment

- Segmented power domains allow to switch off 1/12 of each RSU
- Large IR drops over the segment length, ~26 cm
  - Double side supply, i.e. power distributed from left and right endcap
  - Regulation in each power domain to cope with IR drops of several hundred millivolts, at the price of significantly larger thermal dissipation







https://indico.cern.ch/event/1280150/

Impact of double sides supply: IB

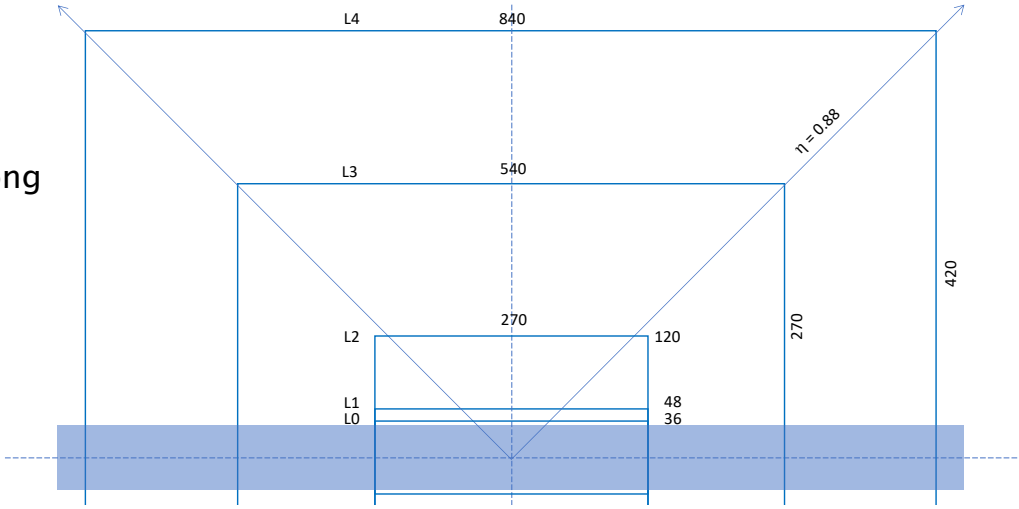
- October 2022 geometry assumed services on one side only of the wafer-scale sensors in the IB, routed in the hadron going direction to minimise material in the electron going direction

- This is no longer possible as power needs to come in from both sensor sides

L0, L1 and L2 lengths are sensors that are ~270 mm long
Services on one side only; no services in active area;
0.05% X/X0

Units = mm

October 2022 geometry



Impact of double sides supply: IB

- Two options
  - Route power cables from both sides
  - Route power in active area from one side of the sensor to the other via Flexible Printed circuit or Redistribution Layer (RDL) on sensor backside

- Choice depends on
  - Impact of more material in the electron going direction versus more material in IB active area
  - Effect of FPC/RDL on bent, thin sensor

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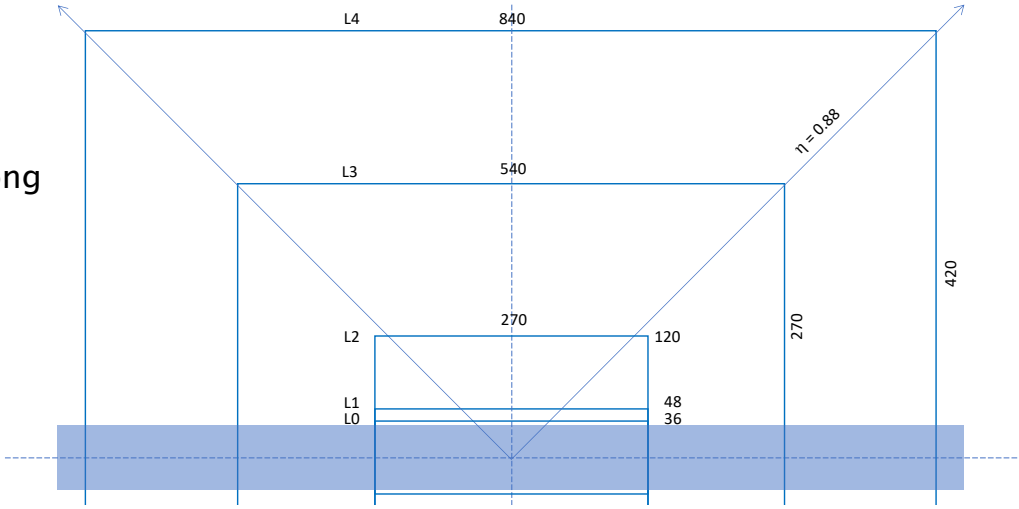
Services on one side only; no services in active area;
0.05% X/X0

Units = mm

October 2022 geometry



Impact of double sides supply: OB

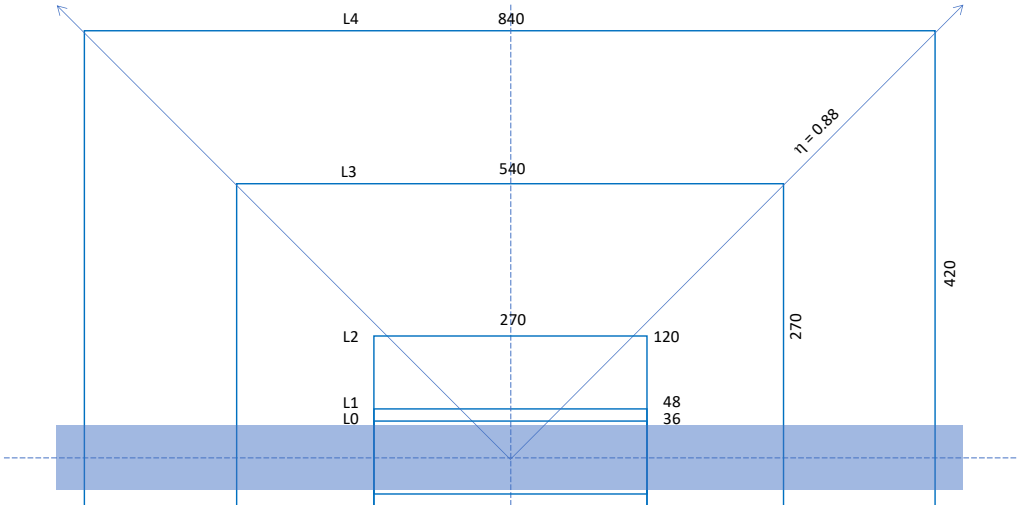
- The L3 design to achieve 0.25% X/X0 assumed two segments of maximum length, back to back, with services coming in on one side of each, i.e. no services in active area
  - With the double sided supply, power routing is needed along the stave (FPC or RDL)
- L4 already assumed an FPC along the stave, but the power distribution on two sides might require larger stave coverage with FPC
  - Also here an RDL could be used instead of the FPC

L3 length is achieved using two sensors ~ 270 mm long, placed back-to-back;
Services come in on the two sides of the stave; no services in active area; 0.25% X/X0

L4 length can be achieved using four sensors ~210 mm long;
Services need to run on the stave to reach middle EIC LAS sensors; 0.55% X/X0

Units = mm

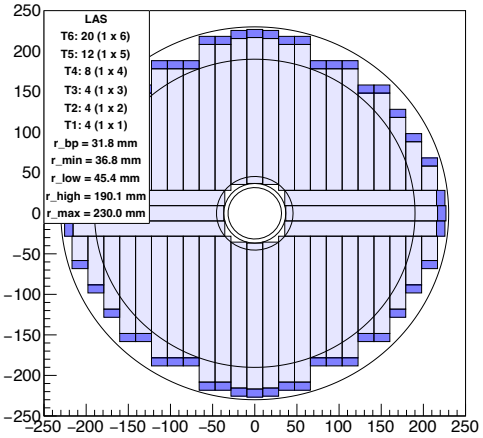
October 2022 geometry



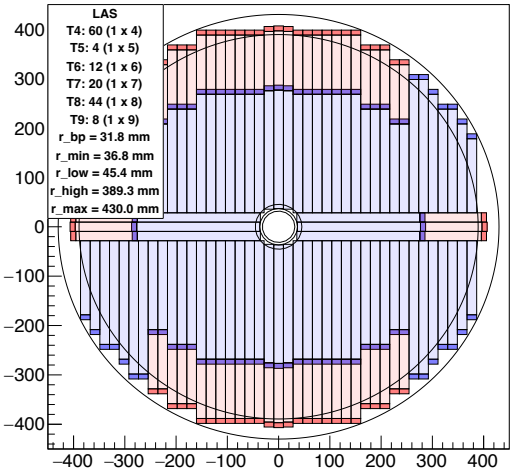
Impact of double sides supply: ED, HD

- The figures on the side are examples of disk configuration from the previous tiling study
  - EIC LAS of different colour are on opposite side of the disk (red stops where blue starts)
  - Darker areas are the endcap
  - See https://indico.bnl.gov/event/17713/
- For ED/HD0, the configuration did not foresee services running along the disk; endcap were located at the outer edge of the disk
- For ED/HD1-4, services for blue sensors run in front of red sensors (on opposite side)
- With power on two sides, FPC or RDL needed along sensors to bring power to both sides

ED/HD0



ED1/ED2/HD1



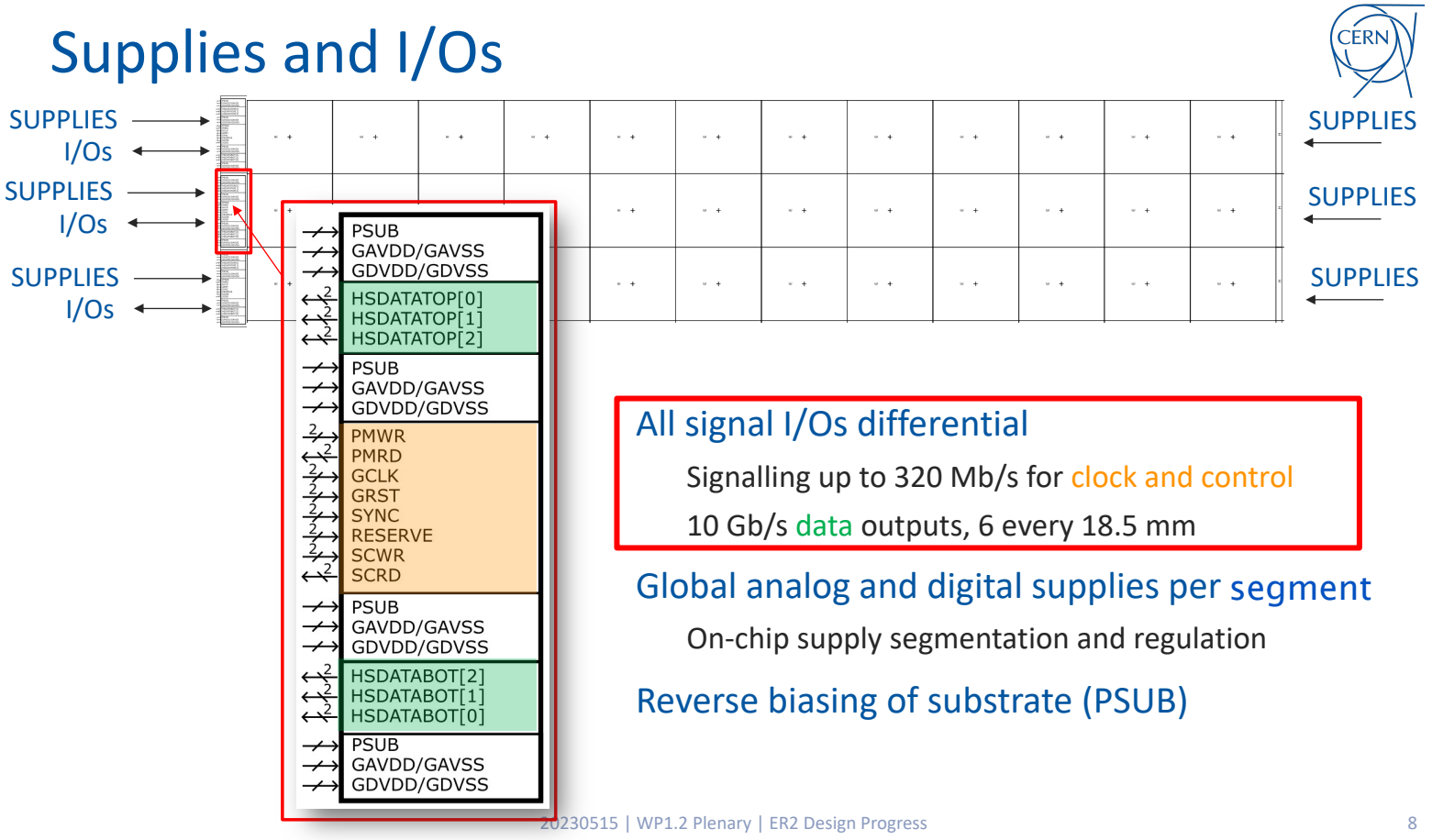
Impact of double sided supply: further considerations

- As the EIC LAS sensor for the OB layers and disks will consist of shorter segments, power might not be needed from two sides.
  - However, shorter sensor means a larger number of sensors in OB and disks. In some places (L3, ED/HD0) this will result in more material as services will need to run in active area.
  - OB and disks new conceptual design study needs to consider material, coverage, yield, and cost trade-off between longer sensors with two endcaps and short sensors with one endcaps

- R&D on RDL is already included in the FY23 generic R&D programme. With respect to an FPC, it would be the solution with the lowest material budget.

- Note that the total current to the ePIC detector does not change, i.e. the total cable mass from the power supplies to the (vertex and barrel) layers and disks does not change.
  - The impact of this change is on the material budget of the active area for OB layers and disks, and of the IB layers active areas or other detectors in the electron going direction.

ER2 supplies and I/Os

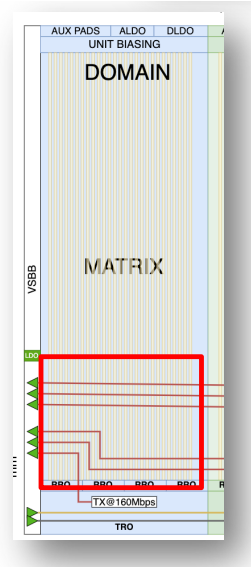


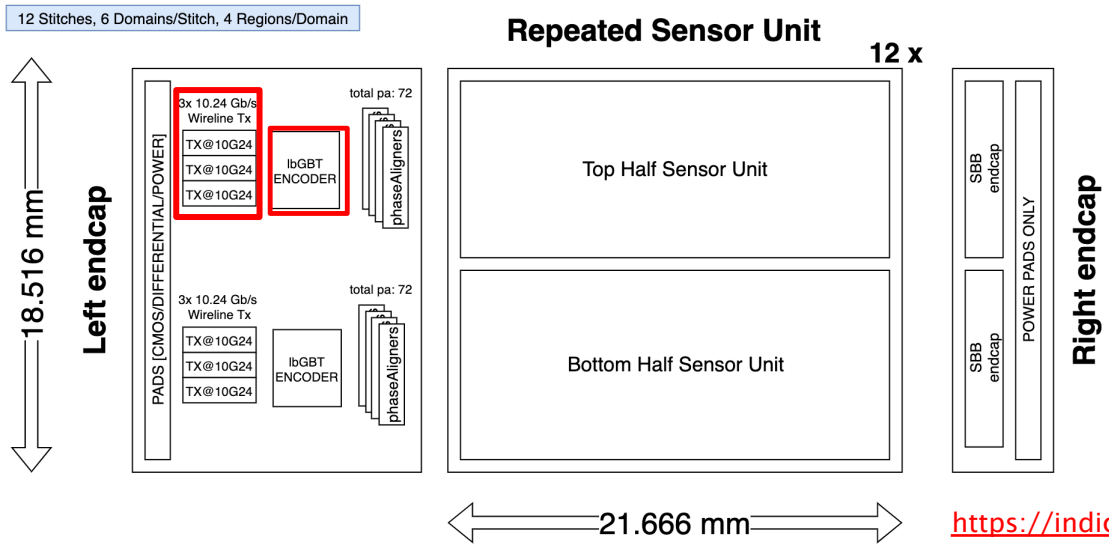
- Reminder: MAPS sensors integrate both sensor and ASIC functionality in one silicon substrate, so they need both analogue and digital supplies for the electronics, and reverse bias for the sensor

https://indico.cern.ch/event/1280150/

Data transmission on/off ER2 segment

- On-segment
  - 26 cm range 160 Mb/s on-segment transmission lines (possibly up to 320 Mb/s)
- Off-segment
  - 320 Mb/s clock and command lines
  - High speed (10 Gb/s) wireline drivers for data, 6 per segment
    - Need to drive signals at this speed on 50 cm of FPC
  - Integration of (parts of) lpGBT encoder in left endcap
    - Sensor output can drive optical transceivers (VTRX+)





https://indico.cern.ch/event/1280150/

Integration time in ER2

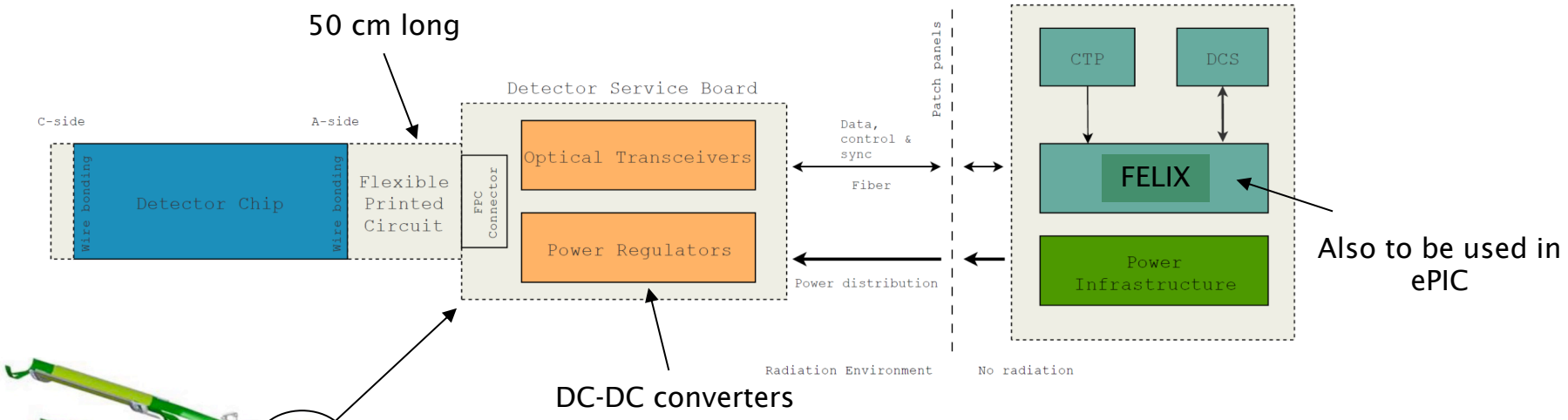
- The integration time for ER2 targets figures similar to ALPIDE, 5/10/20 μs
  - Figures of 5 μs and below are challenging given the power budget, design for manufacturing (DFM) rules, and speed of data transmission on chip
- The power budget, amongst other things, sets a lower limit to the time walk
  - The time walk is 3.3 μs in the MOSS, but timing specs are being reviewed for the ER2 targeting <2 μs
- The ER2 integration time will be programmable, below 5 μs
- Target integration time for ePIC is 2 μs
  - Faster layers could be used in the ePIC SVT where material is less of a concern if a faster integration time can be supported by the on-chip data transmission speed needed at ePIC occupancy (ITS3 occupancy is a limiting factor with the achievable on- chip speed)

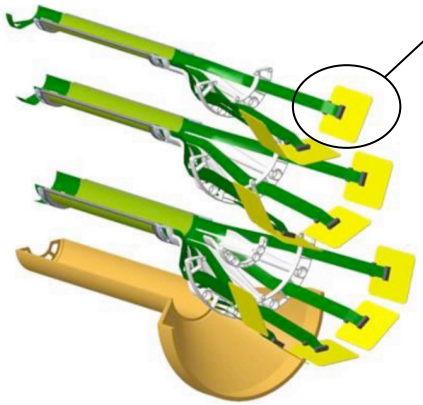
Integration aspects

- Power distribution
- Readout scheme
- Staves/disks
- Cooling
- Mechanics for integration

- As we use the same/similar sensor, it makes sense to look at what ITS3 is doing, but there are large differences…
  - Size/sub-systems (IB, OB, disks)
  - Data rates
  - Radiation levels

ITS3 power and data schemes





- The ITS3 does not have OB layers and disks, ePIC SVT does; constrains placement of detector service board
- Data rate of the ePIC SVT estimated to be few tens of Gb/s, much lower than ITS3
- Radiation levels expected to be lower for ePIC
- Serial powering chosen for the ePIC SVT

R&D progress in FY23 and plans for FY24 - eRD104 @ https://indico.bnl.gov/event/19740/

Data transmission for the ePIC SVT

- Multiplex output links as ePIC SVT rate is lower
  - External rad-hard FPGA or
  - Integrated multiplexer in left endcap (EIC LAS modification)

- If links speed programmable, ePIC could also use lower transmission speed
  - Lower transmission speed → longer transmission distance on FPC
  - Impact on how far/close the detector service board could be

- Low radiation levels at ePIC also beg the question as to whether the optical/electrical interface could be placed close to the sensor
  - i.e. place detector service boards at the end of stave/disks and use only fibers all the way from to FELIX
  - Not a eRD104 line of development; just Laura's idea

- Note: the detector service boards will need cooling (more in later slides)

Readout and DAQ for ePIC SVT @ https://indico.bnl.gov/event/17882/
Update on readout @ https://indico.bnl.gov/event/19390/
R&D progress in FY23 and plans for FY24 - eRD104 @ https://indico.bnl.gov/event/19740/

Powering scheme for the ePIC SVT

- Serial powering is chosen as the scheme to deliver analogue and digital supplies to the ePIC EIC LAS sensors

- ATLAS/CMS Shunt-LDO regulator selected for the ePIC SVT serial powering
  - The Shunt-LDO will be external, close to the EIC-LAS, not integrated
    - No change of ER2/3 needed for EIC LAS powering scheme
    - Shunt-LDO regulator can be prototyped and produced in a cheaper technology

- Cabling (number and type) for serial powering estimated in collaboration with the project, however
  - Current estimates of sensor power consumption do not include overhead for regulation on-segment and Shunt-LDO
  - Voltage at which power is transmitted will be higher (~3V), not a problem
  - Current will be higher → Impact on services cross-section (i.e. ePIC detector material budget and routing/integration)

Powering scheme for the ePIC SVT @ https://indico.bnl.gov/event/18202/
Update on ePIC powering and associated services estimates @ https://indico.bnl.gov/event/18525/ and https://brookhavenlab.sharepoint.com/:f:/s/EICPublicSharingDocs/Ev9-slM6cgBAh56pykNTLSUB_VcgKukdnQMhoTfdJDbUTg?e=dNvjZ7
Regulator design for serial powering @ https://indico.bnl.gov/event/18853/

ePIC SVT mechanics and cooling

- Bending and interconnections at larger ePIC SVT radii need study
  - Layer 2 radius is much larger than ITS3; do we need another support cylinder between layers 1 & 2?
- Dedicated design of lightweight staves and disks
- Cooling
  - Operational temperature need to be defined (20C for ITS3)
  - How to channel air flow to vertex layers? (i.e. we have disks in the way)
  - Cooling for OB and disks
    - Integrated in mechanical structure
    - Monophase or 2-phase? Air through carbon fiber?
- FPC on staves/disks
  - Laminated on mechanical structure?

eRD111 updates https://indico.bnl.gov/event/18525/
Engineering challenges of initial ePIC SVT configuration https://indico.bnl.gov/event/17713/
R&D progress in FY23 and plans for FY24 - eRD111 https://indico.bnl.gov/event/19740/

Final remarks

- There is a lot of interesting and challenging work to do!

- The ePIC SVT detector is not a copy of ITS3
  - The sensor design is shared but mechanics, cooling, powering, readout, etc need dedicated developments

- The ePIC SVT workforce needs to grow further to achieve the required critical mass
  - Institute presentations today show we are on a good path

- There is a lot more I did not cover
  - Beam pipe bake out
  - Mechanics and integration
  - Detector description in simulations
  - …

Backup

A few words on sensor yield

- A yield figure will be difficult to have in the short term
- Only 24 ER1 wafers
- ER2 design different from ER1
  - Higher segmentation of RSU to switch off parts of it in case of issues
- How is 100% yield defined?
  - Fully working EIC LAS?
  - EIC LAS with M sub-RSU switched? What M can we afford?
- We might have to proceed by studying what are the best EIC LAS sizes, independently of yield, and then fold in a “safety factor”