R&D on Readout Electronics for ePIC TOF

Project Goal: Completing the readout chain for an AC-LGAD based TOF

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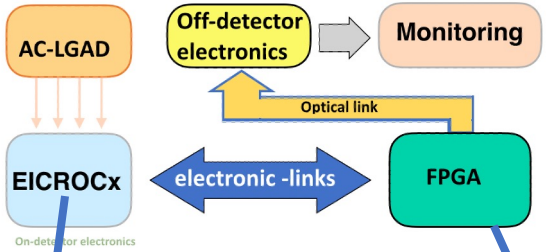
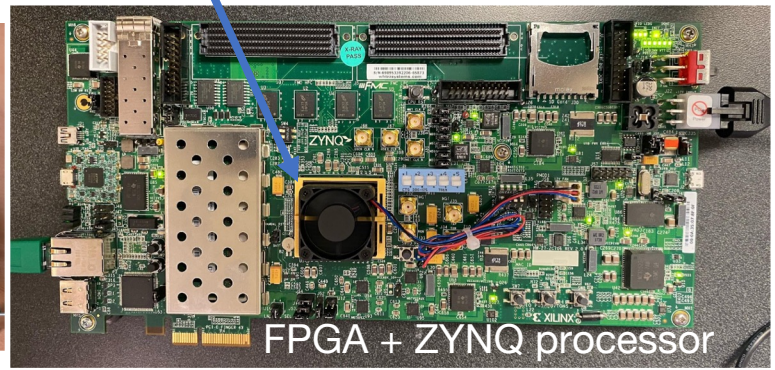
Progress so far at BNL with Xilinx dev kit



EICROC0 at BNL

Xilinx dev kit at BNL


EICROC0 on PCB


FPGA + ZYNQ processor

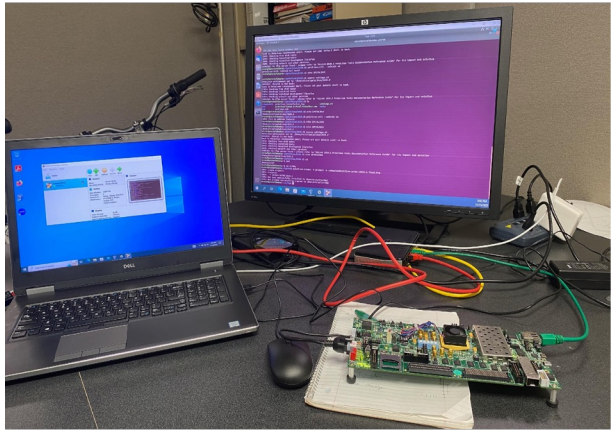
What we have so far for the first step of R&D:

1) One Xilinx dev. kit (ZYNQ processor + FPGA),
2) EICROC0 on a PCB

Read out board development setup at BNL

Stage 0 (FY 23):Establishing the foundation

- Procured EICROC0 ASIC PCB and bonded AC-LGAD + EICROC0 onto the PCB with BNL's instrumentation division
- Made necessary corrections to the PCB
- Acquired Xilinx development kit and set up a test stand at BNL
- Installed required software and firmware, currently modifying software for connections
- Aim to create a fully operational test stand combining sensor, ASIC, and prototype board
- Primary characterizations and replication of EICROCx developer's results
- Workforce development with involvement of two graduate students

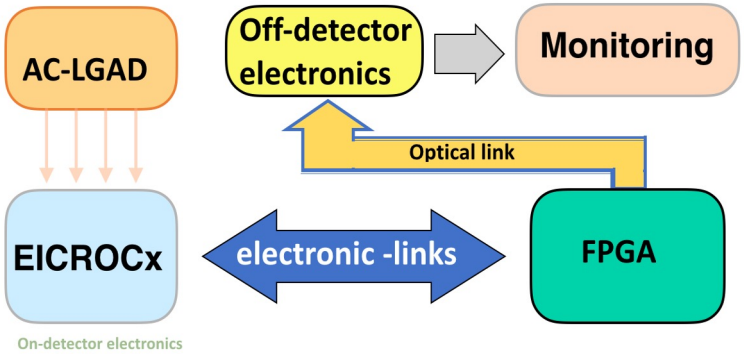


First chain with sensor + ASIC + readout kit is being ready at BNL

FY24 Proposal: stage 1 & 2

- ePIC TOF Readout Board (RDO): Crucial component of readout chain
- Interface PCB between electrical ASICs and fiber-based DAQ system
- Provides data paths, low-jitter clocks, and interfaces with ePIC DAQ
- Design goals: small, cost-effective, low-power, FPGA-based with SFP+ fiber interface, PLLs, clock cleaners, and ASIC connectors
- Different form factors for BTOF and ETOF detectors
- Expected data rates: <0.6 Gbs/fiber for BTOF, ~3 Gbs/fiber for ETOF

The development is divided into a three stage program, the stage 1 and 2 will be targeted in FY24



FY24 Proposal: stage 1 & 2

Stage 1 (First half of FY24):
- Prototype RDO using Xilinx Development Kit (e.g., ZCU106)
- Mount sensor and EICROCx ASIC on Front-End Board (FEB)
- Connect FEB and RDO using FMC connector
- Demonstrate TOF readout chain, use Ethernet interface for backend DAQ

Stage 2 (Second half of FY24):
- Develop complete RDO prototype with FPGA and other components
- Collaborate with ePIC DAQ team for TOF-specific customization
- Continue FEB-RDO connection via FMC connector
- Achieve full demonstration of TOF readout chain

The workload will be distributed to three institution BNL, Rice and ORNL

FY24 Proposal: crucial EE support

We need electrical engineer efforts for 12 months (6 months each for stage 1 and stage 2)

- BNL (0.5 FTE electrical engineer):
  - Interface with EICROCx designer, contribute to RDO prototype development (4 months)
  - Provide input on barrel design considerations (2 months)
- Rice (0.3 FTE electrical engineer):
  - Contribute to RDO prototype development (2 months)
  - Focus on end cap-specific designs (2 months)

- ORNL (More details on the Overleaf):
  - Maintain communication with BNL and Rice
  - Design, produce, and test flex PCB prototype for connecting readout ASIC and sensor assembly to RDO prototype

The EE will be key to communicate with EICROCx developer and tailor it to TOF requirement

FY24 Proposal: Budge & conclusion

Title: Budget
- Engineer Salary: $195,000
- Dev Kits: $10,000
- Other Components: $5,000
- Travel: $6,000
- Total: $216,000

- ePIC TOF RDO project aims to enhance performance of ePIC TOF detector
- Close collaboration with ePIC DAQ Group for prototyping and final versions
- Milestones: Establishing foundation (Stage 0), RDO prototyping and demonstration (Stage 1), customize RDO development and TOF chain demonstration (Stage 2).

The project will deliver sub-30 ps MIP timing systems for ePIC TOF compatible with far-forward AC-LGAD detectors.