EIC-UK WP1 Serial Powering Thoughts

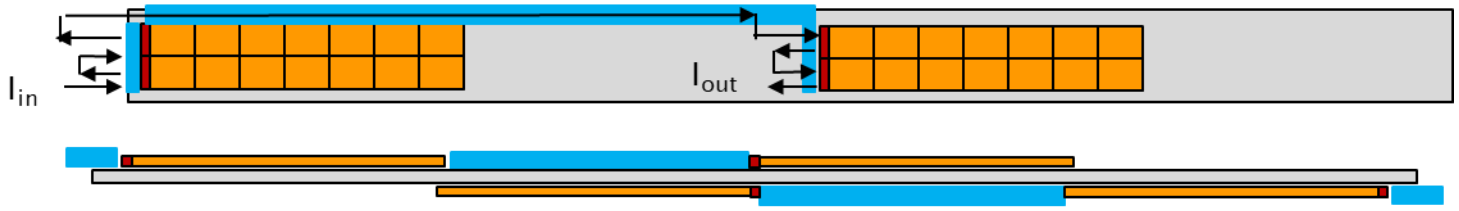
James Glover

Wednesday, 19th July 2023

Previous serial powering thoughts

As mentioned at the Liverpool F2F and previous ePIC SC meetings:

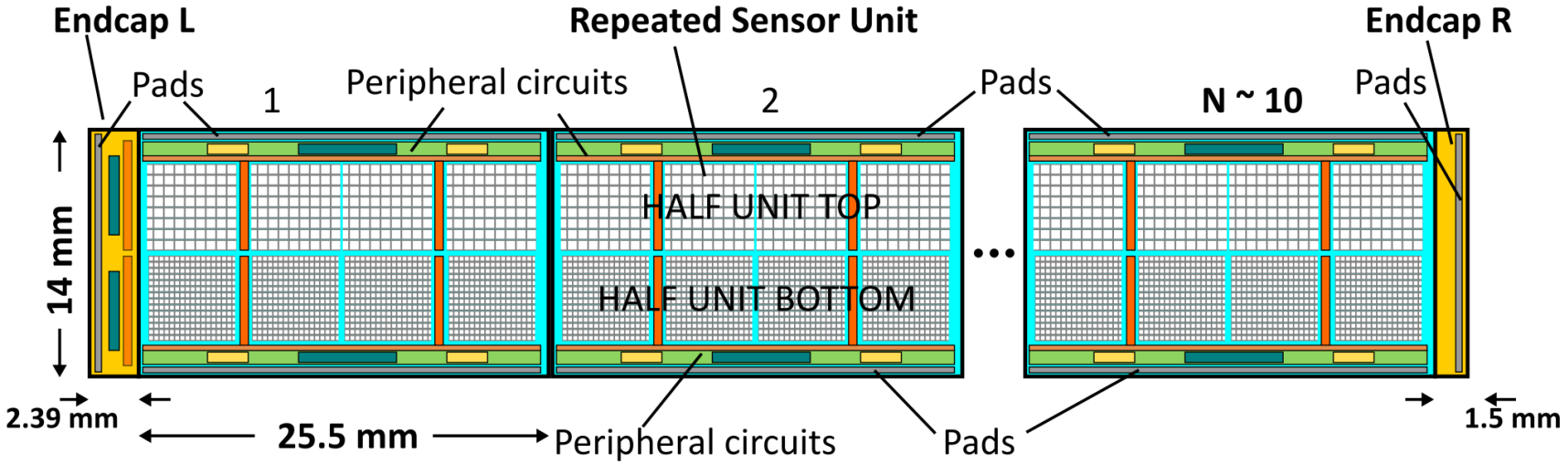
- Serial powering scheme chosen as baseline for the ePIC SVT.
  - Provides lowest material option.
- Shunt-LDO placement on a dedicated powering chip outside the sensor.
  - Allows re-using of ITS3 sensor on-chip power distribution; Does not require modification of sensor periphery; Can be prototyped and fabricated in cheaper technology.
- Serial powering scheme drafted for sagitta layers (prior to ITS3's ER1 delivery).
  - Current flowing between sensor segments on each side of the stave.
  - Factor 4 current reduction for L4, factor 2 current reduction for L3.



L4 serial powering scheme;
top – stave top view, bottom – stave side view

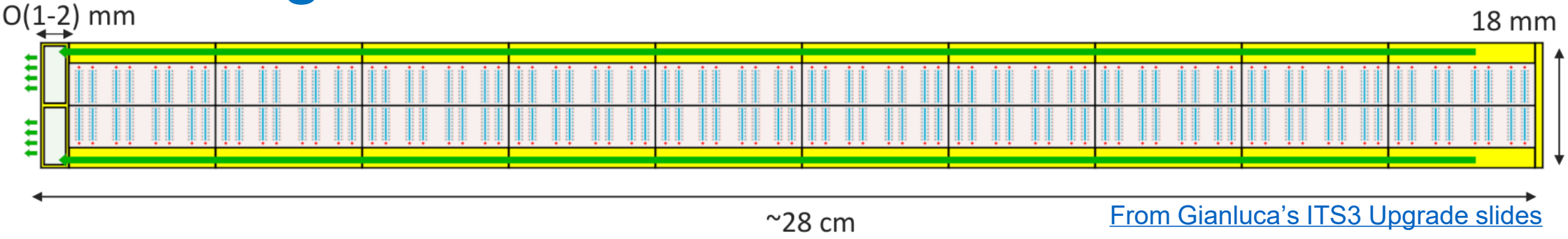
ER1 made things more complicated

- It was previously assumed that a wafer-scale, stitched sensor would have a single periphery (endcap) for all power and data connections.
- This turned out not to be the case; IR-drop across wafer diameter is too great.
  - A 2nd endcap is needed to power repeated sensor units (RSUs) from both ends (only account for IR-drop across half the RSUs). Data still be read from 1 endcap.



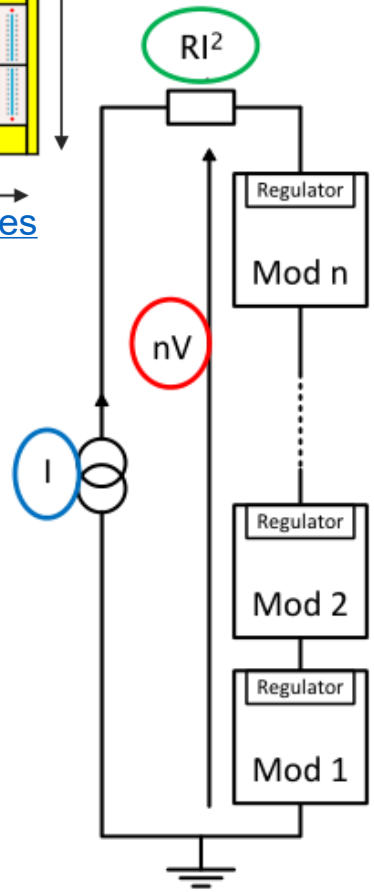
From Gianluca's ITS3 Upgrade slides

Things to remember.



From Gianluca's ITS3 Upgrade slides

- Serial powering (SP) requires all modules in the SP chain to have a different ground reference to the other modules in the chain (GND of Mod_N becomes V_{in} of Mod_{N+1}), with only the final module in reference to the power supply ground.
- Each RSU in the MOSS is not electrically isolated, therefore the whole MOSS must have the same GND reference.
  - ∴ The 2 endcaps cannot be in series to each other!
  - How do you get power to both endcaps (in a SP scheme)?



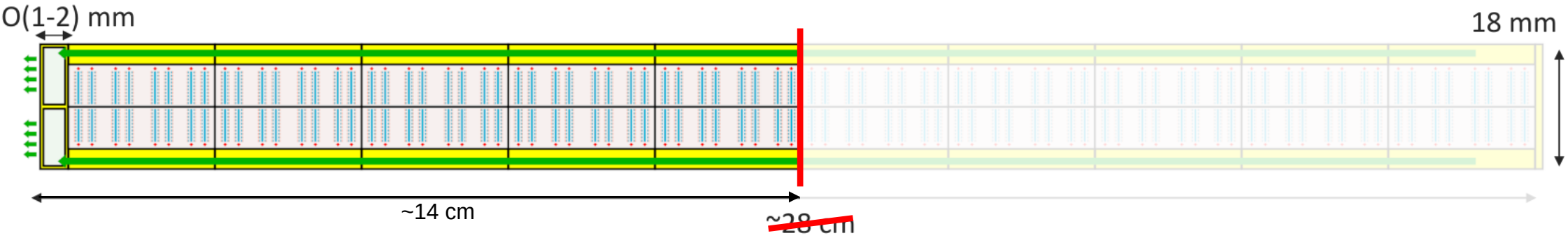
From Laura's EIC SC slides

What may be easiest

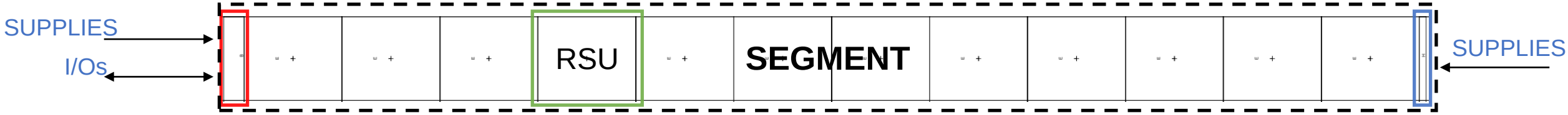
- Including half the RSUs per stitched sensor segment would remove the need for 2 endcaps.
- May need to include more segments in a single SP loop to keep material low.

However:

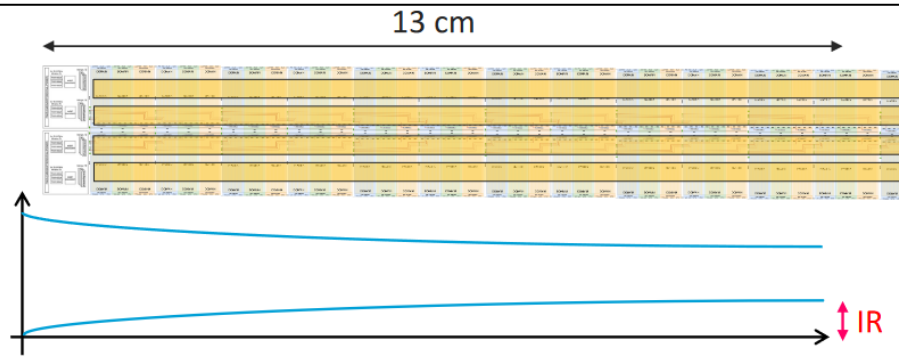
- Segments are not long enough for current layout plans.
  - L0, L1 & L2 would require 2 of these segments; L3 needs 4 segments; L4 needs 8 segments.
- This doubles the data connections as fewer RSUs are read-out as one segment.
- The power+data endcap is bigger the only power endcap.
  - ∴ 2 “half” segments are longer then 1 “full” segment. Is the wafer real-estate big enough the keep the at least as many RSUs on one wafer?



Additional considerations



- The design for ER2 keeps changing. As of last ITS3 plenary (30/06/2023):
  - Number and dimensions of RSUs; now 12 RSUs of 19.564×21.666 mm.
  - Endcap depth also changes; Left endcap now 4.5 mm and Right endcap is 1.5 mm.
  - May require extra fat metal traces to reduce IR-drop further (extra, nonuniform material within the segment, not such a SP issue).



From Gianluca's ITS3 Plenary slides

P_s [mW/cm2]	J_s mA/cm	I_s mA	Rail R Ohm	IR V		2*IR [V]	GVDD_in V]
10	8.3	108.3	3.68	0.20		**0.40**	2.00
20	16.7	216.7	3.68	0.40		**0.80**	2.40
30	25.0	325.0	3.68	0.60		**1.20**	2.80
40	33.3	433.3	3.68	0.80		**1.60**	3.20
50	41.7	541.7	3.68	1.00		**2.00**	3.60

L=13 cm
Current Metal (ER1)
V_{core} = 1.2V

P_s [mW/cm2]	J_s mA/cm	I_s mA	Rail R Ohm	IR V		2*IR [V]
10	8.3	108.3	0.321	0.017		0.035
20	16.7	216.7	0.321	0.035		0.069
30	25.0	325.0	0.321	0.052		0.104
40	33.3	433.3	0.321	0.069		0.139
50	41.7	541.7	0.321	0.087		0.174

L=13 cm
Fat Metal (request for ER2)
V_{core} = 1.2V

ePIC – Oxford Serial Powering update

B. Todd Huffman

Serial powering test lab

- Lab is close to ready
  - Not a clean room
  - Bench and rack and power supplies
  - Some items to be removed (and moved … next week)
  - New Computer
  - Test controls of power supplies (three weeks?)

Other items

- Babak and I to meet with Soniya Matthews at RAL 9 August
  - Purpose
    - Get lessons on Shunt-LDO regulator design
    - Understand schedule
    - Establish test plan that makes sense and fits with the project.
    - Get work for our Engineers that we can fire up the moment we obtain some funding!!!
    - Beg for anything we can get!

Additional slides

Lots of extra info from the 30th June plenary

- Many things relating to the current state of the ER2 design will have an effect of the EIC-LAS design.
  - Not just relating to serial powering!
- It is highly recommended that people have a look through Gianluca's slides:

https://indico.cern.ch/event/1298672/contributions/5460852/attachments/2676382/4641778/20230630-WP2-Report.pdf