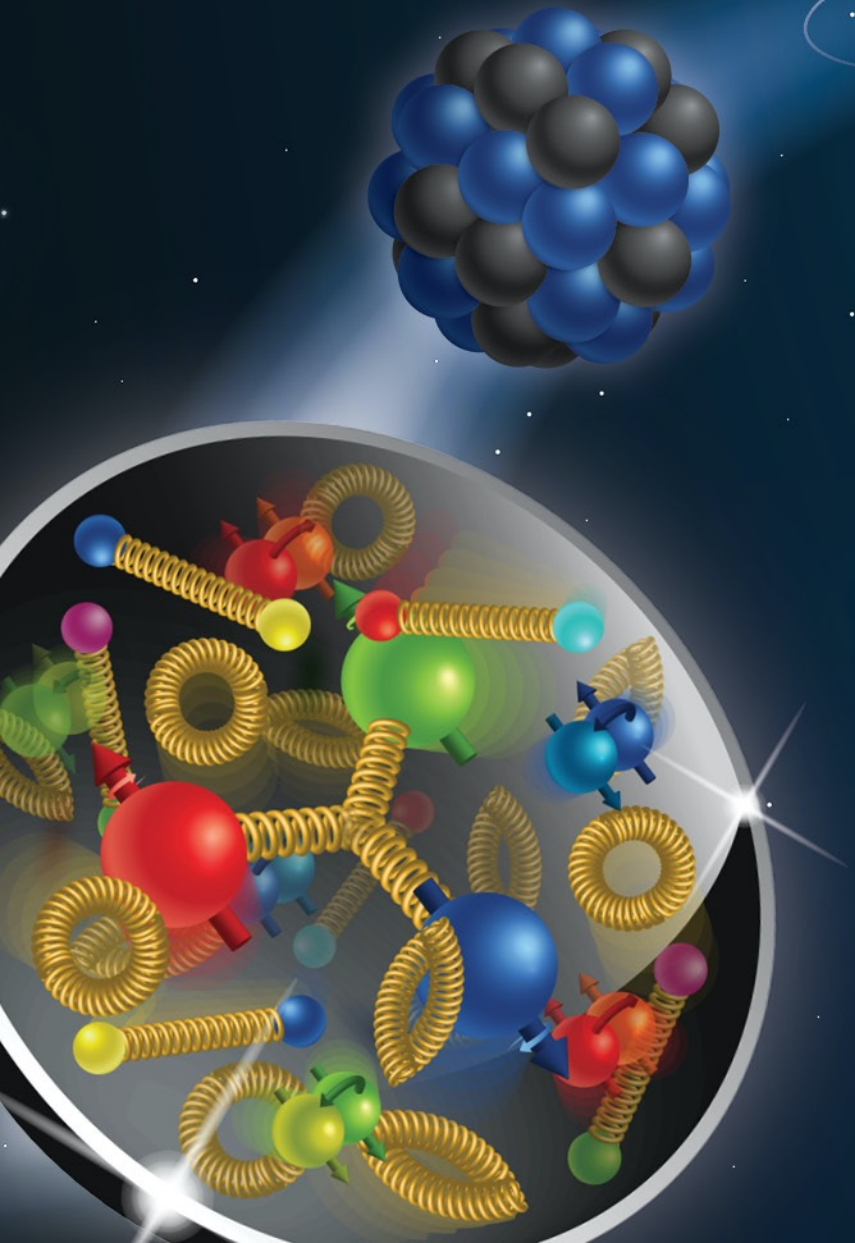


ePIC DAQ System Overview

Streaming Readout

David Abbott

Jefferson Lab

L3 CAM for EIC Detector Project

July 5-6, 2023

Electron-Ion Collider

BROOKHAVEN NATIONAL LABORATORY

Jefferson Lab

U.S. DEPARTMENT OF ENERGY | Office of Science

ePIC DAQ/Online Computing Overview

- The EIC Streaming Readout (SRO) Consortium was formed in 2018 with the goals of engaging the nuclear physics community in exploring the advantages, challenges and requirements to implement a 100% streaming readout architecture for the EIC detectors.
  - Series of ten workshops between 2018 and 2022.
  - General agreement in the Yellow Report, that the adoption of SRO would maximize the impact of the physics program for EIC.

- Talk Outline
  - General DAQ architecture
  - Expected technology choices
  - Interface with Detector Systems – PID focus
  - Relative schedule wrt to the EIC Detector project

EIC Streaming Readout Community

- **ePIC Electronics/DAQ Working Group**
  - J. Landgraf (BNL), F. Barbosa (JLab), J. Huang (BNL)
  - Regular meetings to focus on design and requirements specifically for the new ePIC detector
  - Interface to detectors, readout, DAQ, online processing, monitoring and control.

- **ePIC Software/Computing Working Group**
  - M. Diefenthaler (Jlab), S. Joosten (ANL), T. Wenaus (BNL), W. Deconinck (UM)
  - Coordinating software development for EIC physics
  - Analysis Frameworks, Reconstruction, Simulation, AI & ML
  - Online Filtering (e.g. event ID, calibration)

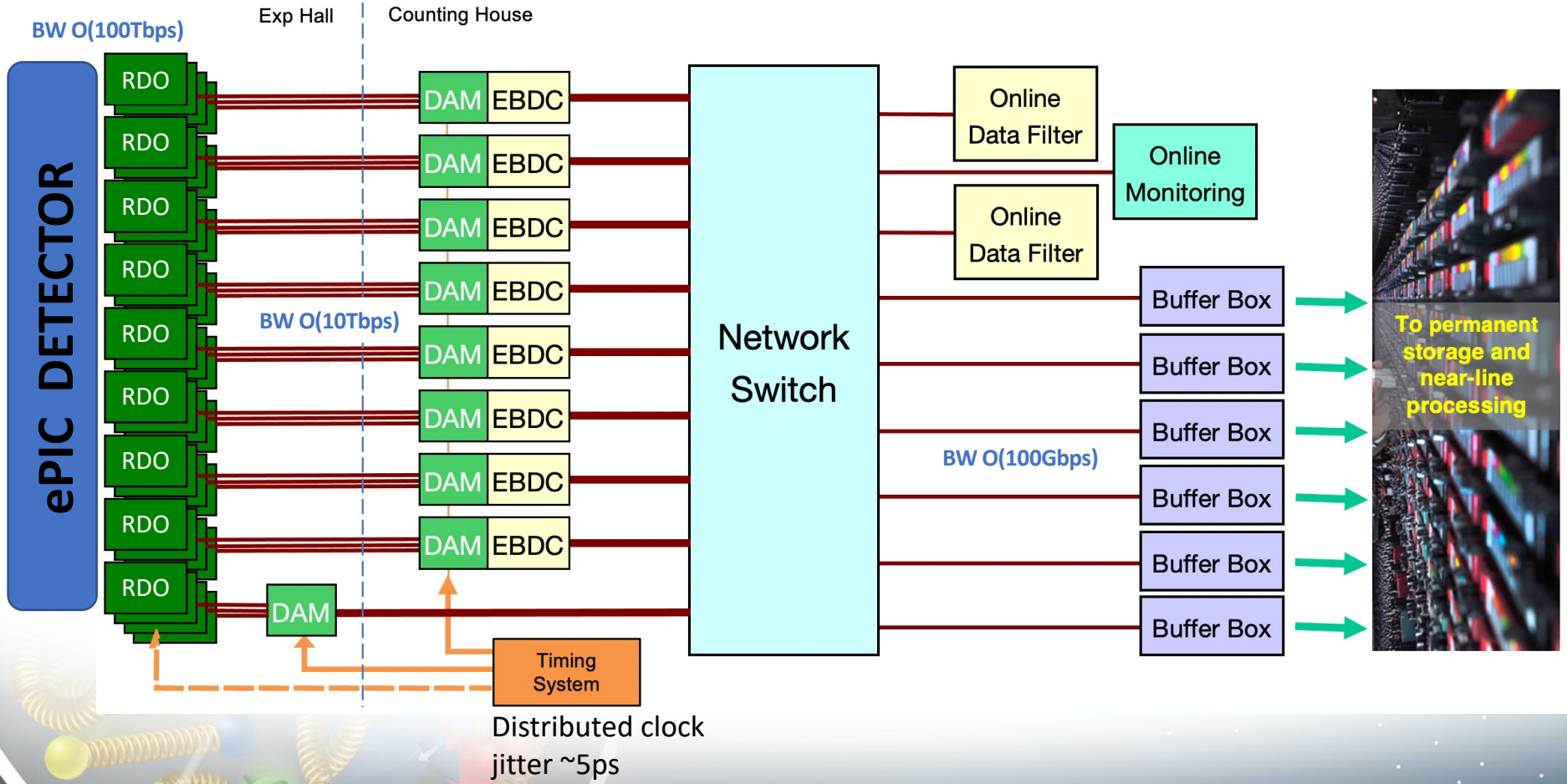
- **EIC Project L3 CAMs (DAQ/Online, Electronics)**
  - D. Abbott (JLab), J. Landgraf (BNL), F. Barbosa (JLab)
  - Project management (cost/schedule)
  - Coordination between relevant EIC working groups (including Detectors)

Streaming Readout Architecture

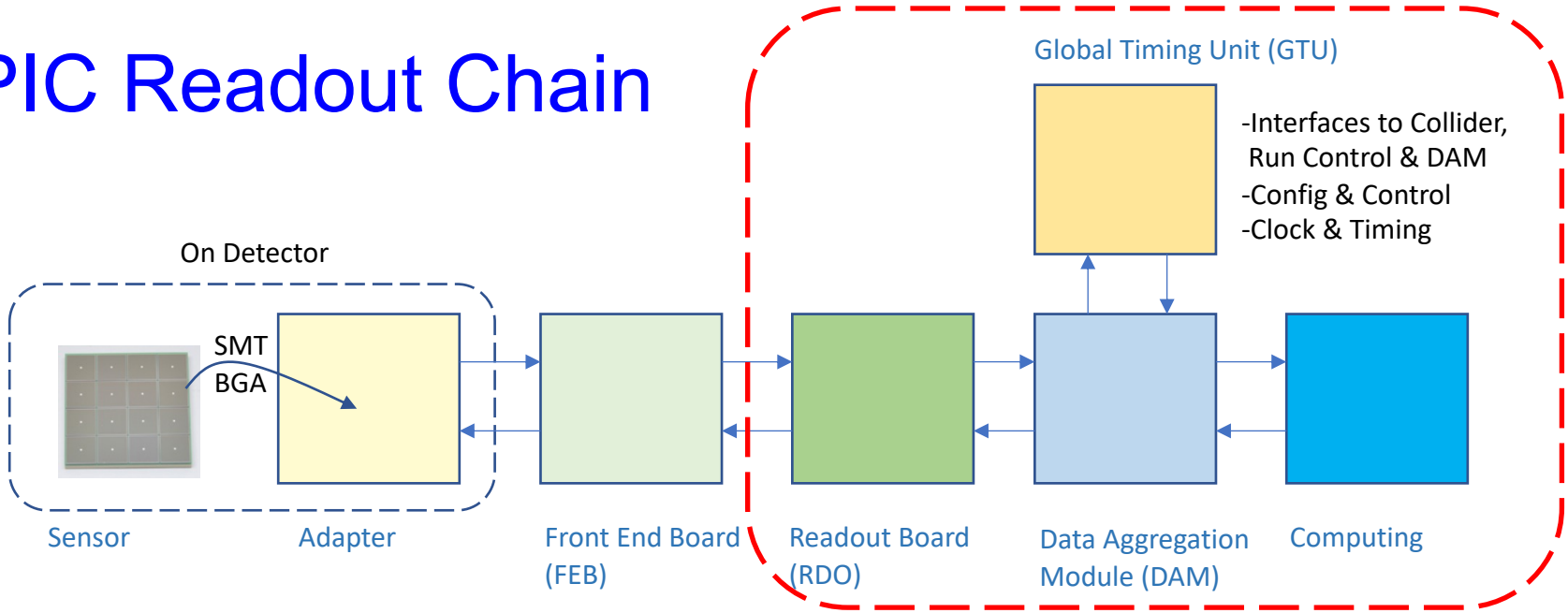
- No hardware-based trigger (well just optional…)
  - Elimination of dedicated hardware and ability to select events based upon the full detector are the main advantages.
  - Exposure to background and noise is the main challenge
  - All front-ends are free-running (or self-triggered)
  - Data flow (congestion) is managed at individual sources
- Streaming requires a robust and accurate distributed clock delivered and synchronized to all the front-ends
  - All data are characterized by detector/channel ID and a time-stamp
- Real time filtering, processing and reconstruction
  - Online vs Offline tasks become blurred
  - Adds requirements such as the need for event identification & quasi-real time monitoring/calibration for filtering and physics results
  - This is the focus of the EIC Software and Computing Group

ePIC Streaming DAQ/Computing Architecture

Bunch Crossing ~ 10.2 ns/98.5 MHz
Interaction Rate ~ 2 us/500 kHz
Low occupancy.



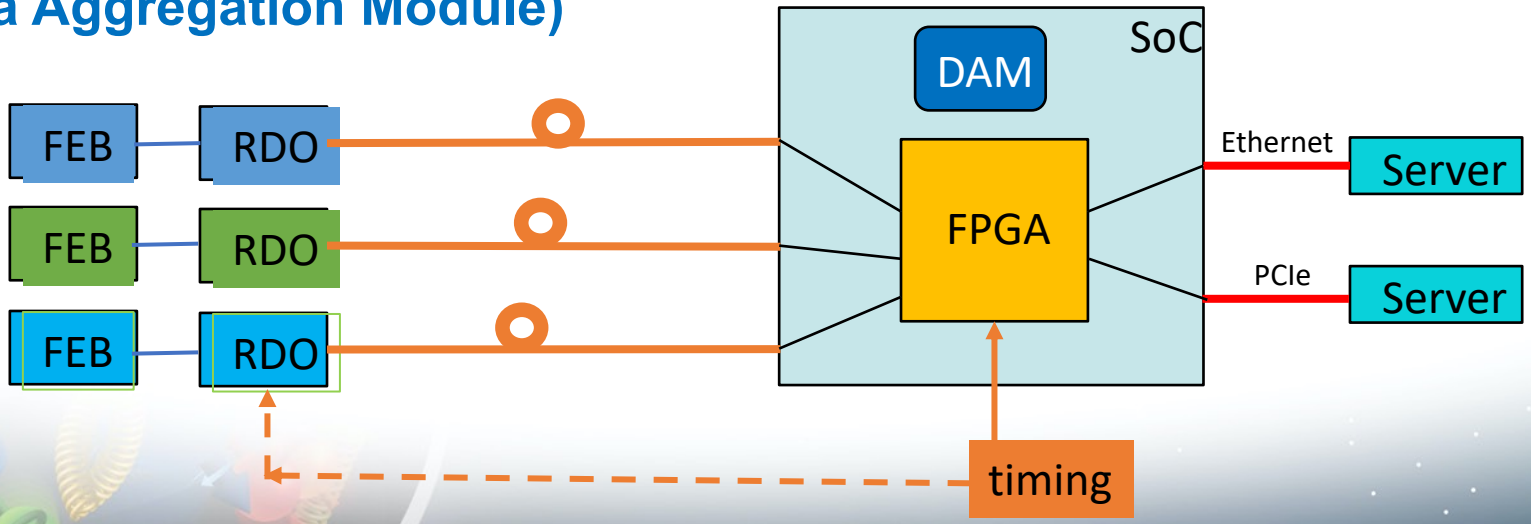
ePIC Readout Chain



Name	Sensor	Adapter	Front End Board (FEB)	Readout Board (RDO)	Data Aggregation Module (DAM)	Computing
Design	**Detector Specific**	**Detector Specific**	**Detector Specific**	**Few Variants**	**Common**	**Common**
Function	-Multi-Channel Sensor	-HV/Bias Distribution -HV divider -Interconnect Routing	-Amplification -Shaping -Digitization -Zero Suppression -Bias Control & Monitoring	-Communication -Aggregation -Formatting -Data Readout -Config & Control -Clock & Timing	-Computing Interface -Aggregation -Software Trigger -Config & Control -Clock & Timing	-Data Buffering and Sinking -Calibration Support -QA/Scalers -Collider Feedback -Event ID/Building -Software Trigger -Monitoring
Attributes	-MAPS -AC-LGAD -MPGD -MCP-PMT -SiPM -LAPPD/HRPPD	-Sensor Specific -Passive	-ASIC/ADC -Discrete -Serial Link	-FPGA -Fiber Link	-Large FPGA -PCIe -Ethernet	-COTS -Ethernet

DAQ Interface to the Detector Systems

- Managing data “streams” is ideally done in a deterministic way – e.g. FPGAs
- Proprietary communication with the front-end electronics.
  - Bi-directional link (fiber)
  - Send: clock, commands, control, config
  - Receive: high speed data streams
- System on Chip (SoC) facilitates DAQ/User applications to communicate with the Front-end.
  - Readout, Configuration and Control
- **DAM (Data Aggregation Module)**

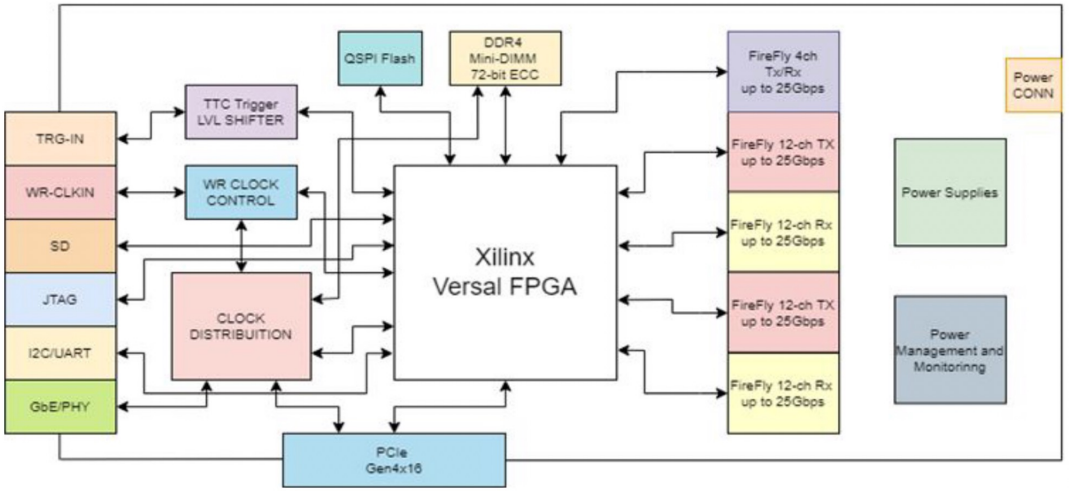


DAM Option - Front-End Link Exchange (FELIX)

- Originally developed for ATLAS at CERN
- Design team is based at Brookhaven
  - Current version (FLX-172) in use at BNL for sPHENIX
- New board being prototyped now for ATLAS HL-LHC running.

FPGA: Xilinx Versal Prime XCVM1802

- PCIe Gen4 x16
- 24 Firefly links with 3 config options
  - 24 links @ 25Gbs
  - 24 links @ 10Gbs
  - 12 @ 25Gbs + 12 @ 10Gbs
- 4 additional Firefly links
- Front Panel: Fiber I/O
  - Additional 3 Inputs, 3 Outputs
- 1 DDR4 Mini-UDIMM
- USB-JTAG/USB-UART



Block Diagram of FLX-182 Prototype

Notes: The Xilinx Versal Prime is a SoC.- Dual Core ARM Cortex
Power usage ~133W. No power through PCIe.
Can be implemented as a stand alone device (no Server)

FELIX timelines

10 boards were produced in early 2023.

DAQ Working Group has recently acquired one of these boards for testing

General technical support for the FELIX Hardware should be available through the end of HL-LHC operation.
(i.e. into the late 2030s for Run 5)

Plan for 48-ch FELIX

- FPGA: Versal Premium, e.g. VP1552
- Transceivers: Up to 100+ GTYP/GTM
- PCIe Gen 5 up to 16 lanes
- If FPGA is available as planned, design will start in Q1 of 2023, first board is expected to be available in Q3 2023.

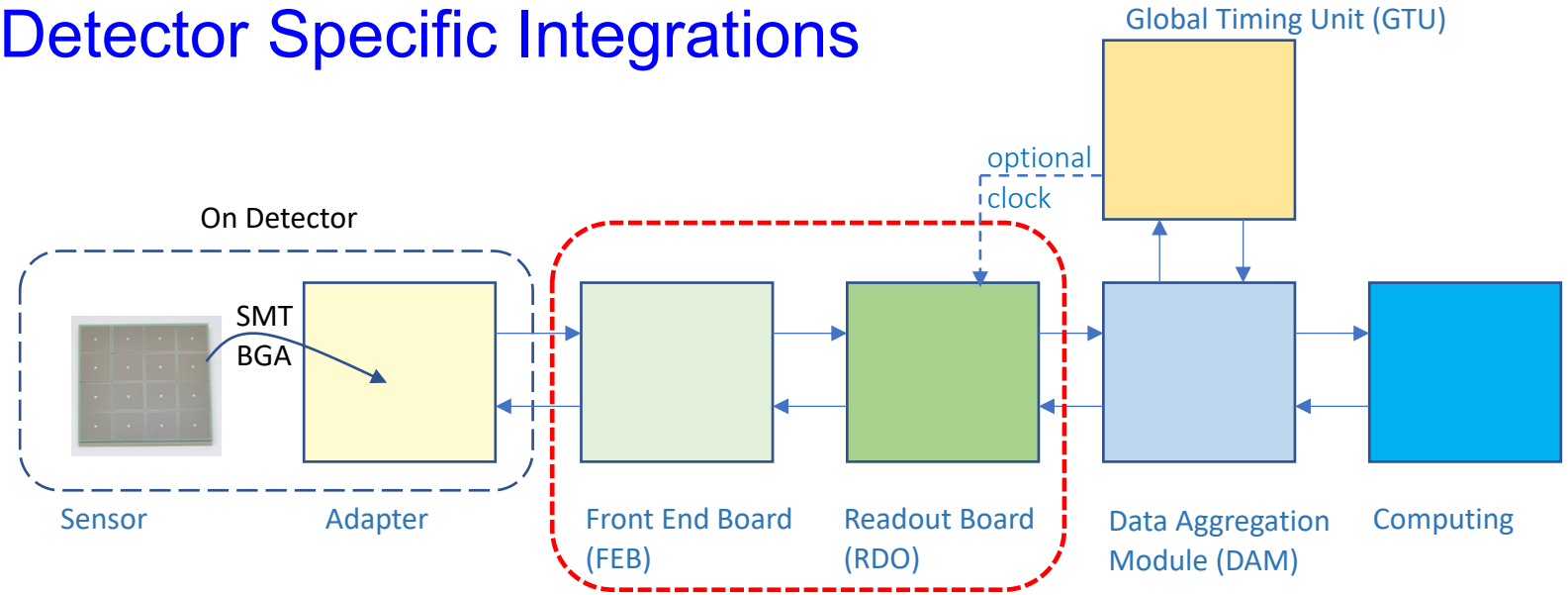
ePIC Detector Systems: Summary of Channel Counts

Detector Group	Channels					RDOs / Fibers	DAM	Data Volume Estimate (Gb/s)	Data Volume To Tape (Gb/s)
	MAPS	AC-LGAD	SiPM/PMT	MPGD	LAPPD				
Tracking	36B			100k		415	11	35	15
Calorimeters	88M*		150k			249	11	15	15
Far Forward	300M	2.3M	500			174	5	1	1
Far Backward		1.8M	700			117	4	100	2
PID		3M-50M	300k		150k	1117	49	1856	45
TOTAL	32B	7.1M-54M	450k	100k	150k	2072	80	2007	78

PID Specific Information

Detector System	Channels	Fiber pair	Data Volume	DAM Boards	Readout Technology	Notes
PID-TOF	3M-50M	240-500	6Gb/sec	12	AC-LGAD/ EICROC	Channel / Fiber counts depend on sensor geometry. Considering pitches of: .5mm x 1cm, .5mm x .3cm, .5mm x .5mm
PID-Cherenkov:						
dRICH	320k	312	1830Gb/s (<20Gbps to tape)	28	SiPM / ALCOR	Worse case after radiation. Includes 30% timing window. Requires further data volume reduction (software trigger, or AI/ML)
pfRICH	70k	17	15Gbps	1	LAPPD/HRPPD /EICROC	
hpDIRC	74k	288	11Gb/sec	6	LAPPD/HRPPD /EICROC	12 boxes x 24 sensor x 4 asic x 64 ch

PID Detector Specific Integrations

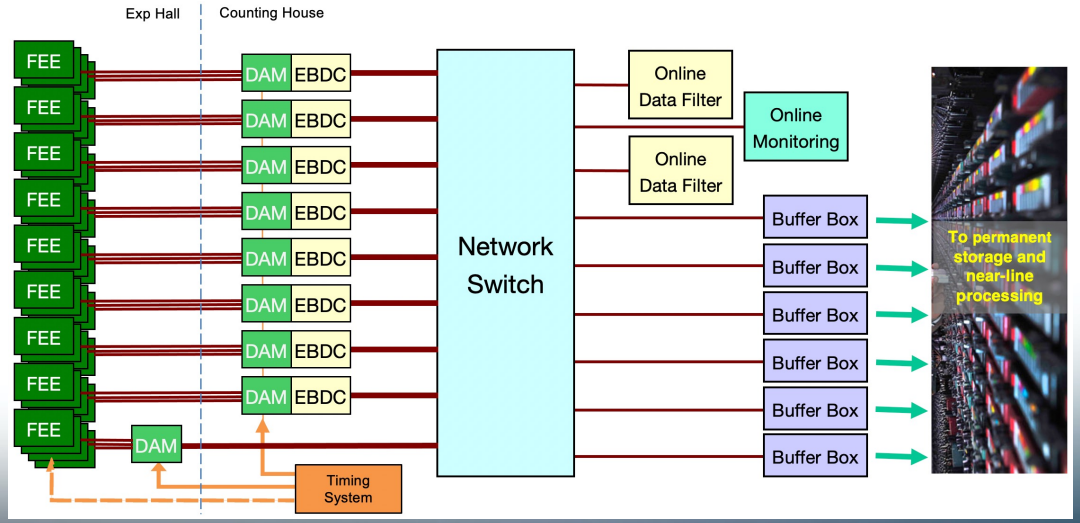


Detector	ASIC	RDO/Fiber	DAM	Data rate	Det. Tech
pfRICH	EICROC	17	1	15Gbs	LAPPD/HRPPD
dRICH	ALCOR	312	28	1800Gbs	SiPM
hpDIRC	EICROC	288	6	11Gbs	LAPPD/HRPPD
TOF (B) TOF (FEC)	EICROC	240-500	12	6Gbps	AC-LGAD

Scale of the Online Task

- EIC minimum bias collision rate ~500kHz
  - Expected real physics data from the detector < 100Gbps
- Background/Noise is the wild card.
  - Synchrotron radiation, Beam Gas, Detector/electronics noise
  - Try to keep below the level of the physics signal.
  - Online/DAQ processing will focus on Event ID and reducing the background

- Front-End (DAM Boards) - will support total bandwidth O(50Tbps)
  - 3000+ fibers(streams) off the detector (nominally 10Gbps links)
  - ~110 DAM Boards
- Online DAQ/Computing (over 100/400Gbps network)
  - ~200 nodes
  - GPU/FPGA processing options
  - Data Monitoring
  - Staged disk storage (Buffer Box)

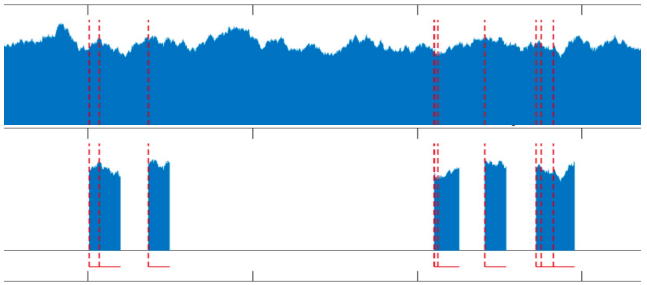


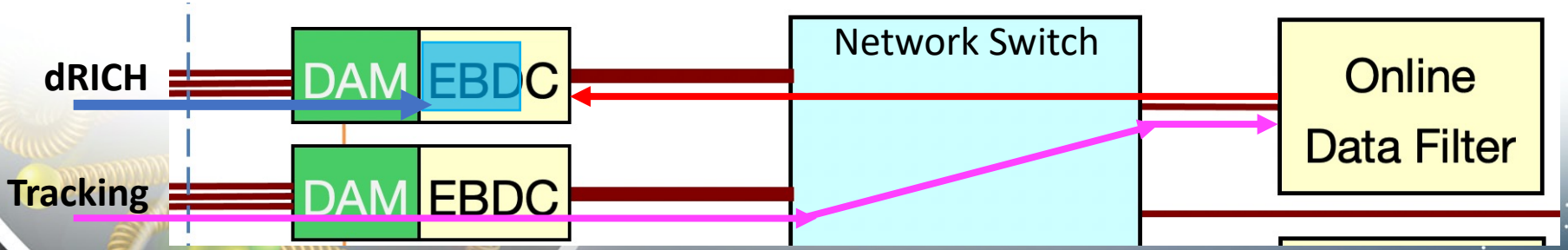
Potential “Hot spots”

- In general the high fiber counts coming to the DAM boards are not bandwidth driven, but the expected numbers of RDOs needed to instrument the ePIC detector can vary for different sub-systems.

- Detectors using SiPM readout at thresholds sensitive to single photons
  - Dark current rates will increase over time due to radiation damage.
  - E.g. dRICH could eventually generate **~1800Gbps data rates**

Example:
Use some EBDC (Event Building/DataCompression) servers as a RAM buffer until Event ID processing can identify time windows that are important. Then filter data from the high rate detector we should keep.

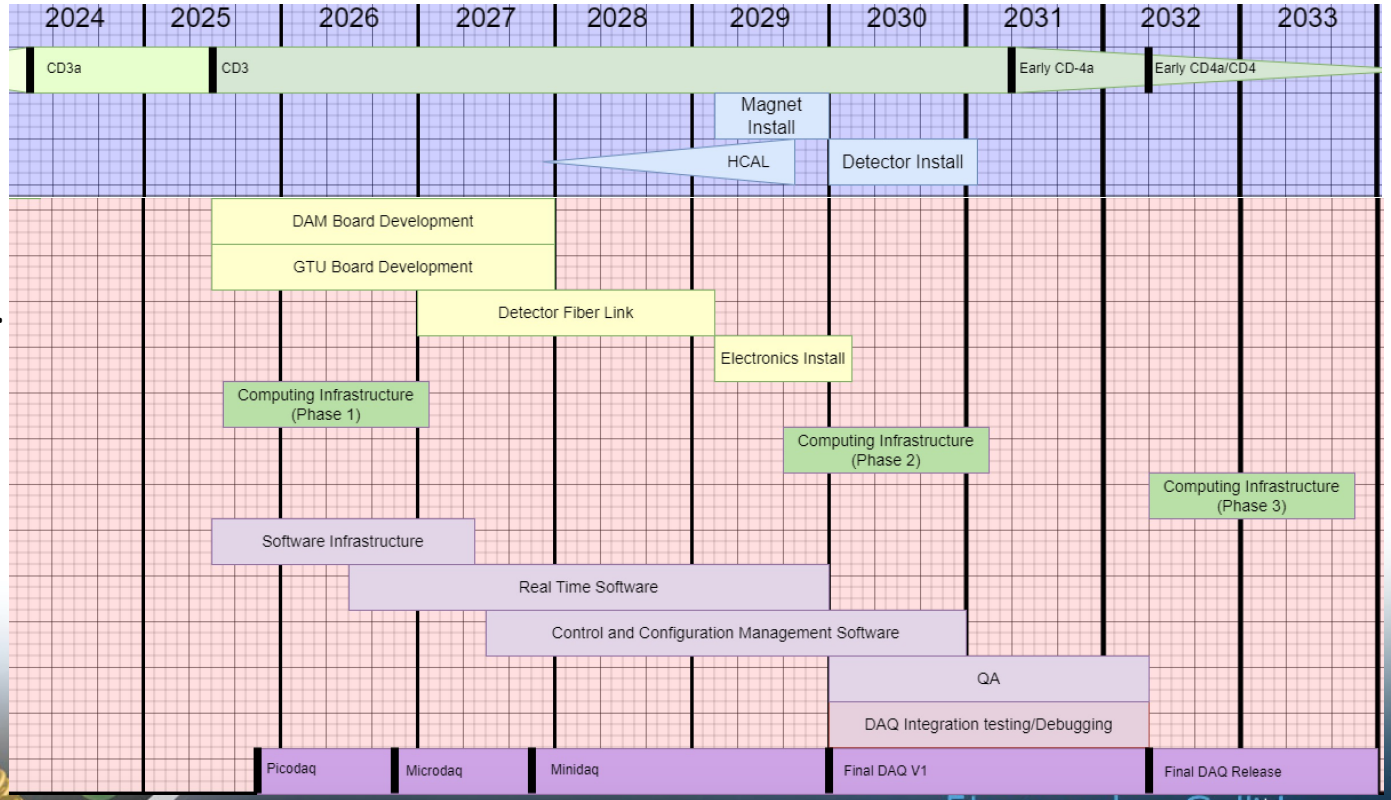




EIC DAQ/Computing schedule

- The DAQ and computing schedule is planned to be somewhat accelerated in relation to the full detector construction.
- A functional DAQ will be necessary for small scale detector testing as well as commissioning and pre-ops.
- Hardware and software development early in the construction phase will provide a streaming DAQ system (Minidaq) well before final detector installation begins.

- Final computing resources are purposely delayed to allow access to highest performing hardware available.

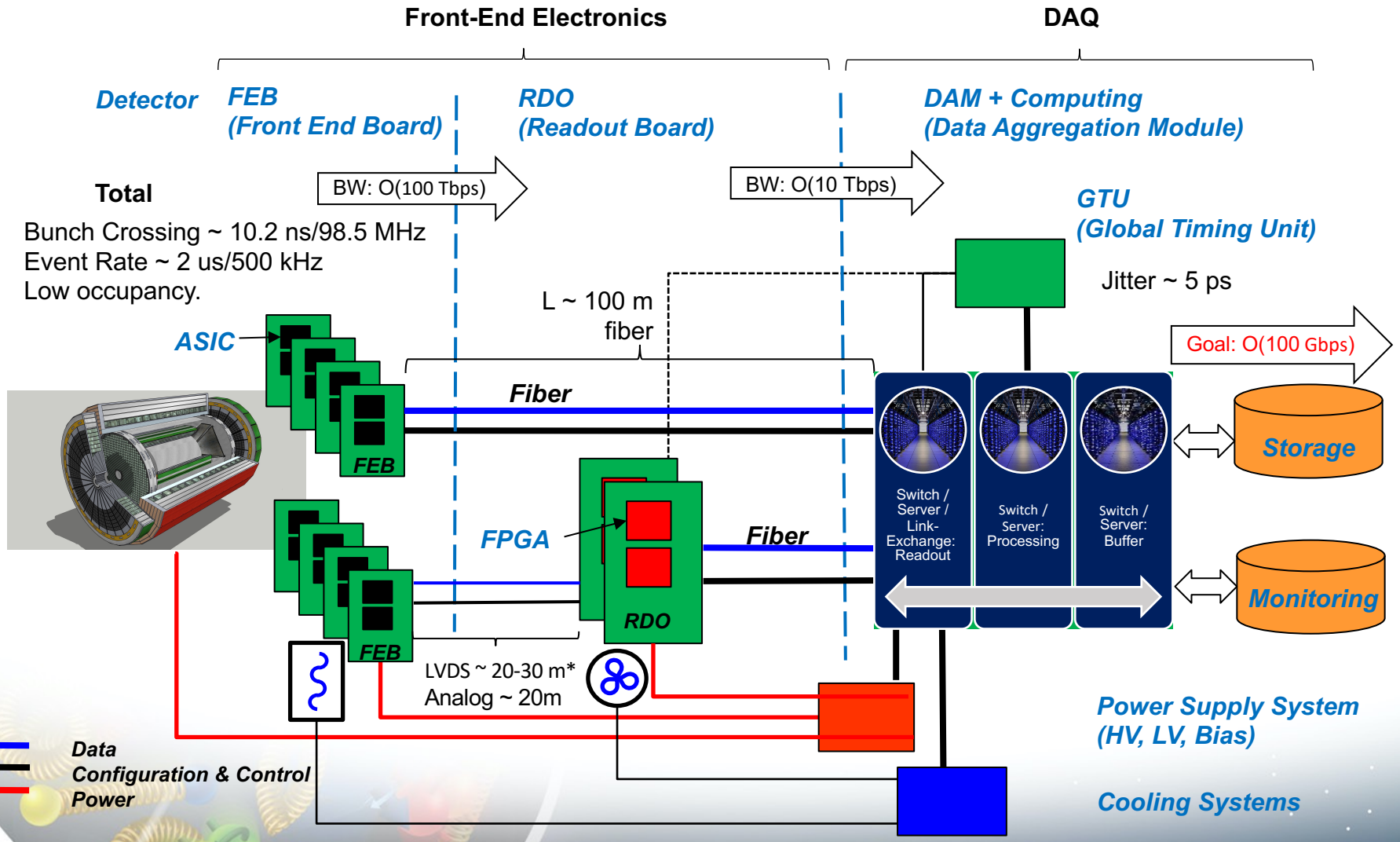


Summary

- A general picture of the scope, scale and technologies we expect to need for the EIC data acquisition and online computing reasonably clear at this stage.
- Most of the DAQ/Online will be COTS-based procurements
- We have a viable candidate for a Front-end interface and stream management hardware (FELIX)
- Integration plans and requirements for all the detector subsystems are currently being developed.

BACKUP

EIC Streaming Readout Architecture

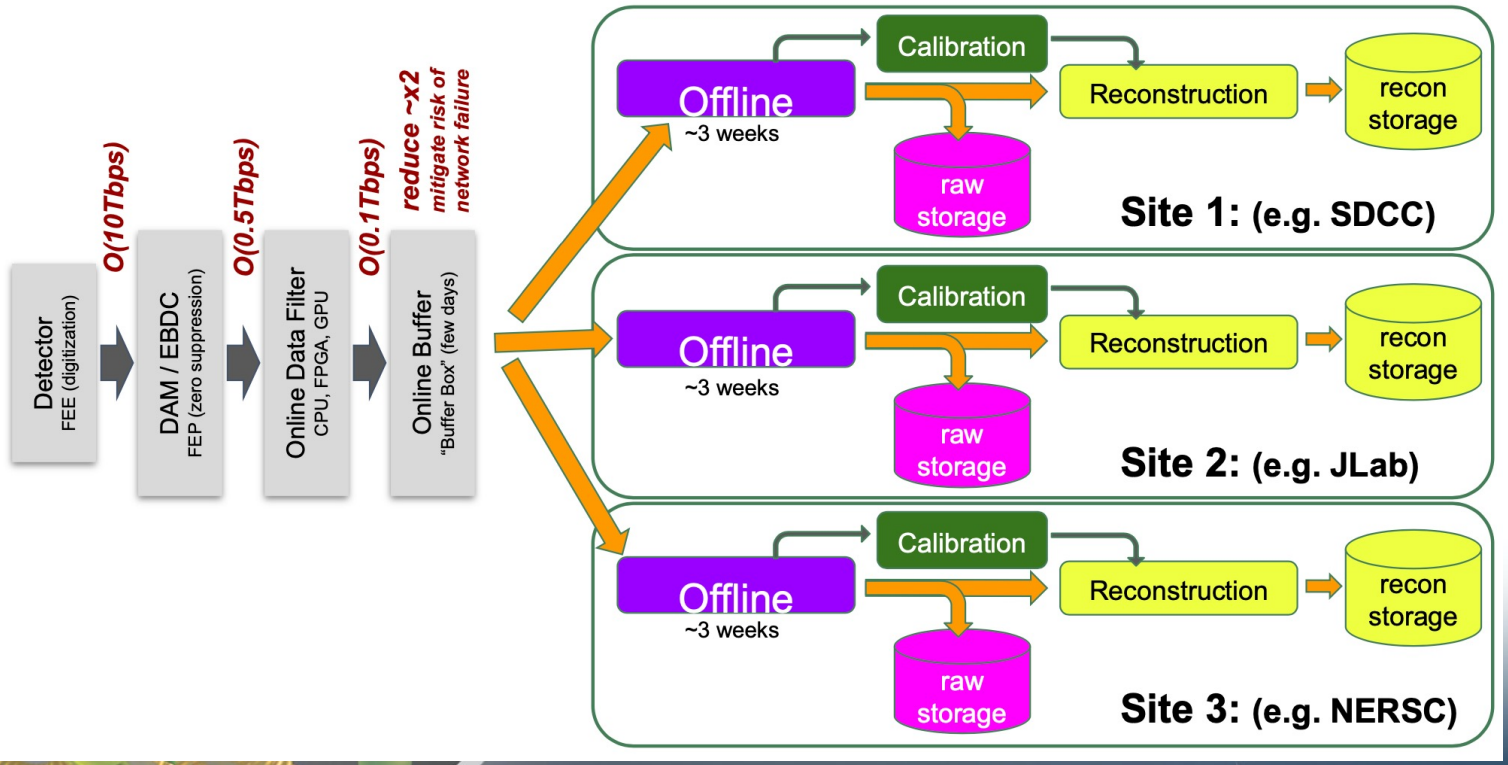


*LVDS – ANSI/TIA/EIA-644A standard. Maximum cable length dependent on data rate.

Boundary between Online and Offline

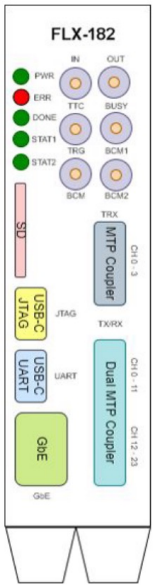
- Full understanding of the Online processing responsibilities and physical make-up is still being hashed out.
- We still require elements of the Offline Computing framework within the Online

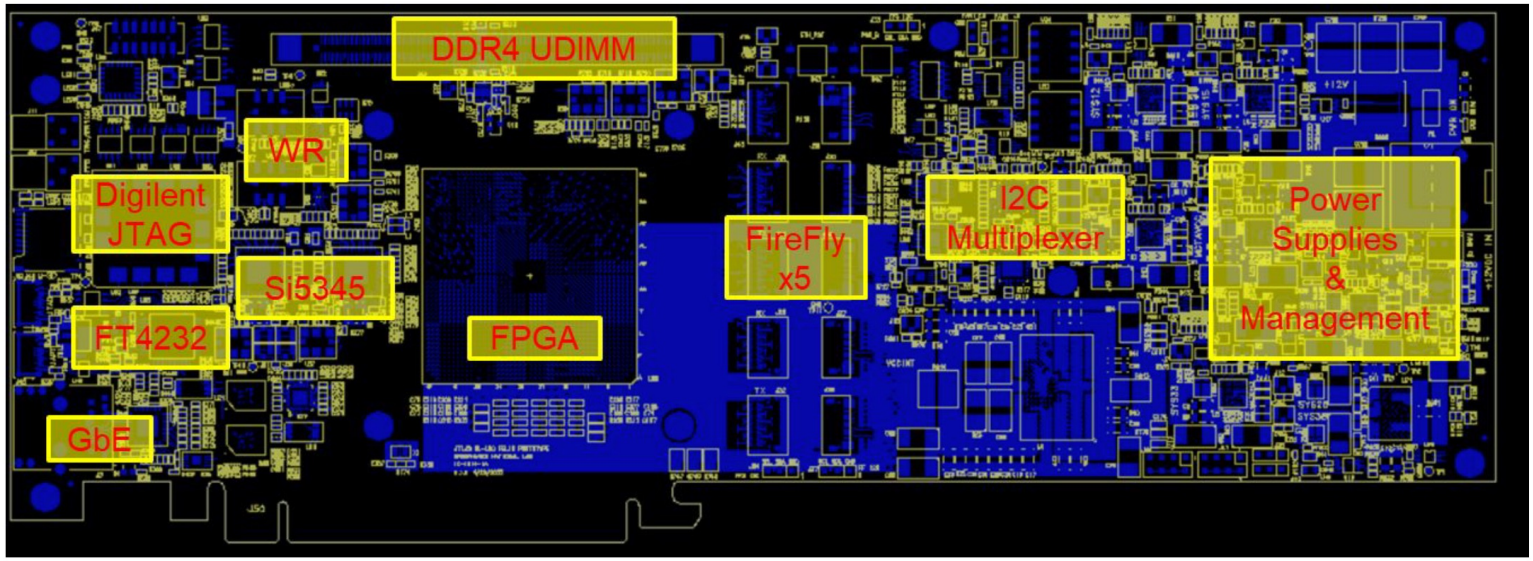
- Online Storage (Buffer Boxes) are intended as a “pause” and a decoupling with further Offline processing .
- Offline buffering will allow several weeks for calibration and reconstruction.



Slow Control Integration

- There will be many slow control and monitoring systems associated with the EIC collider and ePIC detector subsystems.
  - BPMs, magnets, detector biases, HV, gas flows, temps, pressures, etc…
- Design and implementation of these control systems driven primarily by the relevant subsystems.
  - We want to coordinate ePIC slow control as much as possible with the collider approach (still not finalized) – some SCADA type system.
  - sPHENIX currently supports Ignition and WinCC using UPC-UA.
- DAQ/Computing has defined responsibility for SC Integration (L4 WBS 6.10.09.2)
  - Databases for maintaining SC data for calibrations and online/offline processing
  - Manage SC data readout to synchronize with the physics stream data
  - Maintain Software tools and libraries
- Also included is the development and implementation of a general network infrastructure in the experimental hall and counting house to support slow controls and other ancillary systems.


FLX-182
IN
OUT
PWR
ERR
DONE
STAT1
STAT2
TTC
BUSY
TRG
BCM1
BCM
BCM2
SD
TRX
MTP Coupler
CH 0 - 3
USB-C JTAG
JTAG
TX/RX
USB-C UART
UART
Dual MTP Coupler
CH 0 - 11
CH 12 - 23
GbE
GbE


DDR4 UDIMM
WR
Digilent JTAG
Si5345
FT4232
FPGA
GbE
FireFly x5
I2C Multiplexer
Power Supplies & Management