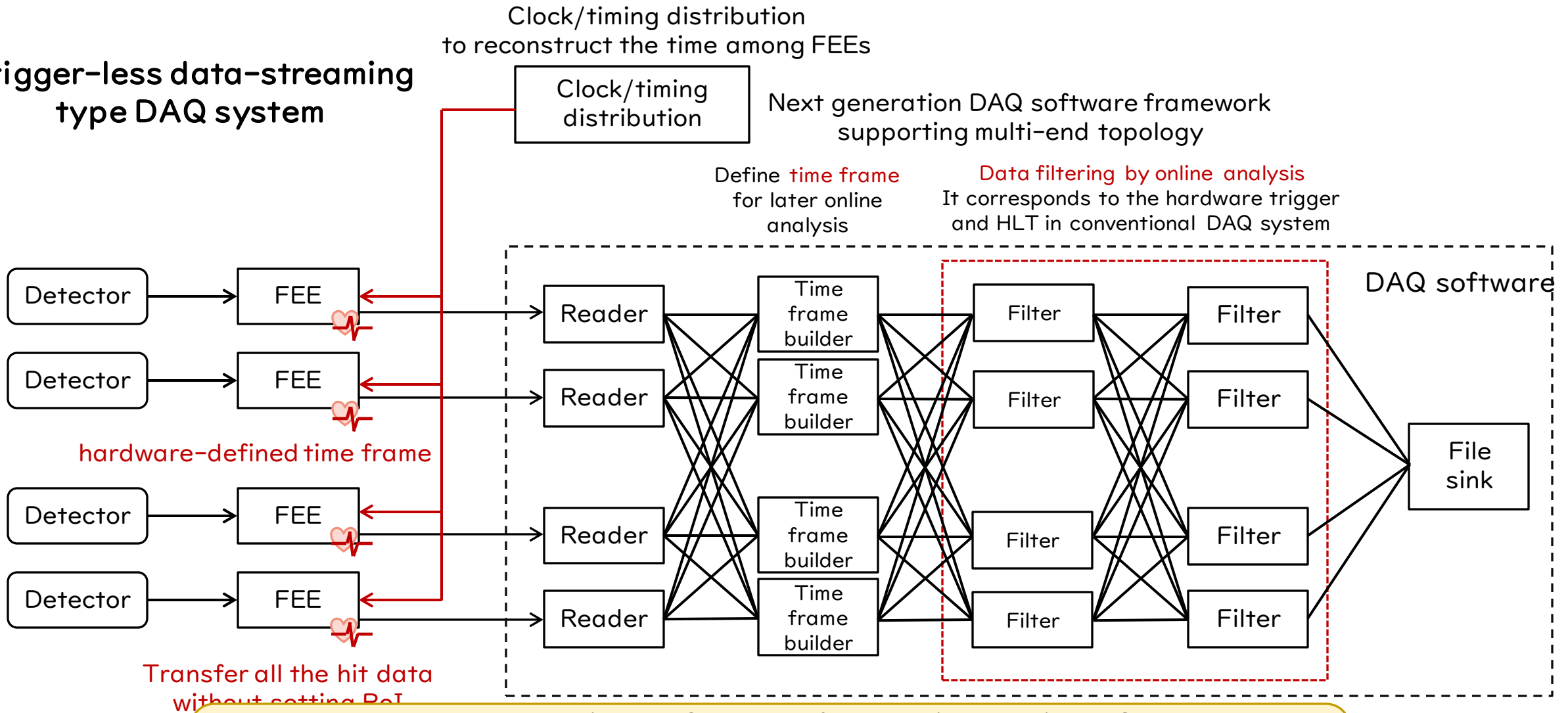# SRO FEE development in Japan

Outline

- Key technologies for trigger-less DAQ system
- Implementation to front-end electronics
- Beam test in RCNP and J-PARC
- Future prospect
- Summary

KEK IPNS
Ryotaro Honda

Toward trigger-less data-streaming DAQ system

Trigger-less data-streaming type DAQ system

Clock/timing distribution to reconstruct the time among FEEs

Clock/timing distribution

Next generation DAQ software framework supporting multi-end topology

Define time frame for later online analysis

Data filtering by online analysis
It corresponds to the hardware trigger and HLT in conventional DAQ system

DAQ software

| Detector | → | FEE |
| Detector | → | FEE |

hardware-defined time frame

| Detector | → | FEE |
| Detector | → | FEE |

Transfer all the hit data without setting RoI

Reader — Time frame builder — Filter — Filter

Reader — Time frame builder — Filter — Filter

Reader — Time frame builder — Filter — Filter

Reader — Time frame builder — Filter — Filter

File sink

Is the streaming DAQ system for the big experiment?
We think NO. There is merit even for small experiments!

We aim to develop a general purpose trigger-less DAQ

Development policy

Scalability
- Should be scalable from single FEE node (stand-alone) to a few thousands FEE nodes.
  - Mbps – Tbps
- Not only for actual physics experiments but also for small setup, e.g., test bench.

Simple to use and maintain
- Usable for a small experiment not having the DAQ team inside.

Standardization
- We would like to promote standardization of developed items under SPADI-alliance
- A DAQ system for many experiments

Ota's talk
in next session

SPADI
Alliance

Define the time frame

From taking a picture to recording a video

Trigger

⇩

Trigger-less

| Event | Event | Event | Event | Event |
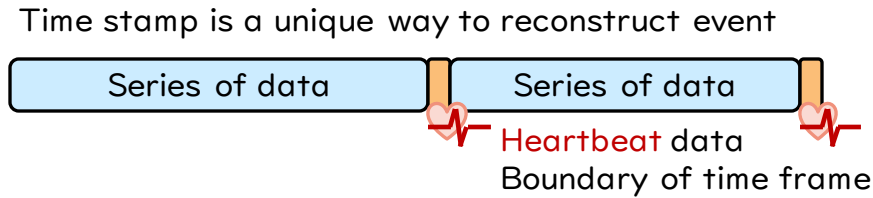
Time stamp is a unique way to reconstruct event

| Series of data | Series of data |

Heartbeat data
Boundary of time frame

Synchronization

Simple & light-weight clock-data-recovery
Frequency synchronization
(MIKUMARI: 水分, R. Honda, IEEE TNS, 70 (6), 1102 (2023).

TDC — FEE

TDC — FEE

MIKUMARI
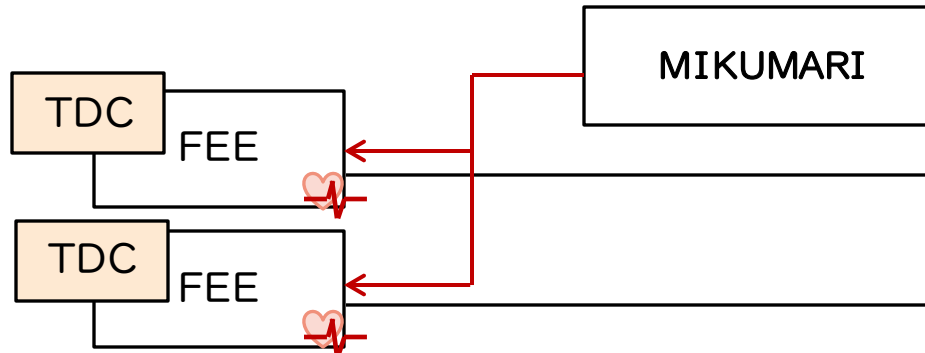
We started from streaming type TDC
since it can be realized only in FPGA.
It is simple.

Nest generation DAQ software (NestDAQ)

Support multi-end topology for load balancing

DAQ software

Reader — Time frame builder — Filter
Reader — Time frame builder — Filter
Reader — Time frame builder — Filter
Reader — Time frame builder — Filter
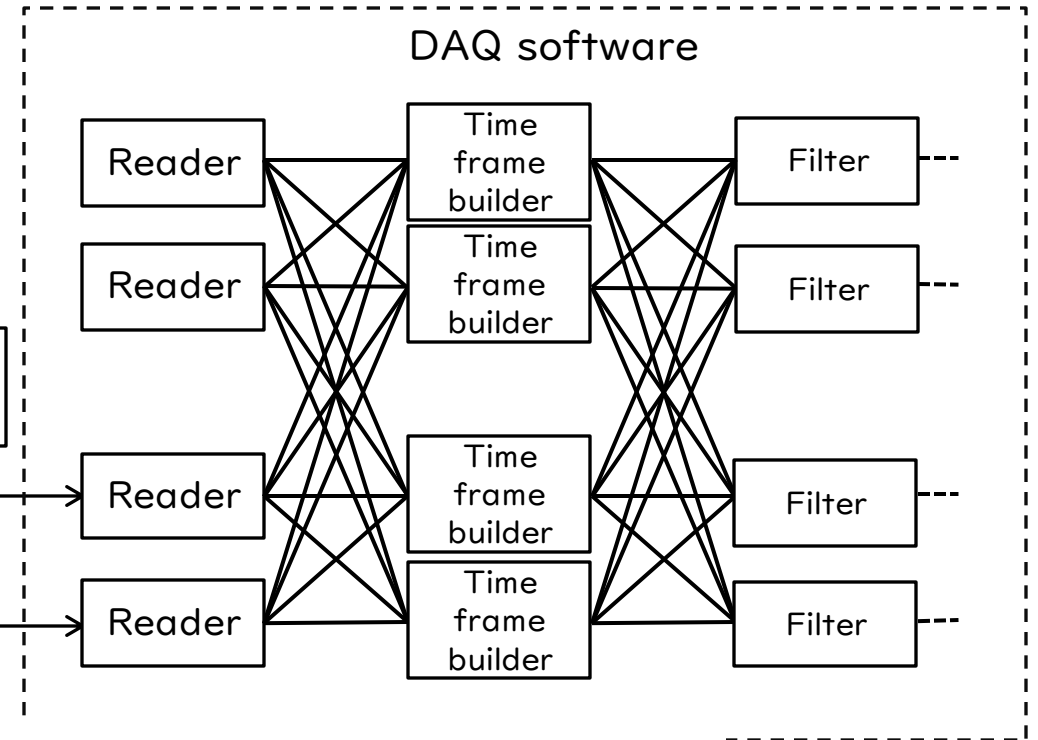
Fast data transmission
- FPGA technology (10Gbps TCP/IP by SiTCP-XG)
  - https://www.bbtech.co.jp/products/sitcp-xg-license/

4

Tapped-delay-line based FPGA TDC

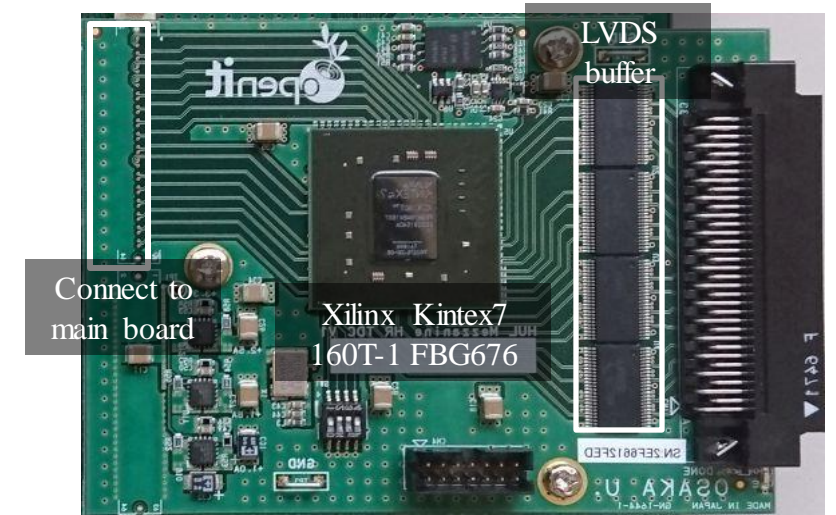**Timing interpolation technique using tapped-delay-line (TDL)**
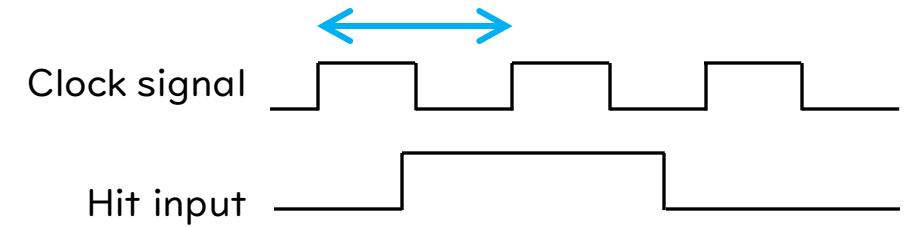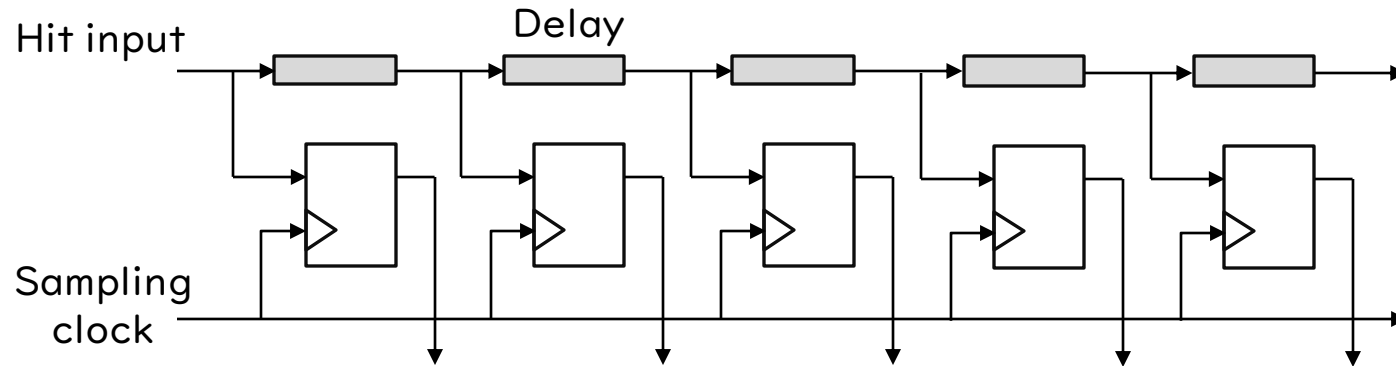
Take a snap shot of a pulse running on TDL
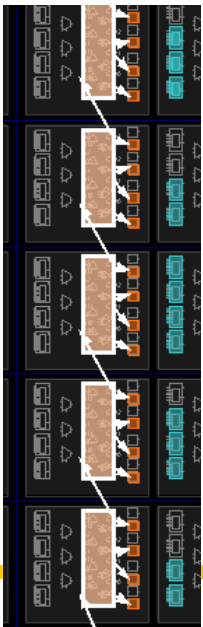
TDC implemented in AMD Kintex-7 FPGA
- Use CARRY4 element
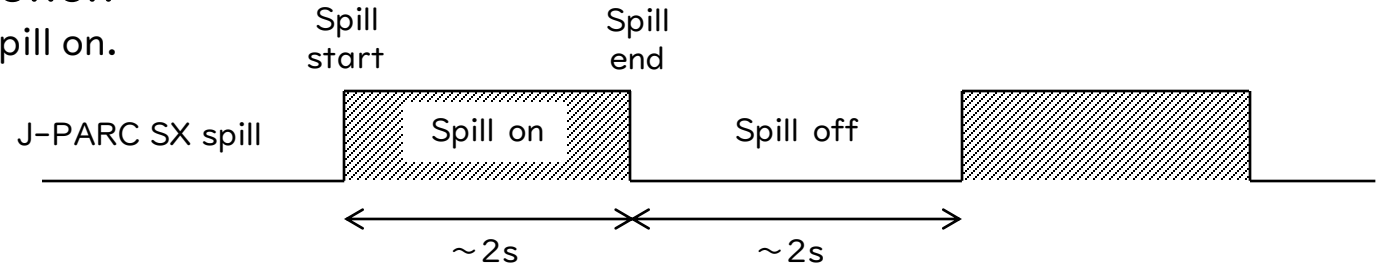- 192 taps corresponding to the vertical size of a clock region.

Timing resolution: 15 ps (σ)

Consider the case for J-PARC slow extraction

- DC beam are delivered to the beamline during spill on.

Spill
start

Spill
end

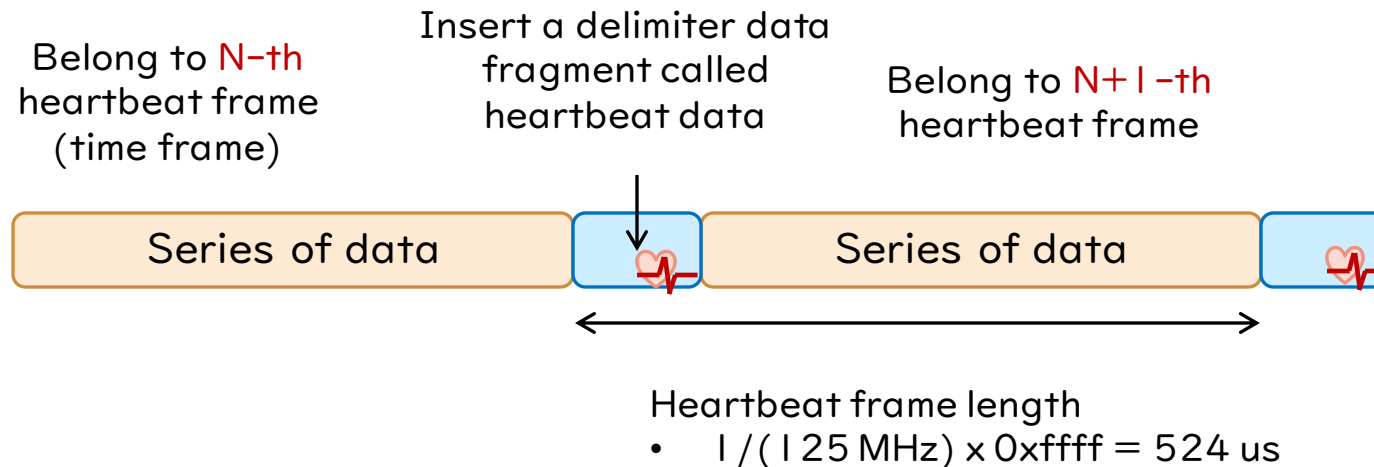J-PARC SX spill   Spill on   Spill off

~2s   ~2s

We need the continuous timing measurement over 2 s (spill duration of J-PARC slow extraction)
- Required dynamic range: $\sim 10^{10}$ (1 ns TDC case)

Introduce **heartbeat method**: a technique to reconstruct the time without a long-length time stamp.
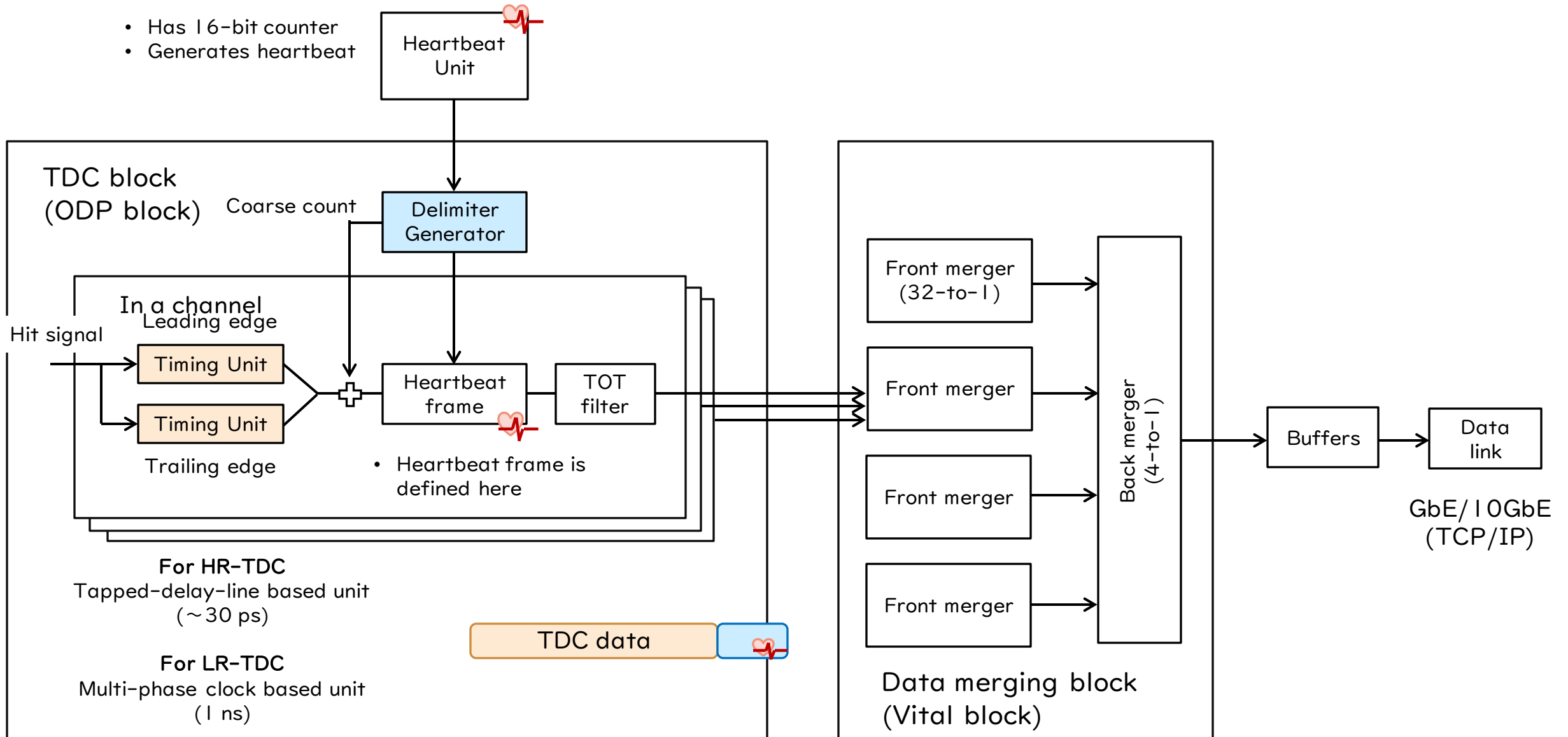- Insert a special data word periodically
- 16-bit heartbeat counter generates this period ⇔ 16-bit coarse count

Belong to N-th
heartbeat frame
(time frame)

Insert a delimiter data
fragment called
heartbeat data

Belong to N+1-th
heartbeat frame

Series of data   Series of data

R. Honda et al., PTEP, ptab128,
https://doi.org/10.1093/ptep/ptab128

Heartbeat frame length
- $1/(125\,\text{MHz}) \times 0\text{xffff} = 524\ us$

Simplified block diagram of Str-TDC

- Has 16-bit counter
- Generates heartbeat

Heartbeat Unit

TDC block (ODP block)

Coarse count

Delimiter Generator

In a channel

Leading edge

Hit signal

Timing Unit

Timing Unit

Trailing edge

Heartbeat frame

TOT filter

- Heartbeat frame is defined here

For HR-TDC
Tapped-delay-line based unit
(~30 ps)

For LR-TDC
Multi-phase clock based unit
(1 ns)

TDC data

Front merger (32-to-1)

Front merger

Front merger

Front merger

Back merger (4-to-1)

Buffers

Data link

GbE/10GbE (TCP/IP)

Data merging block (Vital block)

MIKUMARI link

Clock/data distribution system based on the modulated clock signal (CDCM) using a single transmission line
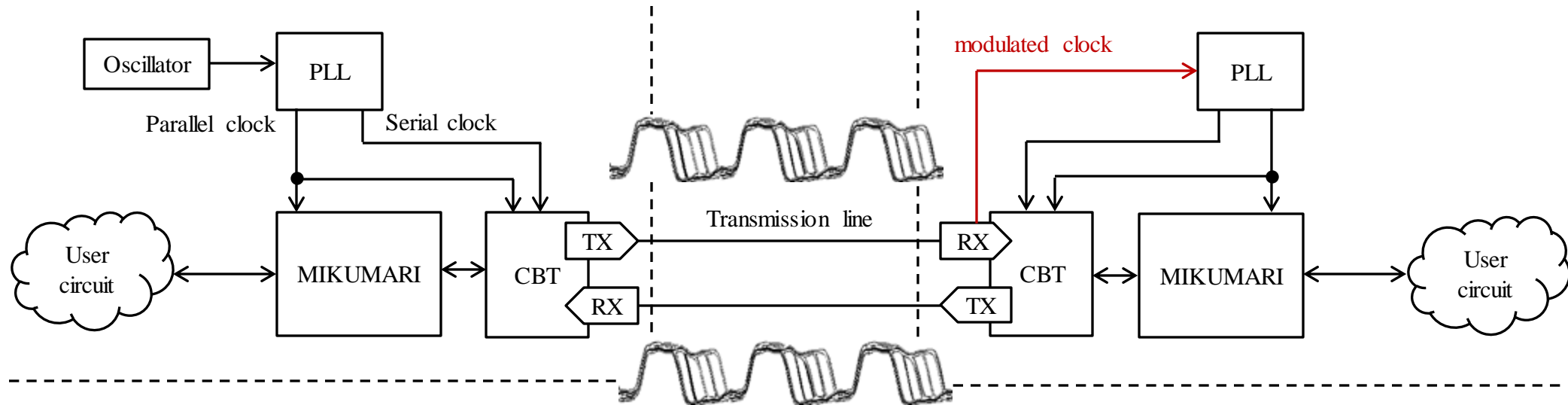
Functions
- Frequency synchronization by transmitting a modulated clock signal
- Data communication based on a data frame
- Pulse transmission with the fixed latency

Features
- It can be implemented in a regular bank. It's independent from high-speed serial transceivers such as MGT in AMD FPGAs.
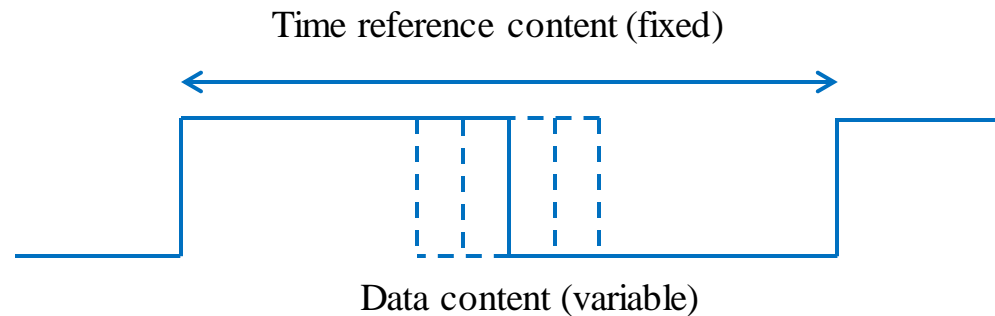- Any PLL is workable as the clock recovery circuit.

Adopting clock-duty-cycle-modulation (CDCM) as a core technology

- CDCM is a clock-centric type modulation.
- Data bits are embedded to the trailing edges of the clock signal.

Time reference content (fixed)
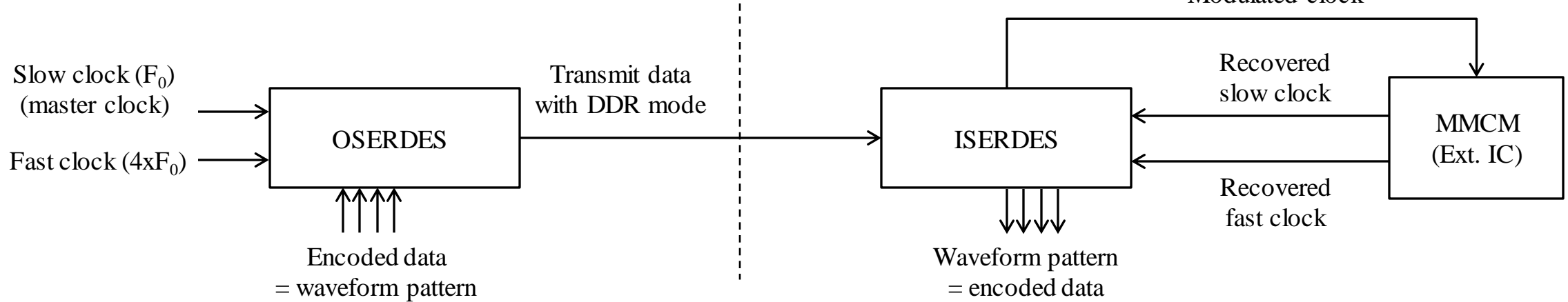
Data content (variable)

Denis Calvet,
IEEE TNS (Volume: 67, No. 8, Aug. 2020)

- Modulated clock can be directly input to PLLs. Every PLL will be a clock recovery circuit.
- When using PLL having a zero-delay mode for clock recovery, output clock skews respect to the input modulated clock are automatically adjusted.
  - No phase uncertainty. (It exits in a CDR circuit due to clock frequency division.)

CDCM by IOSERDES of Xilinx FPGA

Modulation and demodulation by IOSERDES

Modulated clock

Slow clock (F_0)
(master clock)

Fast clock ($4xF_0$)

Transmit data
with DDR mode

OSERDES

ISERDES

Recovered
slow clock

Recovered
fast clock

MMCM
(Ext. IC)

Encoded data
= waveform pattern

Waveform pattern
= encoded data

Waveform pattern

Payload

Duty cycle are
changed
in **37.5-62.5%**

$1/F_0$
Divided to 8-segments
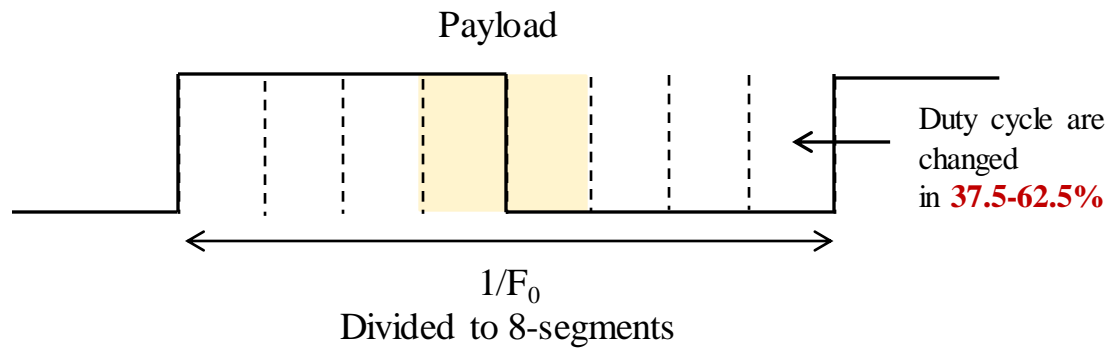
CDCM-8-1.5

*0.5 means idle pattern
Naming rule is defined in Ref. [1]

Present MIKUMARI supports
CDCM-8-1.5, CDCM-10-1.5, and CDCM-10-2.5.

[1]. D. Calvet, IEEE TNS, 67(8), 1912 (2020)
[2]. R. Honda, IEEE TNS, 70 (6), 1102 (2023)
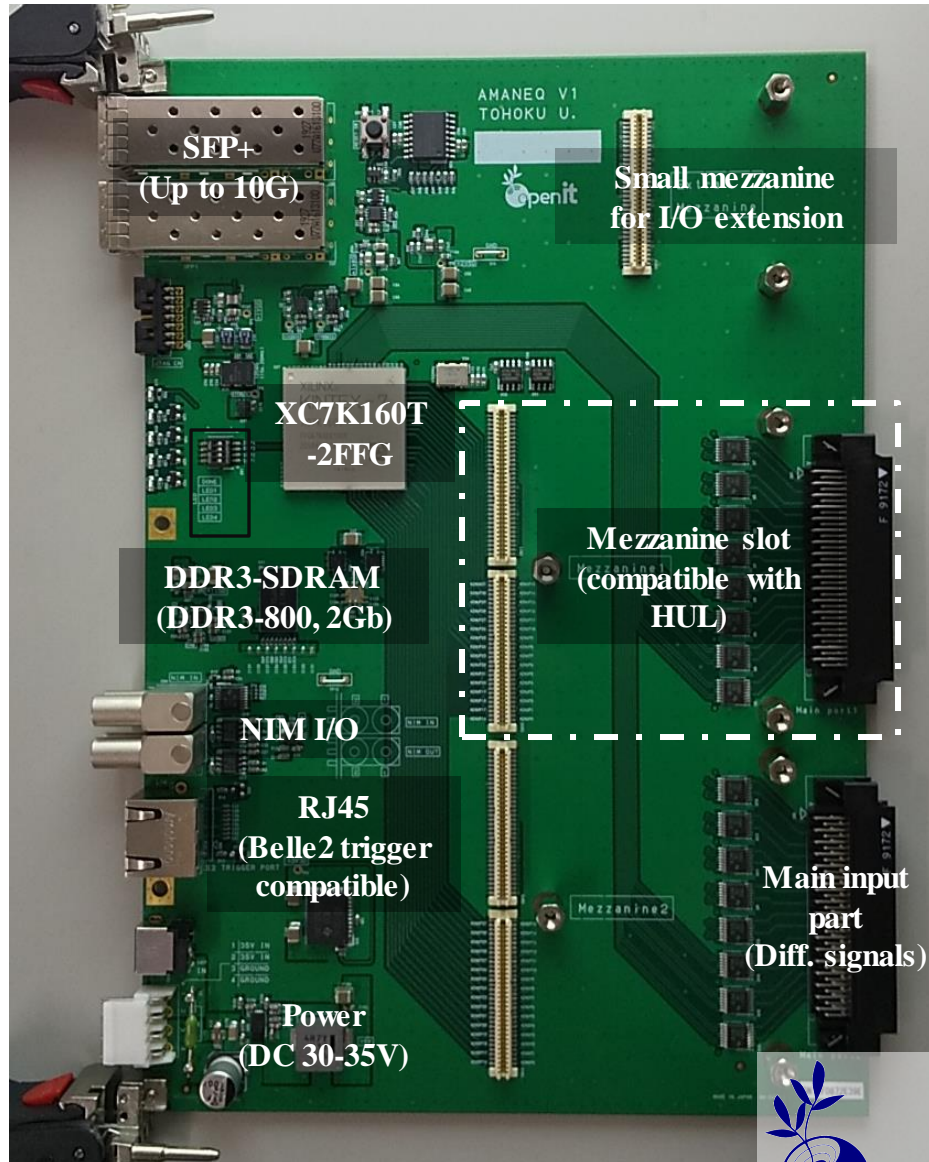
Simplified block diagram of Str-TDC
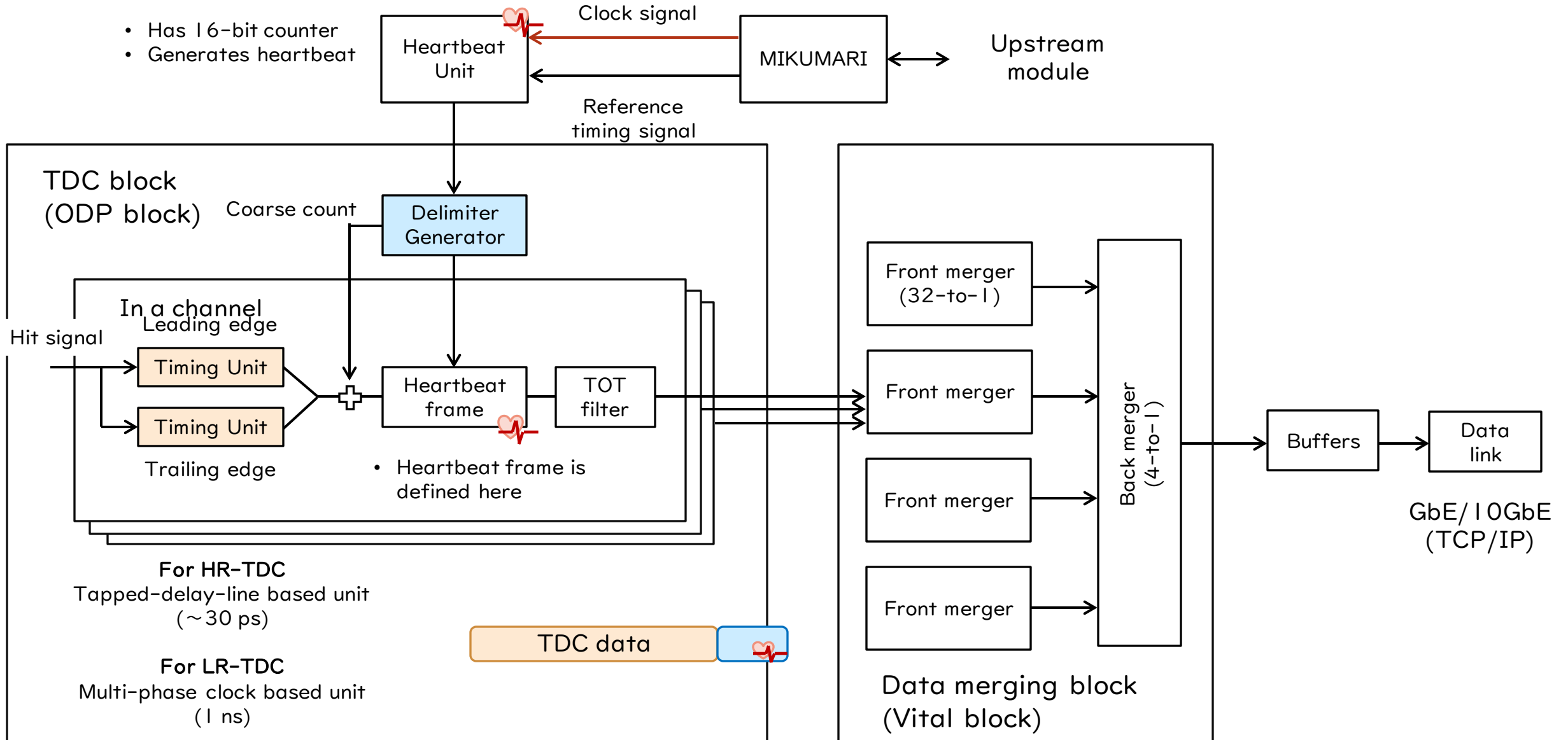
# Implementation to electronics

Hardware

A main electronics for
network oriented trigger-less data acquisition system
(AMANEQ)

- Kintex7 with speed grade -2
  - Transceiver bandwidth up to 10Gbps
  - Can implement SiTCP-XG
- Has two mezzanine slot
  - Mount HUL mezzanine HR-TDC
  - Mount DCR mezzanine for DC readout
- Has a jitter cleaner (CDCE62002)
- DDR3-SDRAM as a de-randomizer
  - DDR3-1333 with 16-bit bus width.
  - 2 Gb
- Powered by the external power supply with DC 30-35V

Hardware for streaming high-resolution TDC
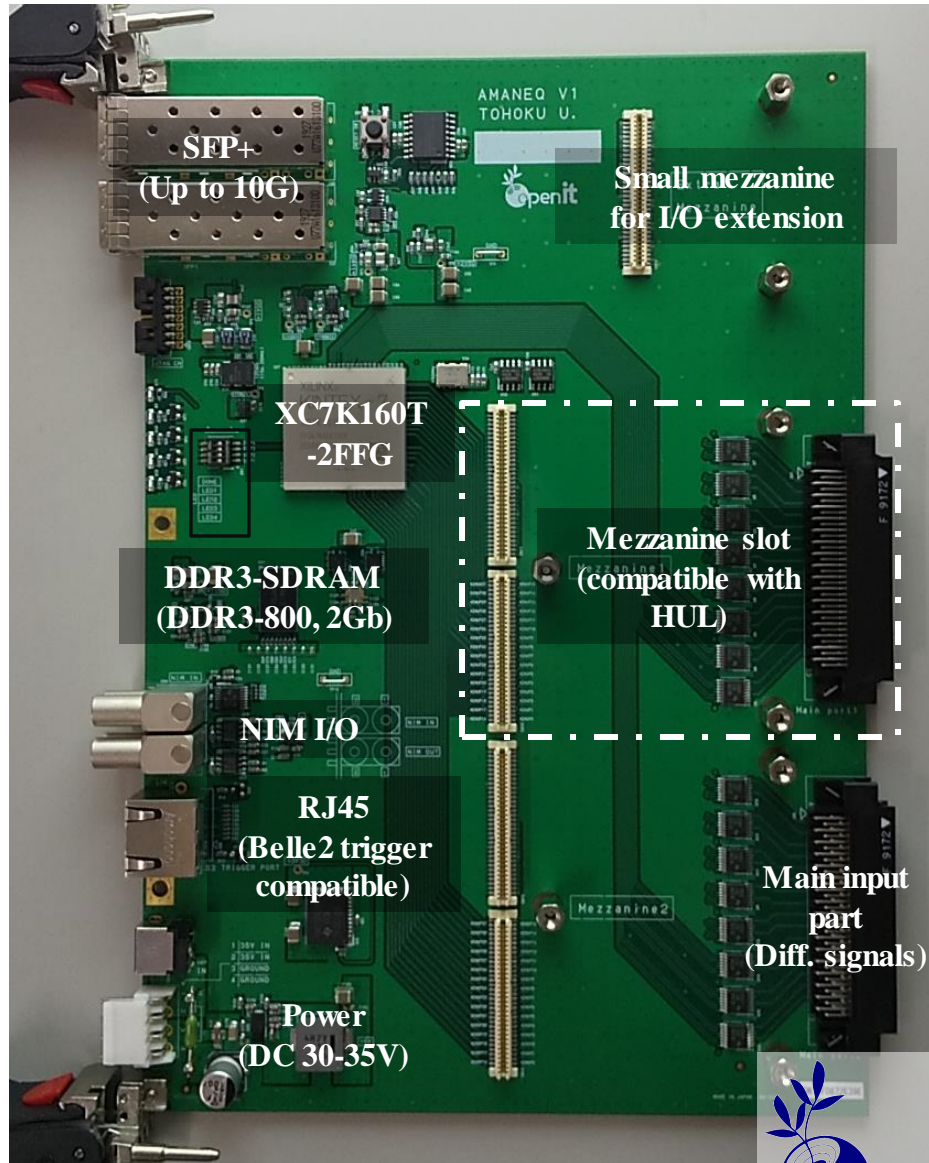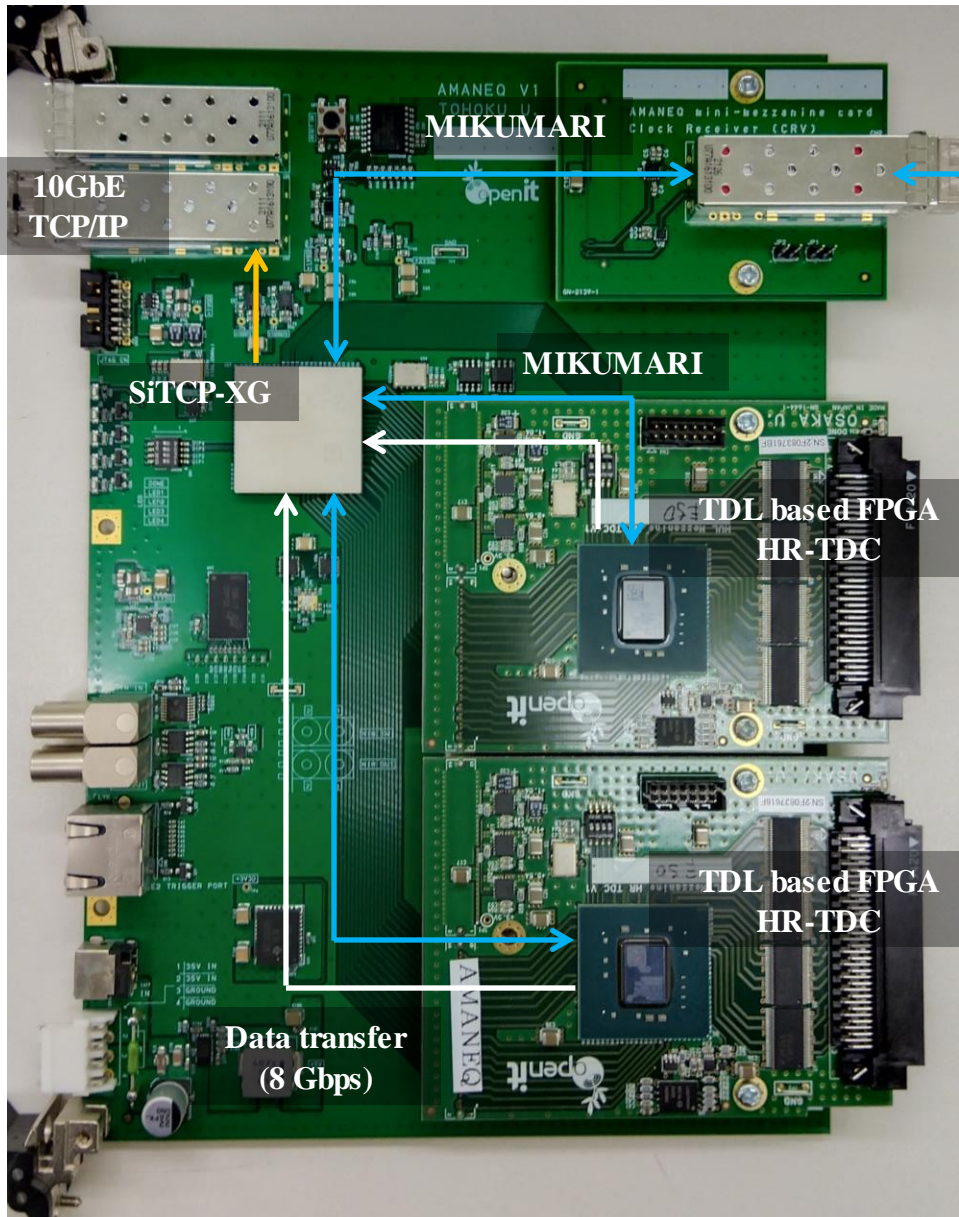

HUL/AMANEQ mezzanine HR-TDC

Attach

32 ch tapped-delay-line (TDL) based HR-TDC
- Input IO std.: LVDS (ECL is not supported)
- TDL consists of a CARRY4 primitive chain.
- Both leading/trailing edges
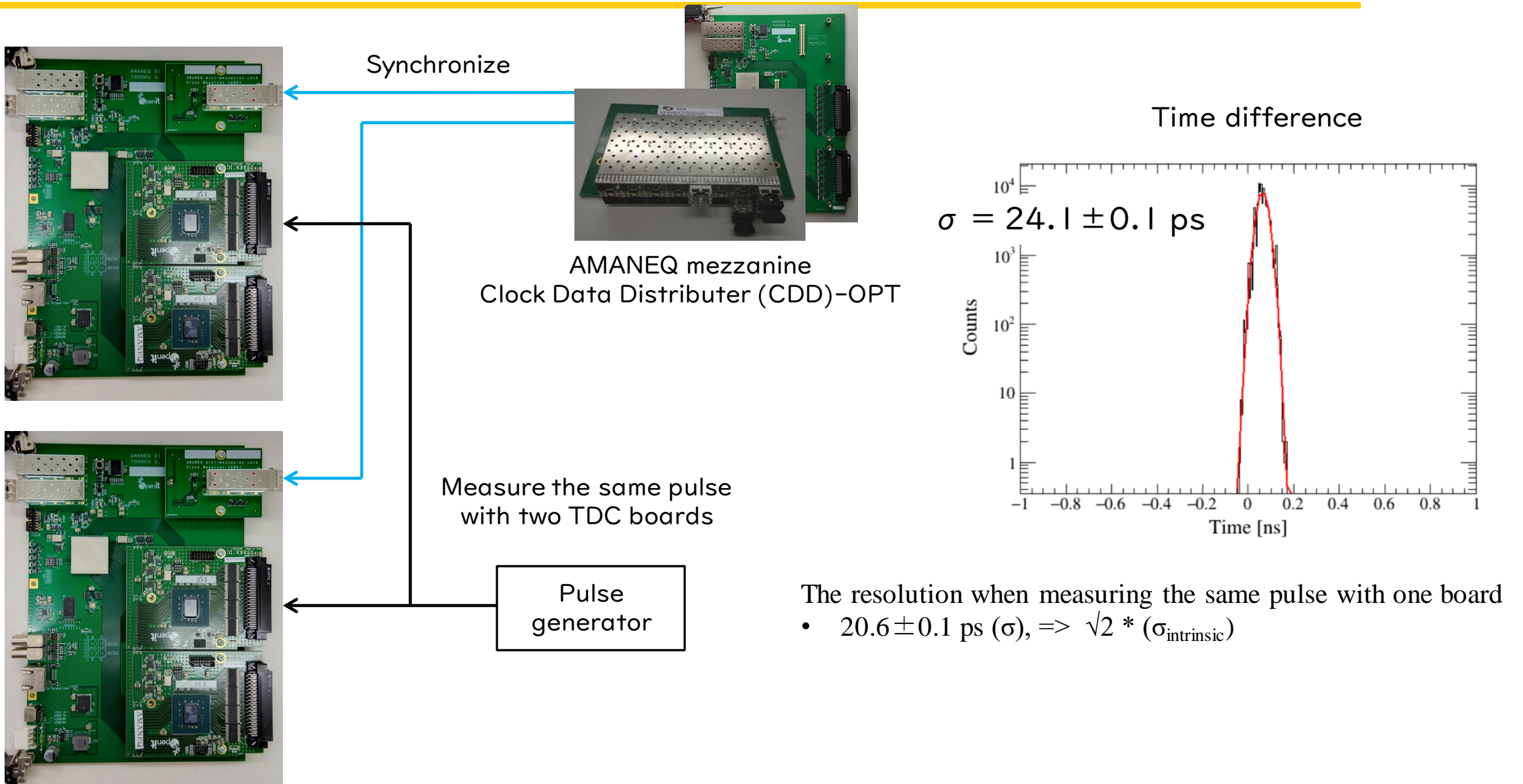- Intrinsic resolution: 15 ps (σ)

Streaming HR-TDC on AMANEQ

Modulated clock
from upstream (distributer) module

AMANEQ Str-HRTDC
- Input : 64 ch (32+32)
- Timing resolution: ~25 ps (σ)
  - Synchronization precision of MIKUMARI is included
- Data link: 10GbE
  - TCP/IP provided by SiTCP-XG
- Operation mode
  - Stand alone mode
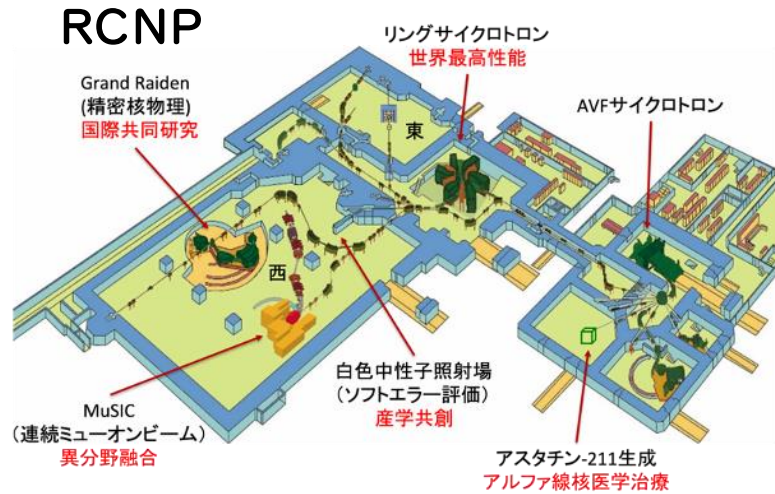 - Sync with MIKUMARI system

HR-TDC timing resolution

Synchronize

AMANEQ mezzanine
Clock Data Distributer (CDD)-OPT

Measure the same pulse
with two TDC boards

Pulse
generator

Time difference

$\sigma = 24.1 \pm 0.1$ ps

The resolution when measuring the same pulse with one board
- 20.6 ± 0.1 ps (σ), => $\sqrt{2} * (\sigma_{intrinsic})$

Use case for
beam experiments

Tested in RCNP and J-PARC
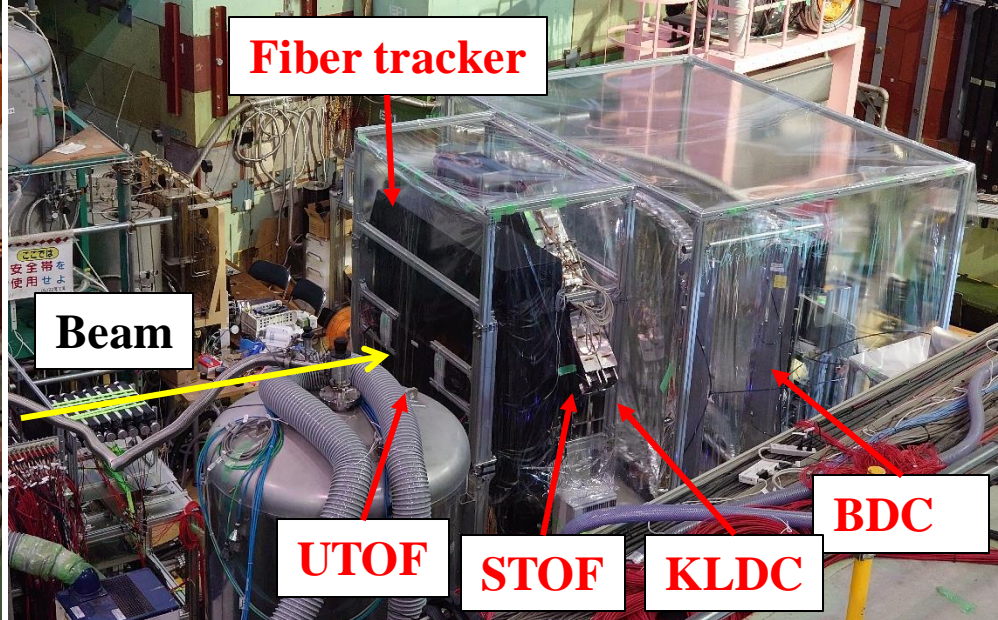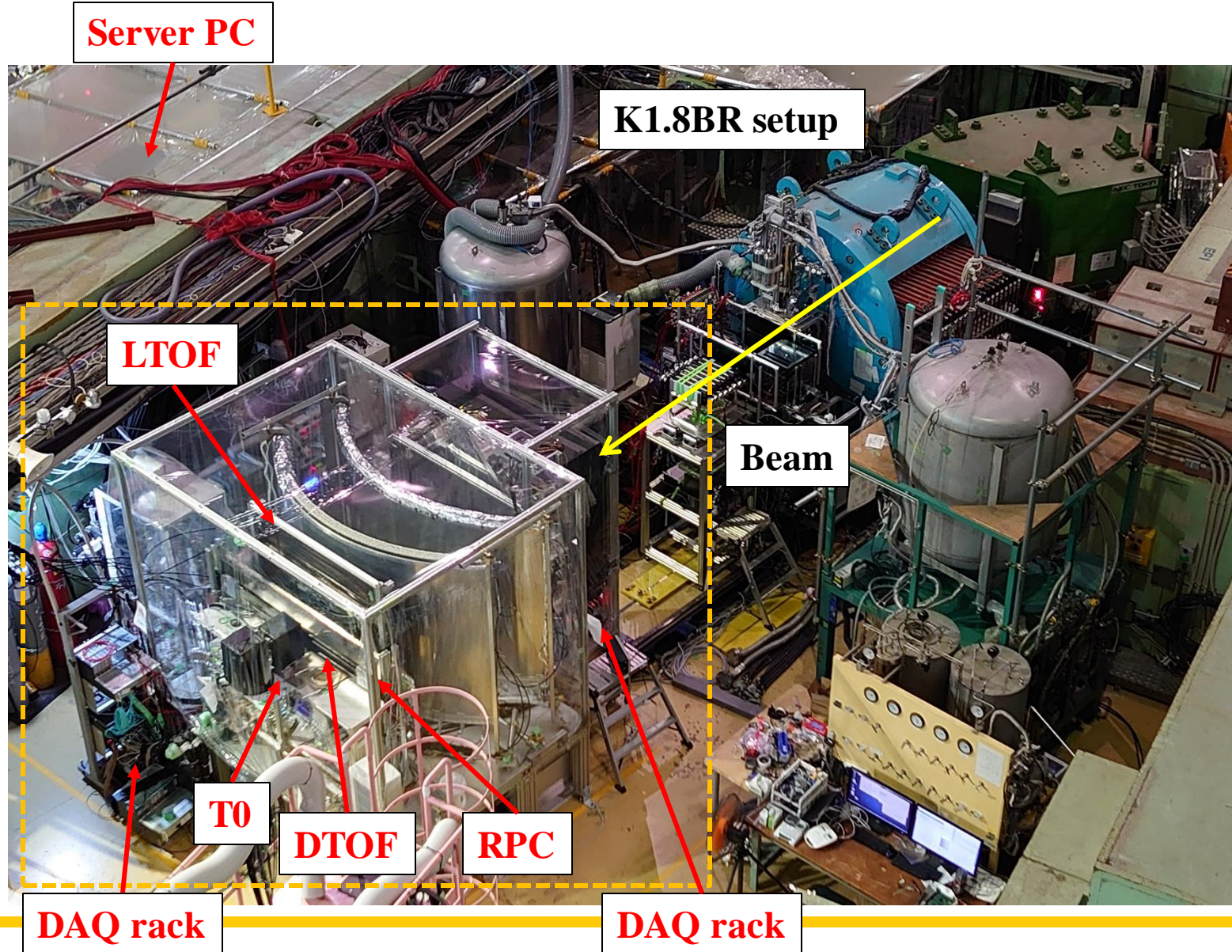
RCNP

Tested at RCNP Grand Raiden
- Cyclotron
  - Primary beams
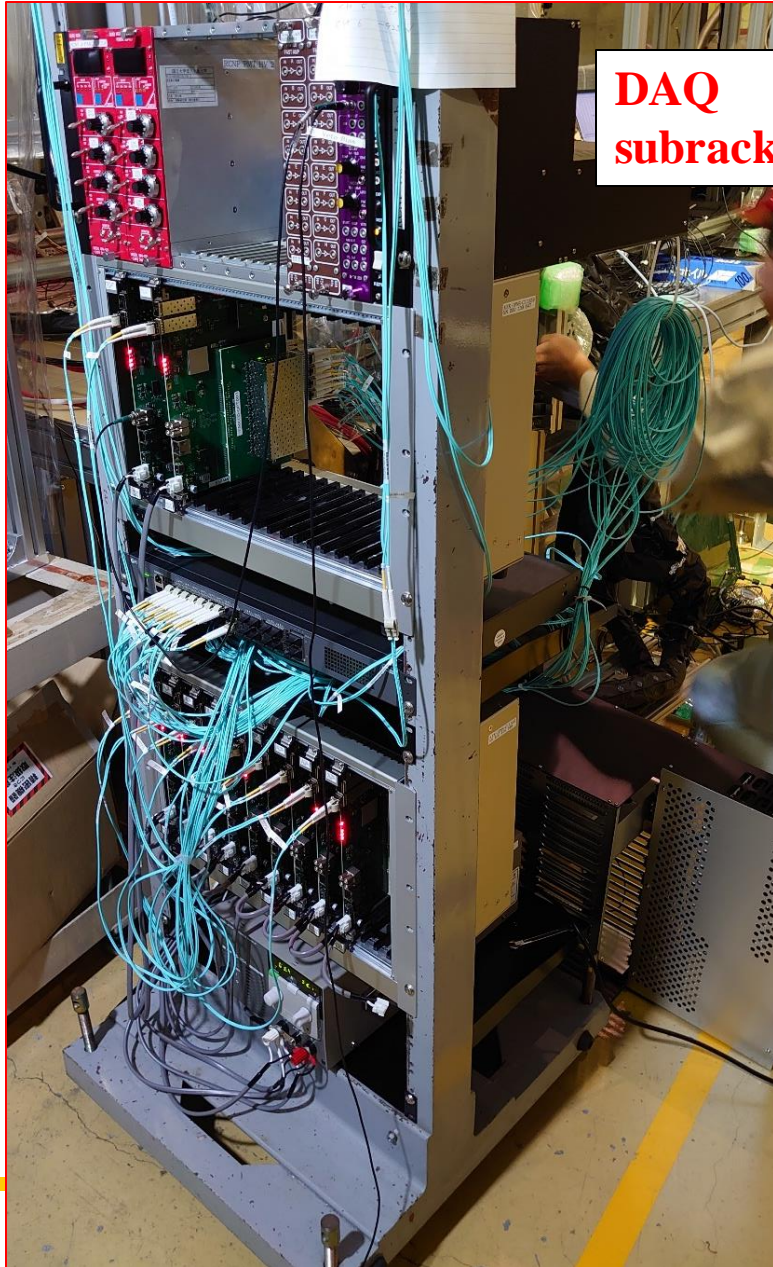- Test experiment/Physics experiment
  - ~0.2 Gbps in total

Tested at Hadron facility, K1.8BR beam line
- Synchrotron
  - Secondary hadron beams
    - π, K, p
  - Slow extraction
- Test experiment
  - ~2 Gbps in total
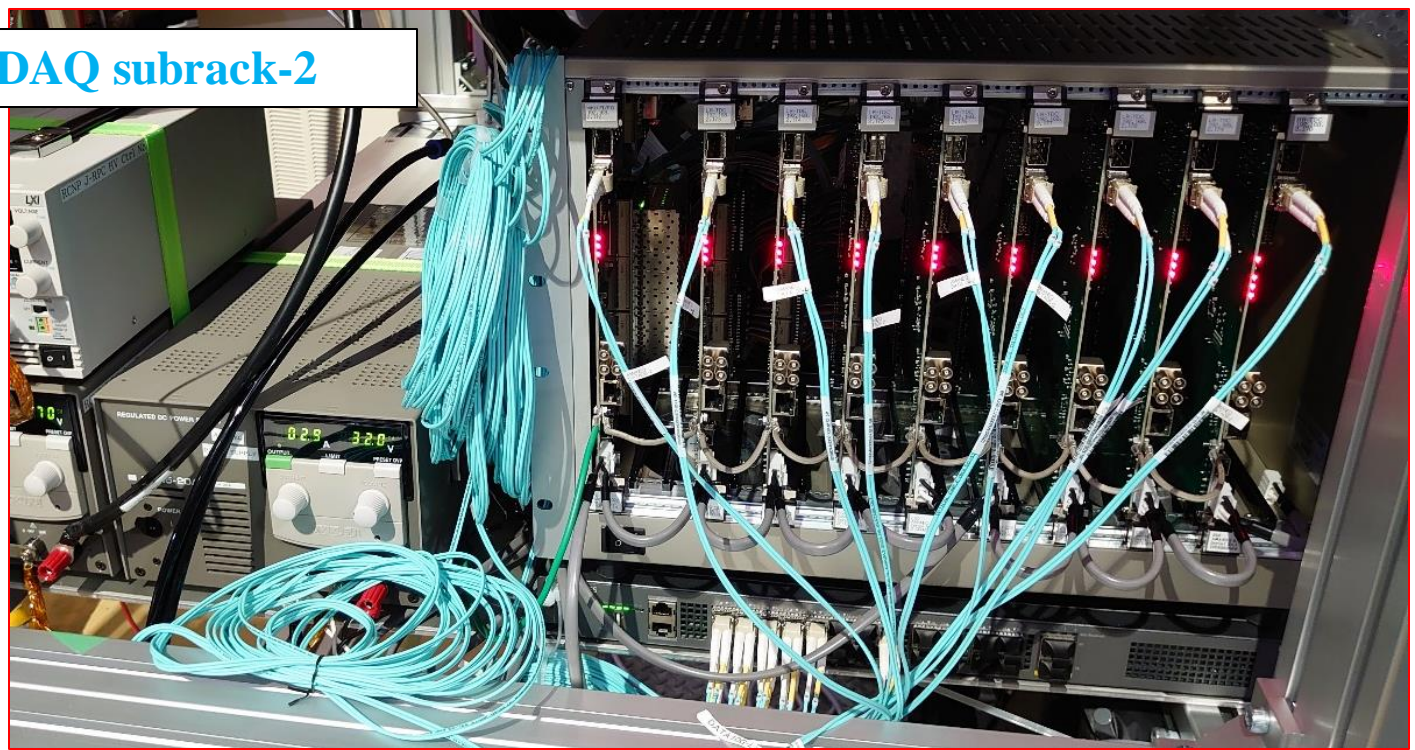
Pictures of text exp. at J-PARC

Picture of AMANEQs

DAQ subrack-2

DAQ subrack-1

Detectors

- BDC: 900 ch + KLDC: 512 ch
- SFT: 384 ch
- TOF, MRPC, Timing counters: 62 ch

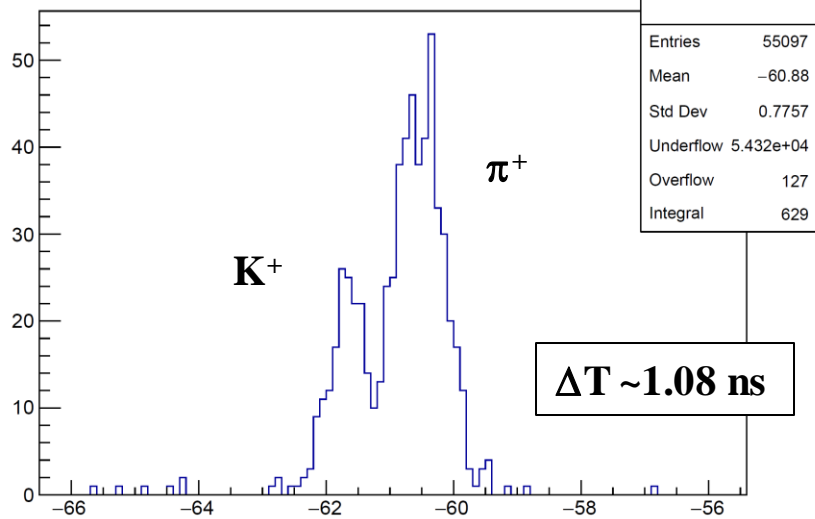Read by Str-LRTDC (1ns)

Read by Str-HRTDC

DAQ system

- FEE: AMANEQ x20 (Streaming TDC x17 + MIKUMARI x3)
  - Str-LRTDC AMANEQ x15
  - Str-HRTDC AMANEQ x2
- NestDAQ software running on a PC

Compact system was achieved

K⁺ beam mode

$\Delta T \sim 1.08$ ns
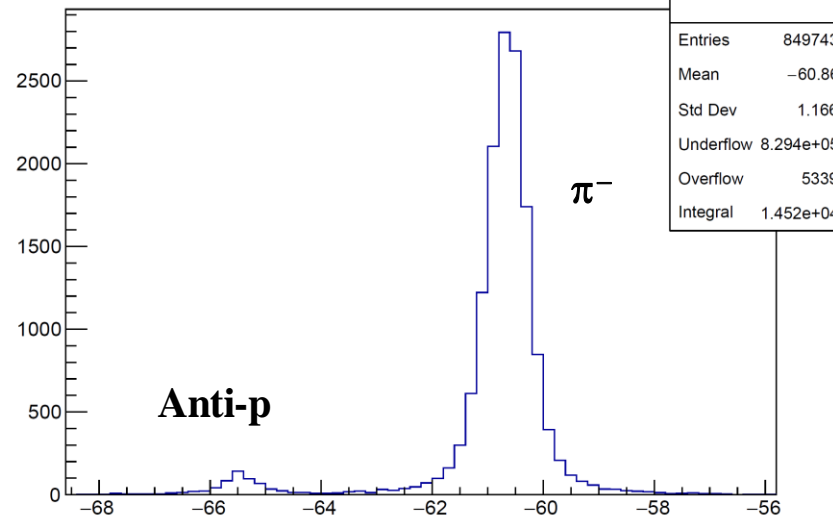
Anti-proton beam mode
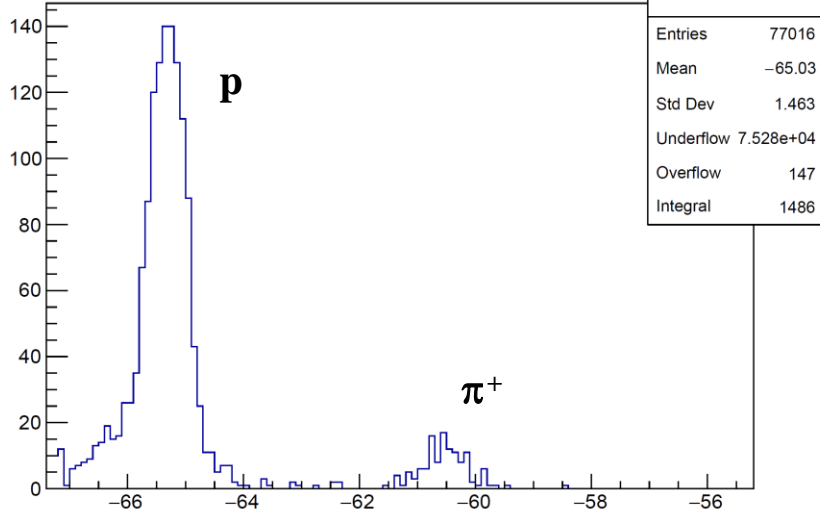
Proton beam mode

Anti-proton beam mode (log scale)

$\Delta T \sim 4.87$ ns
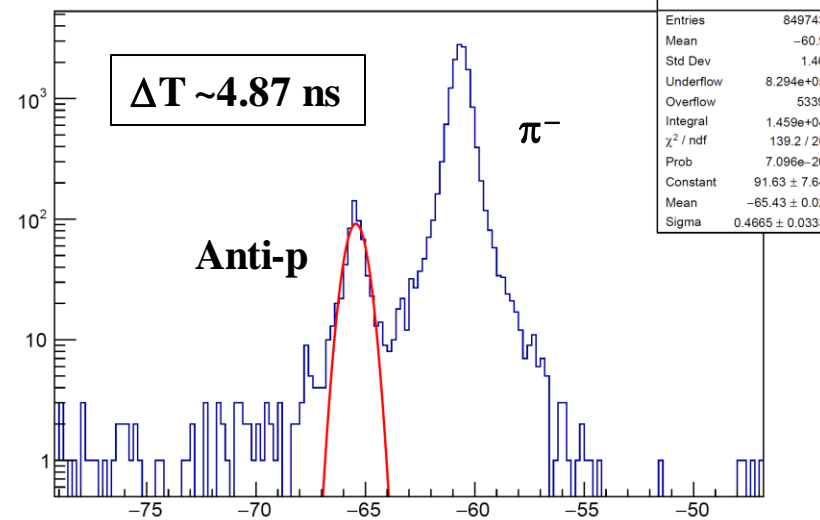
Beam condition
- Mom. : 1 GeV/c
- Flight path length: ~2.6 m
  - 8.67 ns for β=1

Beam purity for K⁺ beam
- K/π ~ 1/3

Trigger-less data-streaming data taking was performed

Events are successfully reconstructed

Future prospect

Implementation of SRO to other FEEs

So far, we have developed…
- Streaming high-resolution TDC (25 ps)
- Streaming low-resolution TDC (1 ns)

Same techniques, heartbeat method and MIKUMARI, will be implemented to FEEs developed under SPADI-alliance (and Open-It)

SPADI
Alliance
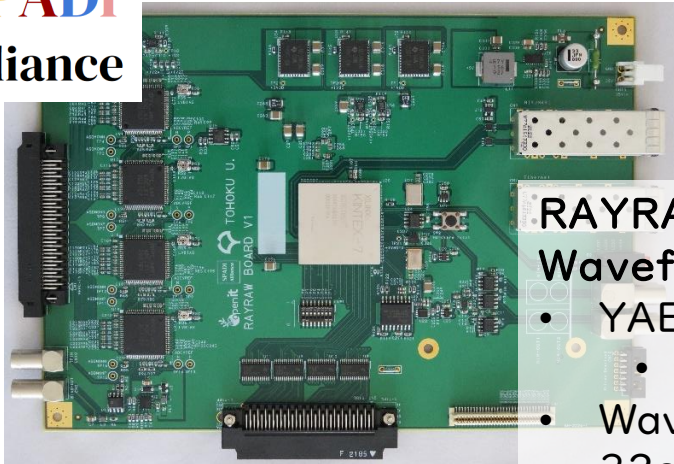
RAYRAW:
Waveform digitizer for MPPC-RO
- YAENAMI ASICs
  - ASD + 10-bit ADC
- Waveform + TDC (1ns)
- 32ch

CIRASAME: MPPC-RO
- CITIROC ASICs
- TDC (1ns)
- 128ch

SPADI
Alliance

SAMIDARE: TPC-RO FEE
- SAMPA ASICs
- Waveform
- 128ch

openit
Open source consortium of Instrumentation

Summary

So far, we have developed several key technologies for the general purpose DAQ system
- Heartbeat method to overcome a problem of long-length counter
- Simple and light-weight synchronization technology: MIKUMARI
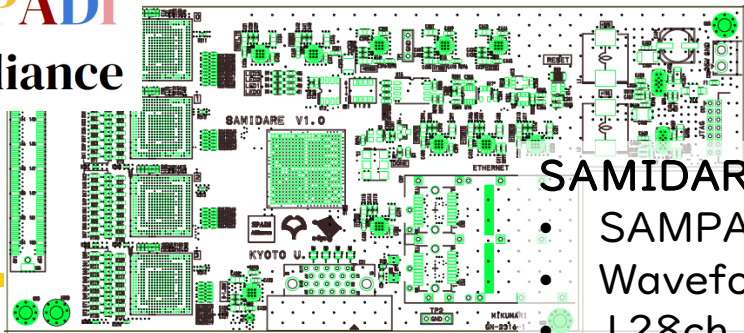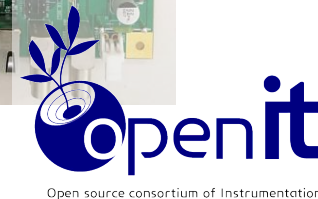- Next generation DAQ software frame work: NestDAQ
  - Semi-automatic topology generation based on service registry by redis

Implementation of Streaming HR-TDC into the AMANEQ board
- TDL based HR-TDC is outsourced to the mezzanine card
  - 64 (32+32) ch input per AMANEQ using two HR-TDC mezzanine cards
- ~25 ps timing resolution including the synchronization precision.
- Data communication by 10GbE

The developed Str-HRTDC was tested in the RCNP Grand RAIDEN and J-PARC hadron facility
- Grand RAIDEN at RCNP
- K1.8BR beam line at J-PARC
  Full-streaming readout and software based event selection was successfully performed

Future prospect
- Implement streaming function to other FEEs developed under SPADI-alliance

Toward trigger-less data-streaming DAQ system

Event selection by hardware based trigger

- Define a data block, "Event"
- Provides the reference timing to set RoI

Conventional DAQ system

Trigger

Trigger generation by hardware is becoming difficult
- Resource is not enough even for world largest FPGA
- Current hardware trigger logic is so much complex
- Difficulty to maintain and develop them

DAQ software

Detector	→	FEE	→	Reader
Detector	→	FEE	→	Reader
Detector	→	FEE	→	Reader
Detector	→	FEE	→	Reader

Partial builder

Partial builder

Event builder

HLT

HLT

HLT

File sink

Option

Data within the RoI are sent to the PC.

DAQ software configuration based on tree-like topology

Data collection relying only on timestamps

Structure of TDC data

$$\underline{\text{Fine count (n-bit)}} \quad + \quad \underline{\text{Coarse count (m-bit)}}$$

Provided by timing interpolation techniques
- Sampling by multi-phases clock signals
- Tapped-delay-line

Independent from data acquisition function

Generated by the DAQ function driven by system (base) clock signal.

In conventional TDC
- The bit-length depends on the record length since it is the relative timing measurement respect to the trigger.
    - E.g., ring-buffer length ⇔ coarse count bit-length

In streaming TDC
- No local timing reference. It will be free running, but what length is necessary?

FEE data format
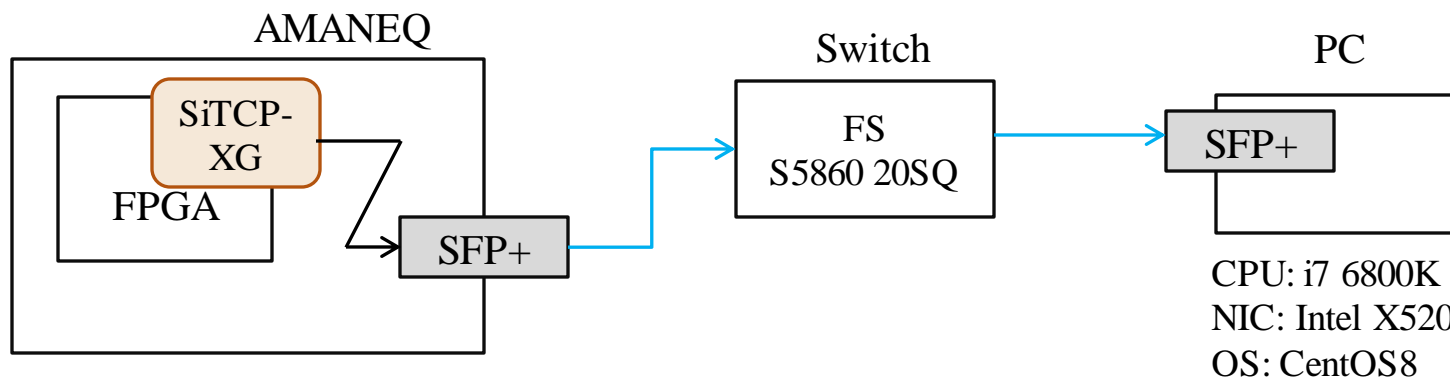
In conventional TDC
- Data header (trailer) exists as the boundary of the data block.
    - It may contains data size, event number, flags, etc…

In streaming TDC
- No local data block, an event, exists. Another data format must be introduced.
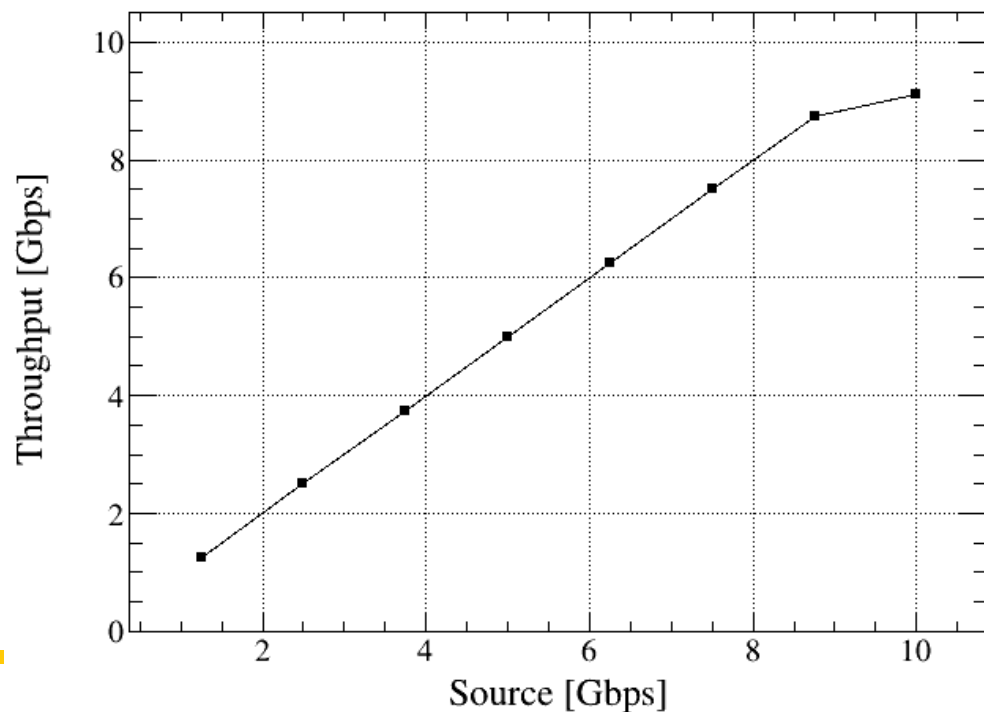
Data transfer speed via SiTCP-XG

Test setup

AMANEQ

SiTCP-XG

FPGA

SFP+

Switch

FS
S5860 20SQ

PC

SFP+

CPU: i7 6800K
NIC: Intel X520
OS: CentOS8

Read data using
C++ software.

Tested by H. Sendai (KEK E-sys)
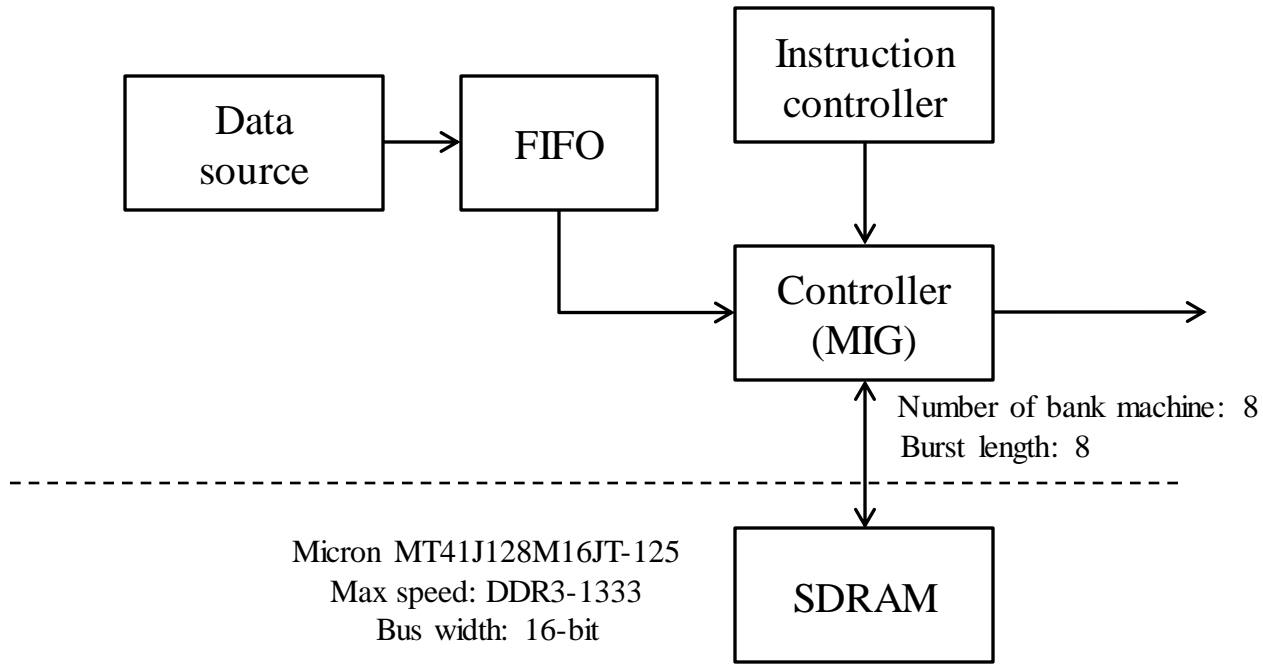
Measured throughput

Obtained throughput: 9.12 Gbps
    ~96% of TCP payload limit (MTU 1500)
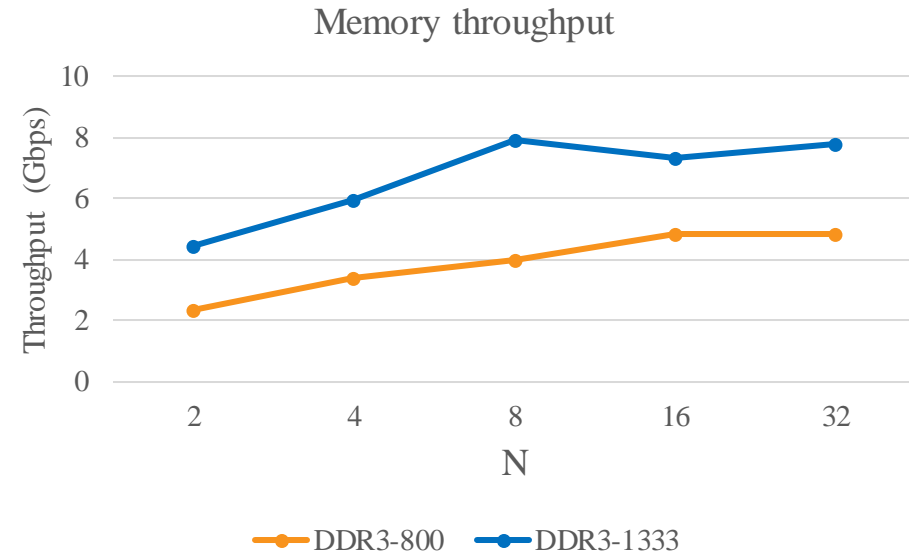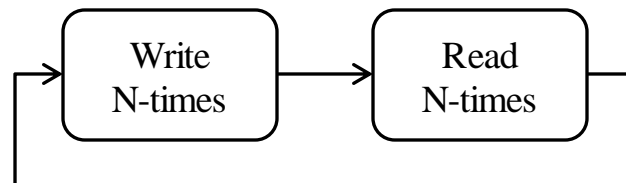
Firmware configuration

```
┌──────────┐      ┌──────┐         ┌────────────┐
│   Data   │ ───► │ FIFO │         │ Instruction│
│  source  │      │      │         │ controller │
└──────────┘      └──────┘         └────────────┘
                      │                    │
                      │                    ▼
                      │            ┌────────────┐
                      └─────────►  │ Controller │ ──────►
                                   │   (MIG)    │
                                   └────────────┘
```

Number of bank machine: 8
Burst length: 8

Micron MT41J128M16JT-125
Max speed: DDR3-1333
Bus width: 16-bit

```
┌──────────┐
│  SDRAM   │
└──────────┘
```

Data bus of SDRAM is bi-directional.
Memory operation is determined by command.

Tested write/read pattern.

```
  ┌─────────┐     ┌─────────┐
┌►│  Write  │ ──► │  Read   │┐
│ │ N-times │     │ N-times ││
│ └─────────┘     └─────────┘│
└───────────────────────────┘
```

Memory throughput

Obtained throughput (reference value)
DDR3-800
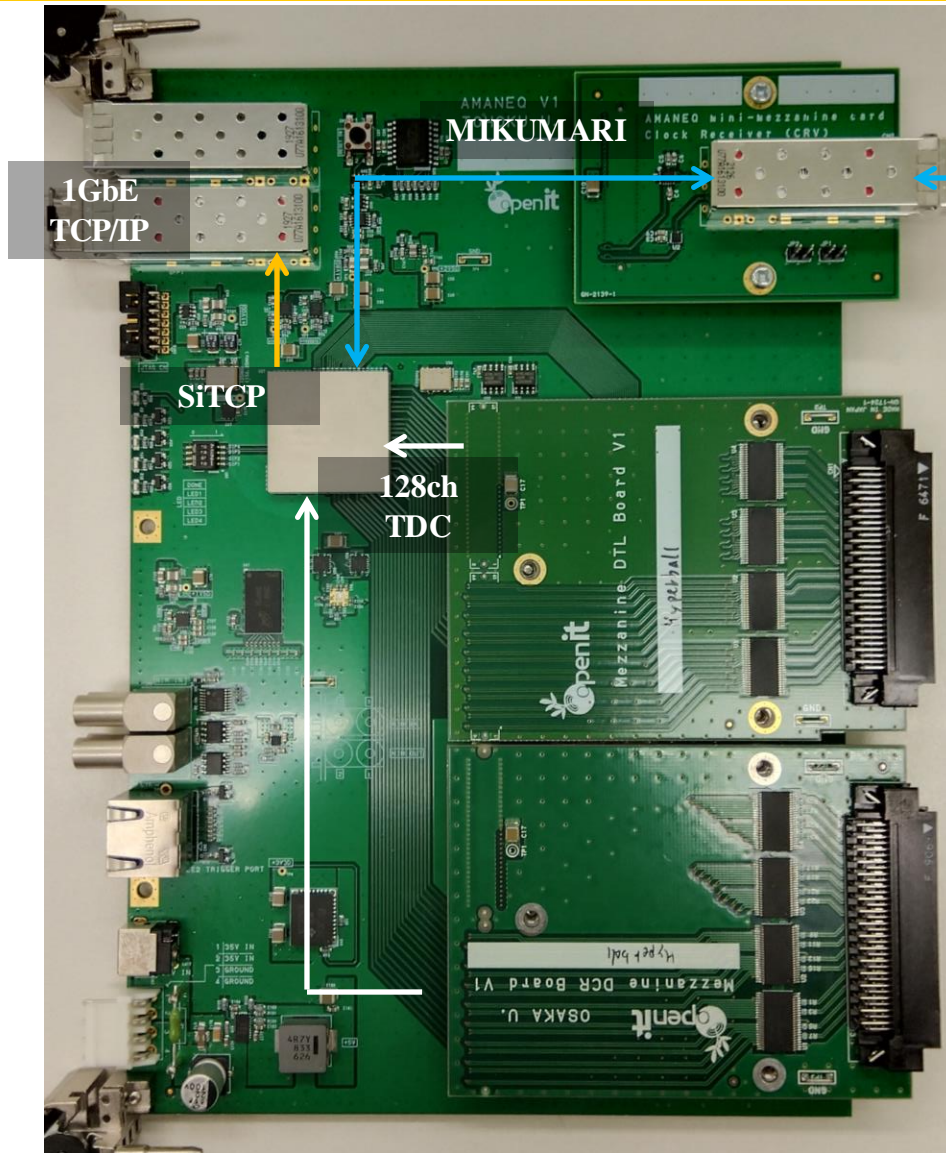- ~4.8 Gbps (6.4 Gbps)

DDR3-1333
- ~7.9 Gbps (10.66 Gbps)

***Access to the same memory bank.
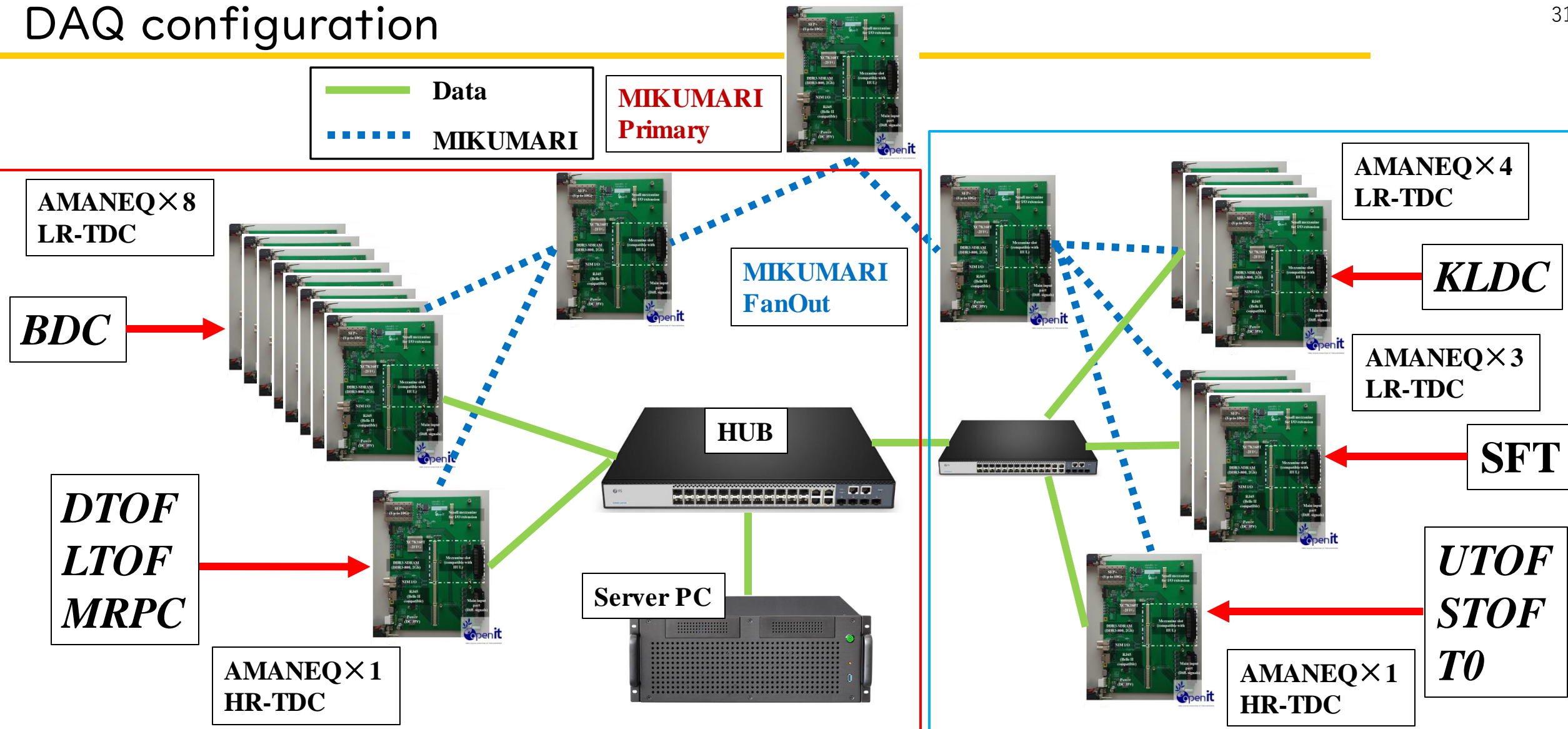Larger over head when changing the bank address.

Streaming LR–TDC on AMANEQ

Modulated clock
from upstream (distributer) module

AMANEQ Str–LRTDC
- Input : 128 ch
  - Mezzanine cards are changed
- Timing precision: 1ns
  - (Resolution is better than 1ns)
- Data link: 1GbE
  - TCP/IP provided by SiTCP
- Operation mode
  - Stand alone mode
  - Sync with MIKUMARI system

DAQ configuration

- Synchronize 20 AMANEQs using MIKUMARI network
- Readout the data from FEE with a server PC