SRO timing distribution system in Japan

Hidetada Baba

RIKEN, Nishina Center, Japan

Overview

- **under consideration**
  - please tell us your experiences
- Requirements are strongly dependent on facilities or experiments
  - 100 ns v.s. 25 ps
  - 1 meters v.s. 100 meters
  - clock only v.s. data + clock
  - local time v.s. global time v.s. sync. with accelerator frequency
- Hardware, methods
  - latching scaler, white rabbit, etc
  - KEK Honda's MIKUMARI (as described previous talk)
  - Versatile clock transceiver module based on AMD Xilinx Kria (this talk)
- we have started some studies, we share our knowledge
  - SPADI Alliance in Japan
  - timing distribution system is not only for SRO, but also for trigger DAQs

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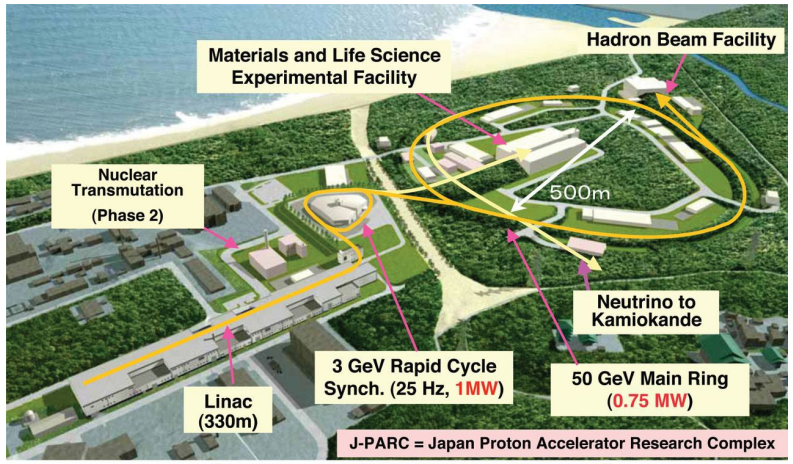
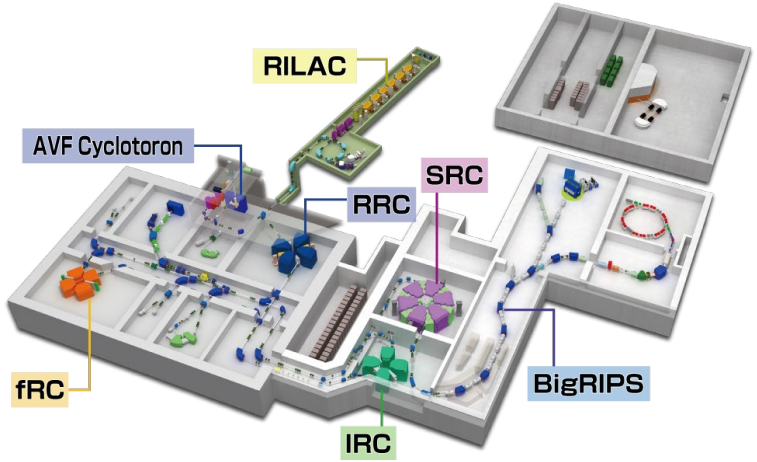
Nuclear physics Accretor facilities in Japan

J-PARC

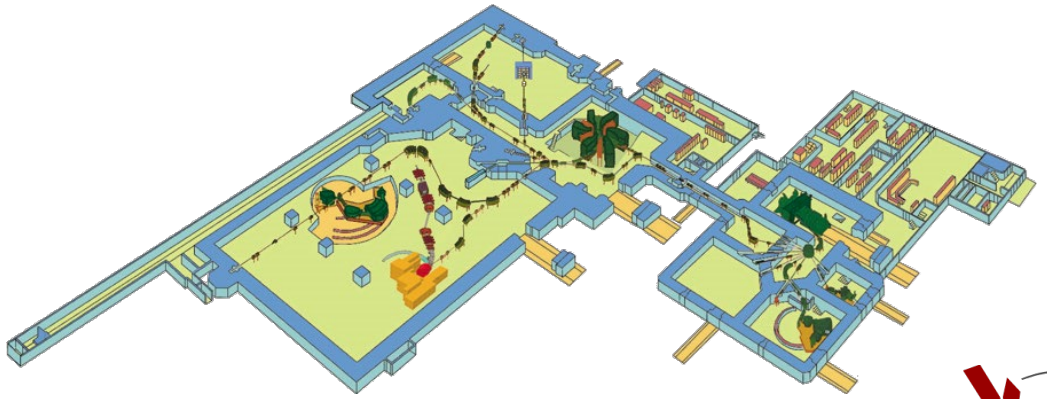


Joint Project between KEK and JAEA

RIKEN, RIBF

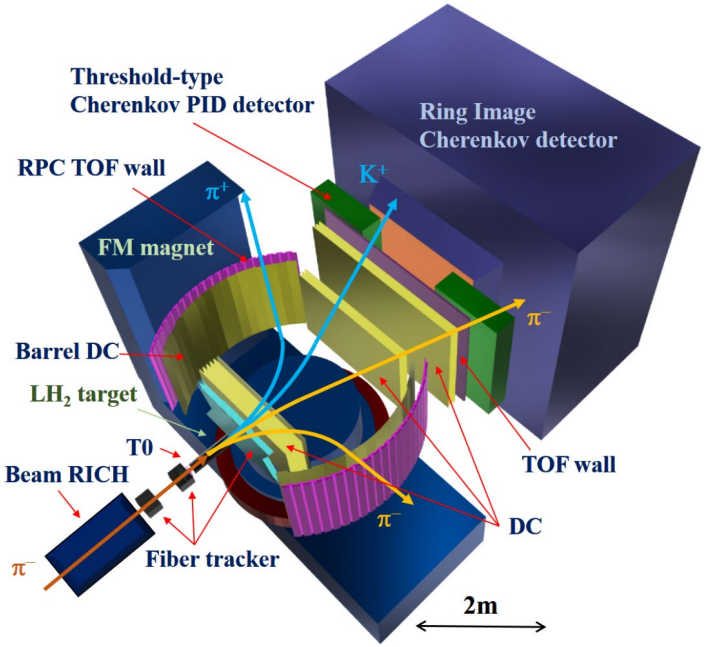


RCNP, Osaka-U



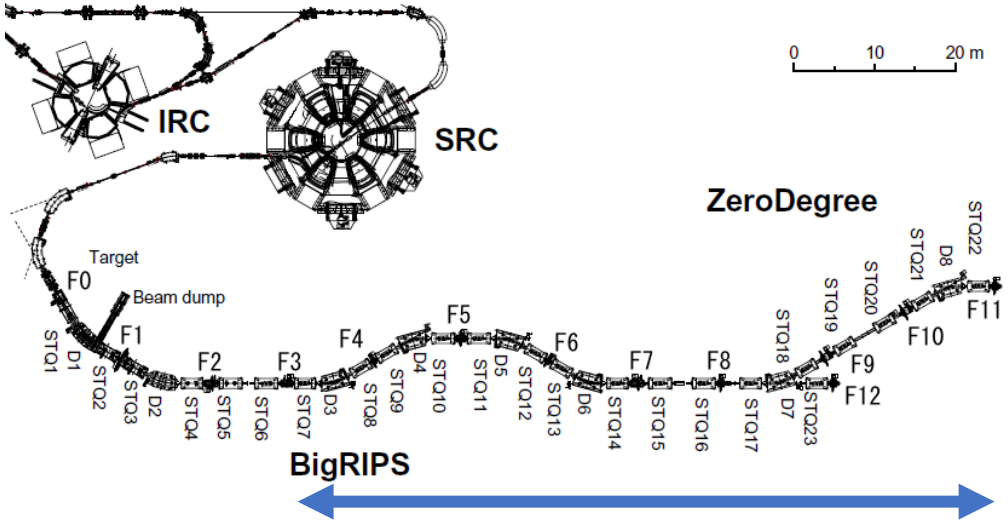
Requirement of timing information

J-PARC E50 (hadron experiment)

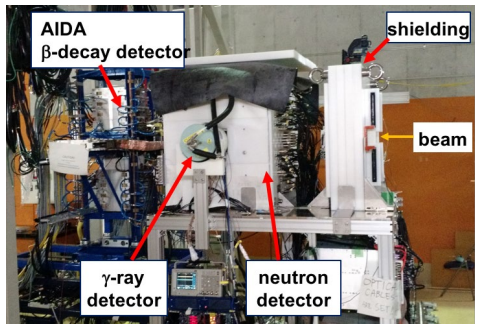


TOF **50 ps** @ few meters
MIKUMARI is suitable

RIBF BigRIPS Particle Identification (RI-beam experiment)



TOF **25 ps** @ **100 meters**



beta-decay experiment@RIBF
RI's lifetime is milli-second order
-> 10ns order synchronization

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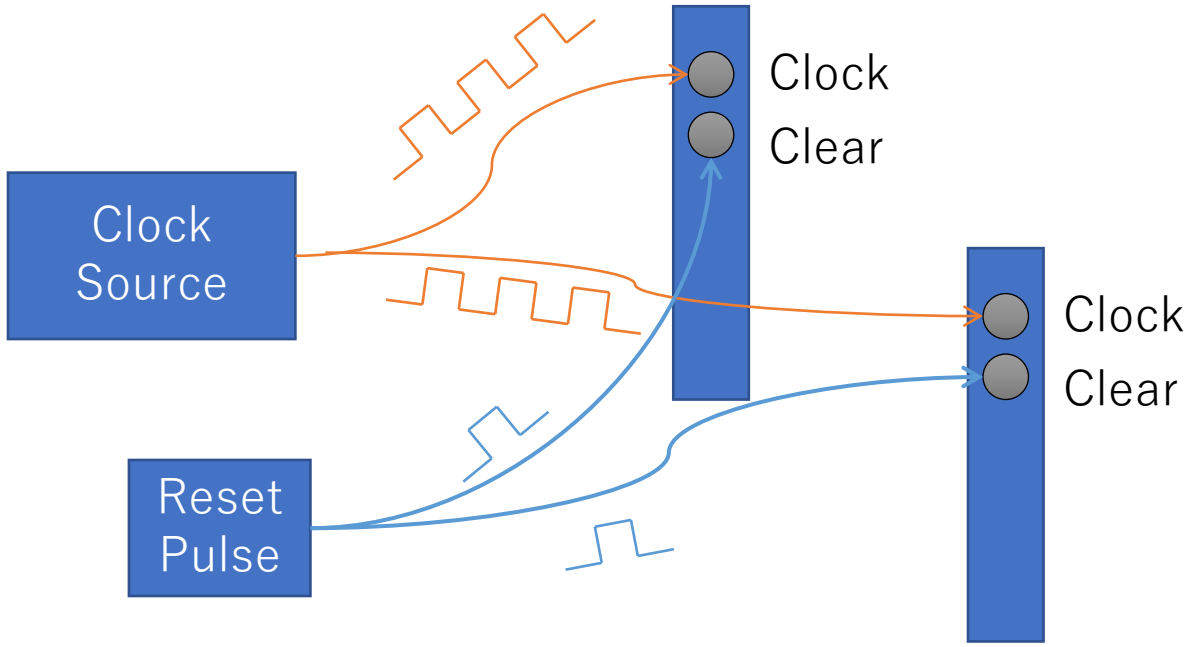
for Beta-decay experiments @ RIBF

requirement is 10ns synchronization

time-stamp by plain HDL latching scaler

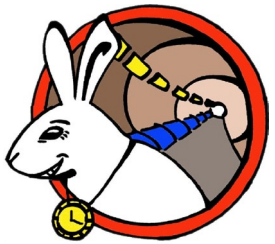
two metal coax. lines: clock + reset (T0)
point-to-point + daisy-chain

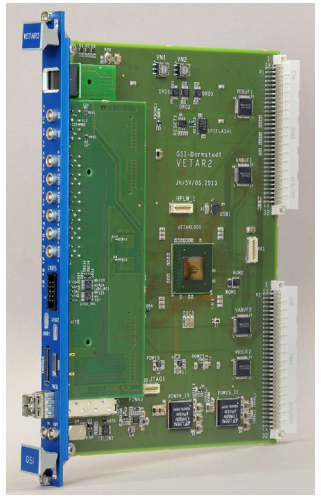


100 MHz (**10ns**), 48 bits (kind of latching scaler)

white rabbit

1 optical cable : clock + data
switch fabric





125MHz (**8ns**) from year 1970
(w/o phase detection in this case)

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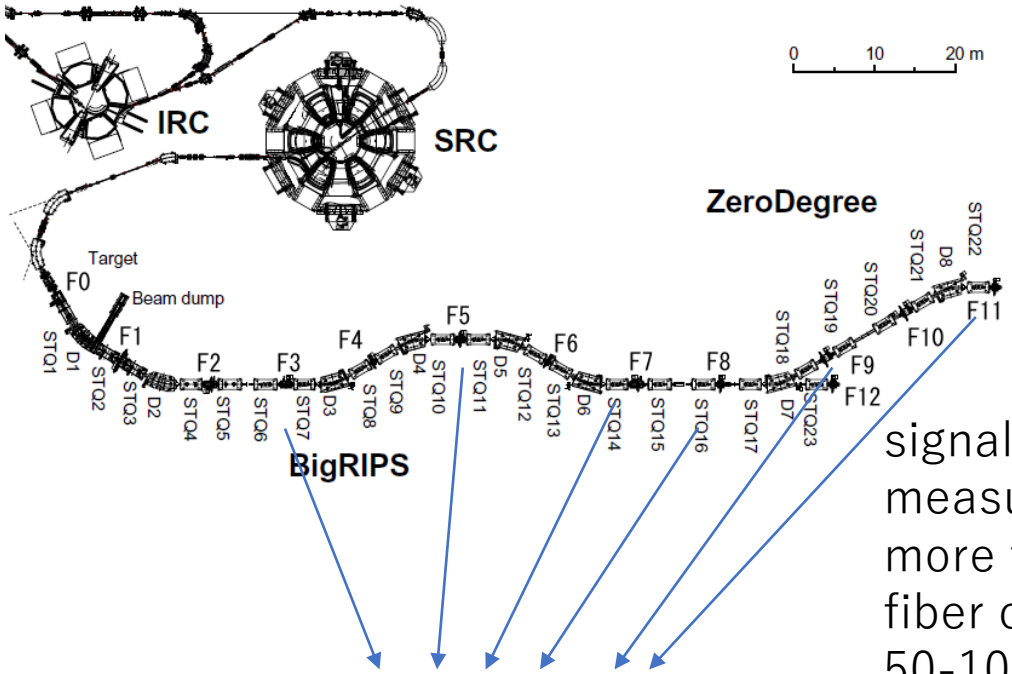
at RIBF, 100-meters TOF 25ps (σ) resolution

Current system

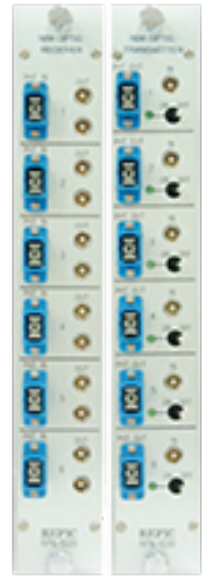


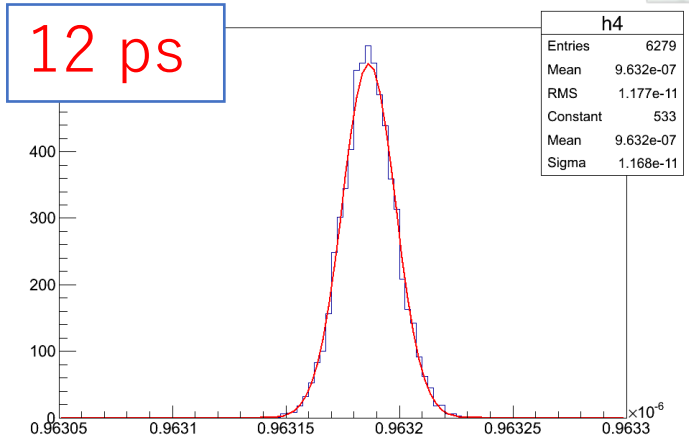
signals are sent to the measurement area using more than **500** single-mode fiber cables (each cable is 50-100 meters long)

measure TOF by a conventional TDC

start-stop

optical transmitter/receiver
+ 192meters single-mode fiber
+ discriminator + few meters coax
+ LEMO connectors





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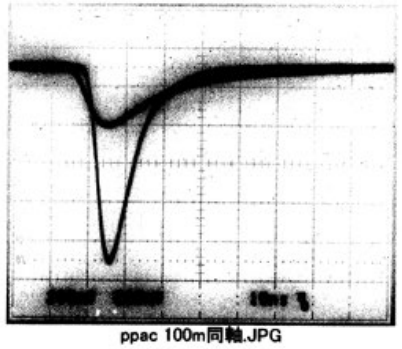
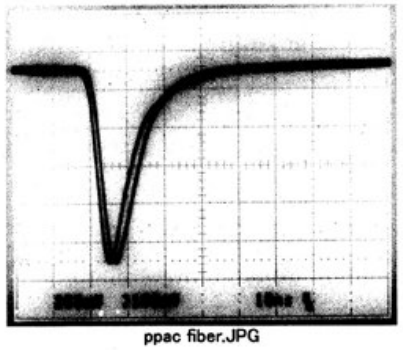
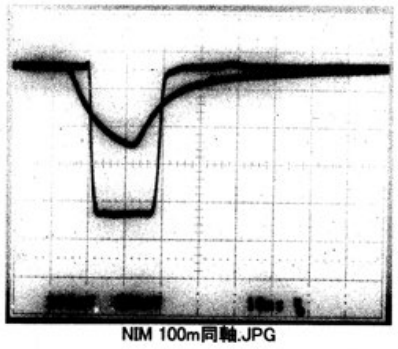
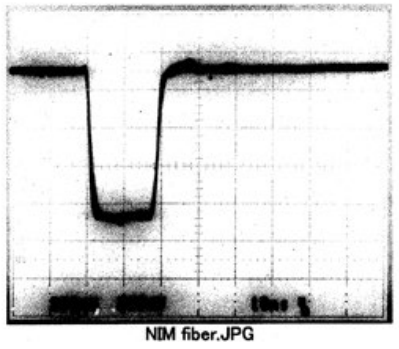
Analog and NIM logic signal via Single-mode fiber







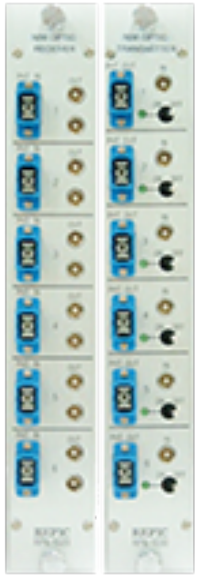


Metal coax. cable
100m

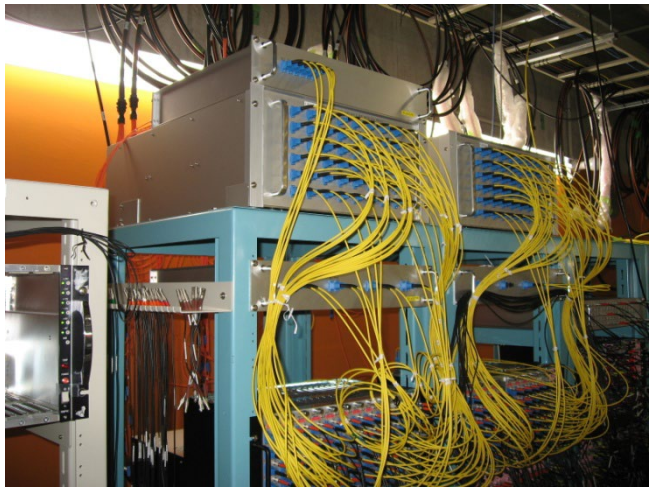
Optical cable
100m

expensive $2,000 / 1 link
end of production
(laser and photo-diode)

- NIM module (transmitter/receiver)
  - **Time jitter is < 5ps**
  - there are 2 types, analog and NIM logic
- Analog signal version
  - AC couple
- NIM logic version
  - DC signal can be transmitted



1.5 us Optical cable delay box



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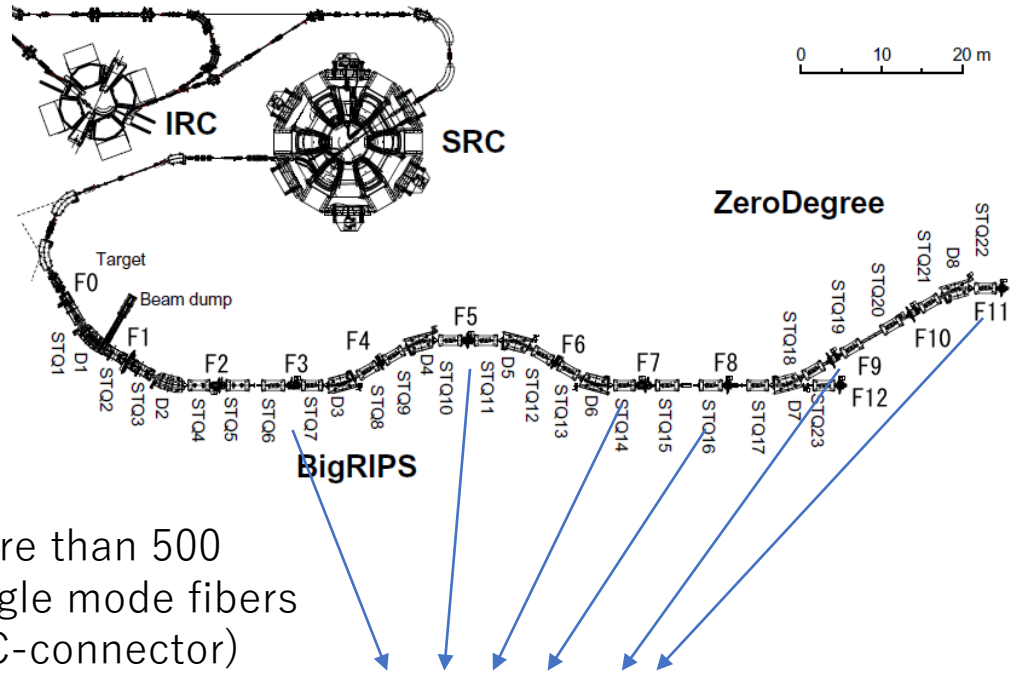
Plan = clock distribution

Current system

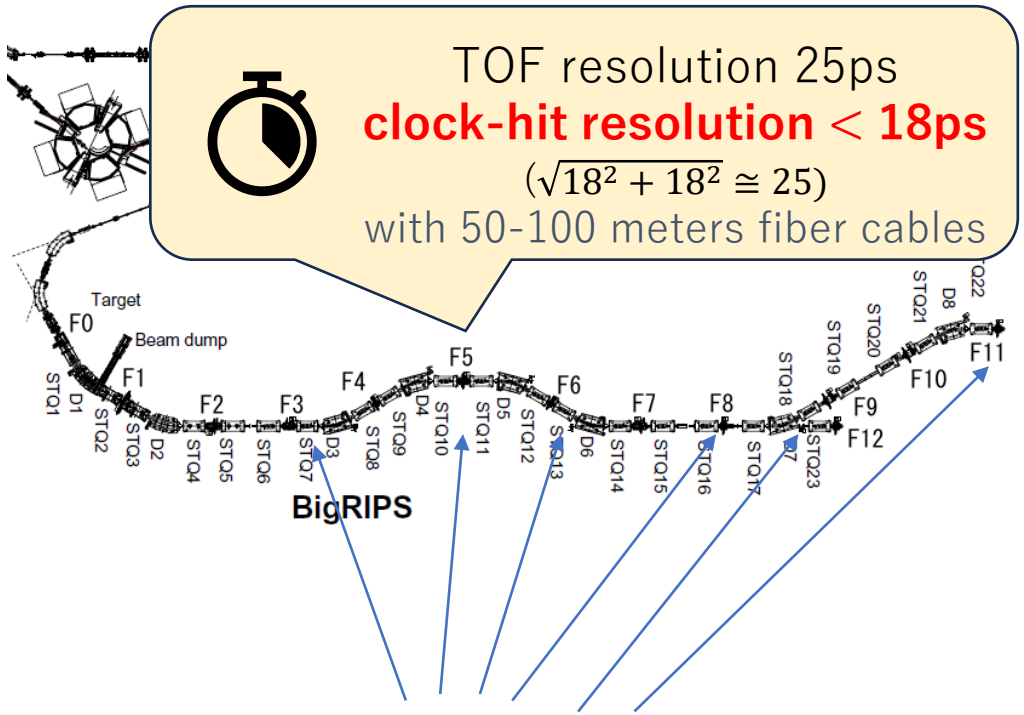


more than 500
single mode fibers
(SC-connector)

measure TOF by a conventional TDC

start-stop
(trigger-hit)
TOF resolution 25ps

Near future system



distribute Clock

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need to communicate with other systems

try to implement 2 stages clock distribution

Clients depend on experiments. At RIBF, experimental setup changes every few weeks.

Str-TDC (MIKUMARI)

trigger DAQ

WhiteRabbit

latching scaler

Others

few meters

Clock Station

Clock Station

Clock Station

Station-to-FrontEnd Link
interface to other systems
MIKUMARI, WhiteRabbit, etc

Clock Center candidate (COTS)

50-100 meters

Clock Center

CORE-to-Station Link
study from now!

GSI/FAIR BUTIS + WhiteRabbit is very nice for kiro-meters sync., but very special

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Plan for Clock Station

will be delivered March 2024

Versatile clock transceiver based on AMD Xilinx Kria

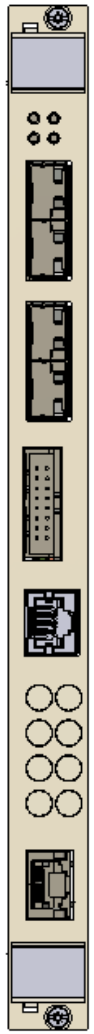
2 x SFP+ for GTH
(gigabit transceiver)

2 x SFP+ for HPIO
(normal port)

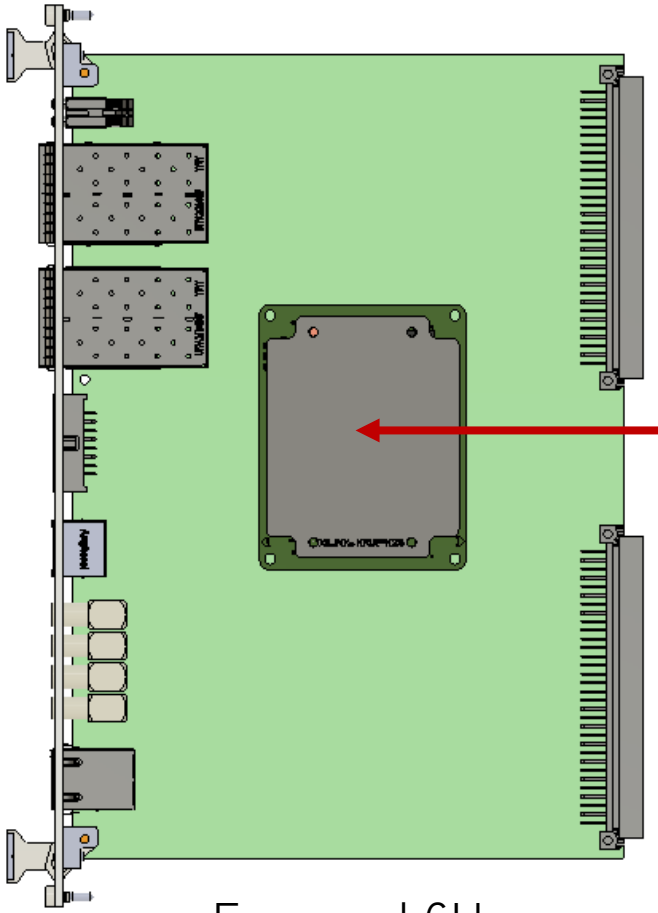
LVDS I/O

NIM I/O

1Gbps Ether

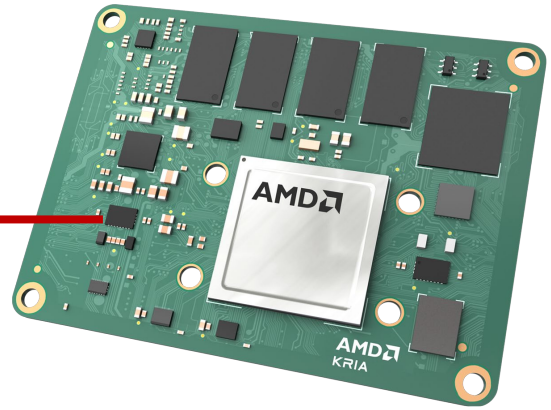


communicate with
MIKUMARI
WhiteRabbit
Xilinx AURORA
latching scaler
etc..
will be worked as
protocol translator



Eurocard 6U

AMD Xilinx Kria K26 SoM



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many works from now

- How to describe time?
  - from EPOCH (1970)? or from arbitrary T0 (time reset)? or 20XX-Jan-01?
- correction of propagation delay change
  - to get enough TOF resolution
  - MIKUMARI + temperature / phase monitor
  - White Rabbit + temperature / phase monitor
    - H. Li et al., “Temperature Effect on White Rabbit Timing Link”, IEEE TNS 62, 1021 (2015)
  - some thoughts
    - use single cable + WDM (same as White Rabbit)
      - should have the same delay for both TX and RX
    - use 2 cables (1 pair)
      - 1 pair for clock+data TX/RX
    - use 4 cables (2 pairs)
      - 1 pair for data link (TX/RX)
      - 1 pair is for clock (TX for clock distribution, RX-loop-back for monitor)
    - how to implement a phase detector?
      - DDMTD (WhiteRabbit)? TDC? simple XOR-based circuit?

always monitor phase changes, and put corrections somehow

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Summary

- Clock distribution
  - Under consideration
- for a link layer
  - we have MIKUMARI based on CDCM
  - there are several candidates
- protocol
  - what kind of functionalities do we need?
- we'll play with a Kria-based board

- Other topics
  - we have just started some studies on real-time data processing
    - HLS with AMD Xilinx Alveo
    - HLS+AI with AMD Xilinx Versal-AI
  - facility-to-facility fast data link
    - 100Gbps IPv6 connection via SINET6 in Japan without firewall
    - similar to ESnet6 in US
    - will be available from 2025
    - study with FPGA-based NIC (from 2024)

let's share our experiences

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