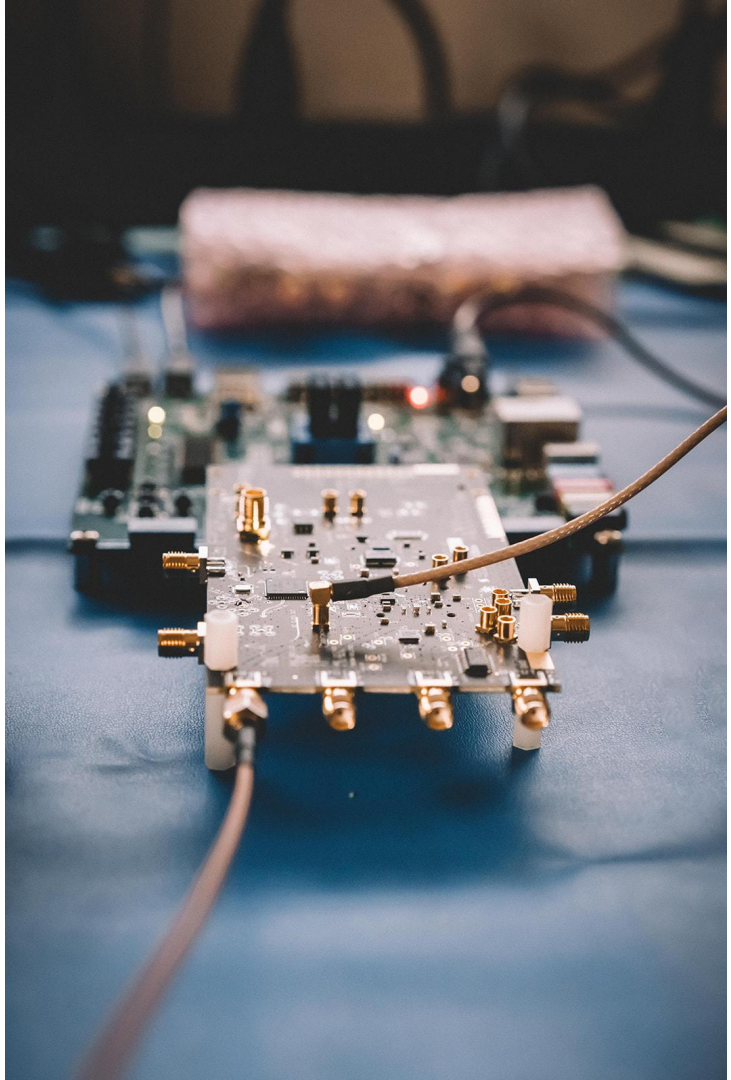

NALU SCIENTIFIC
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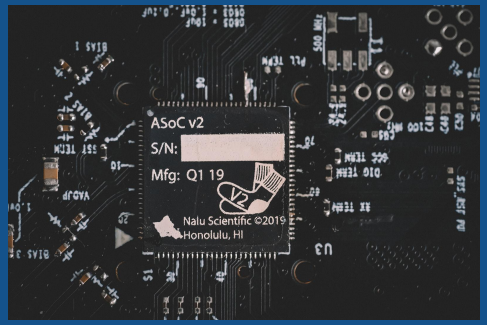
Waveform Digitizing Front-end Electronics for Streaming Mode High Density Detector Readout

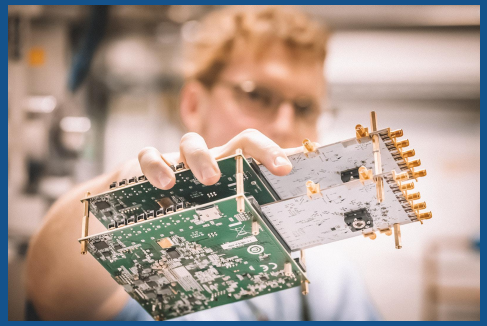
Nov 28, 2023
Isar Mostafanezhad, Ph.D.
Founder and CEO at Nalu Scientific LLC

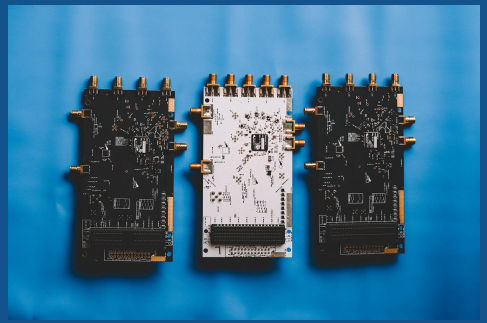
Work partially funded by US DOE SBIR Grants:

DE-SC0015231, DE-SC0017833, DE-SC0020457

https://indico.bnl.gov/event/20010/sessions/6402/#20231128







ABOUT NALU SCIENTIFIC

Agile Small Business in Honolulu, Hawai'i

- Located at the Manoa Innovation Center near U. of Hawaii
- 20 staff members: 7 PhDs, 5 MSc, 8 BSc
- Access to advanced design tools
- Rapid design, prototyping and testing

Vertically Integrated Team:

Microelectronics	Analog + digital System-on-Chip (SoC)
Hardware	Complex multi-layer PCBs
Firmware	FPGAs, CPUs, Embedded
Software	Data science, GUI, documentation
Scientific	Plasma, medical, physicists, space

Exclusive Distributor Agreement for North America CAEN Technologies Inc.

- Sales of ASICs, eval boards
- Enhanced OEM opportunities

Nalu = 'wave' in native Hawaiian language

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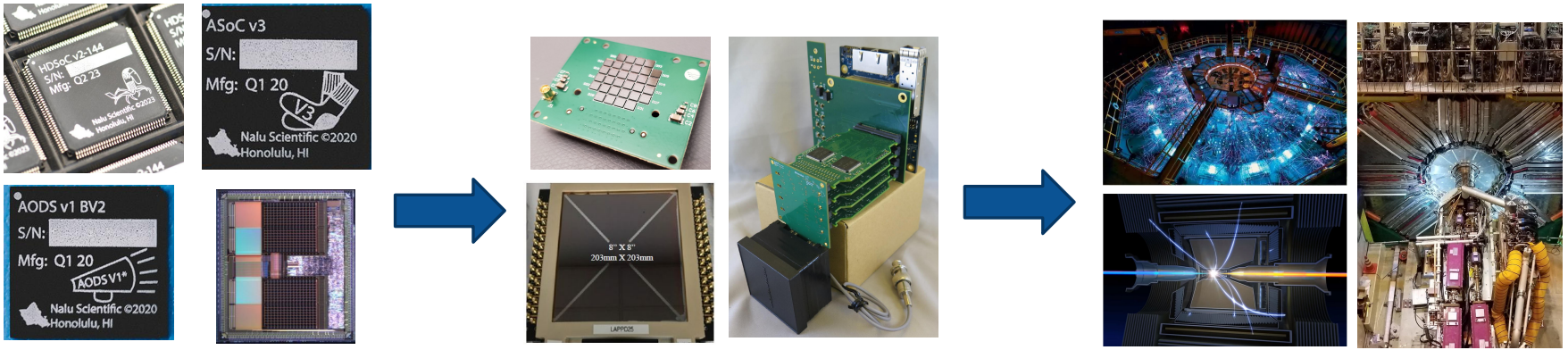
Core Technology:
Data Acquisition Microchips



1. Front-end Chips:

- Event based digitizer+DSP
- 4-32 channel scope on chip
- 1-15 Gsa/s, 12 bit res.
- Low SWaP-C
- User friendly: FW/SW tools

2. Integration:

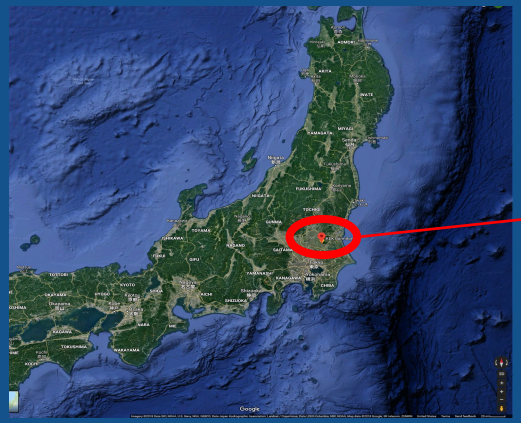
- SiPM
- PMT
- LAPPD
- Detector arrays

3. Applications:

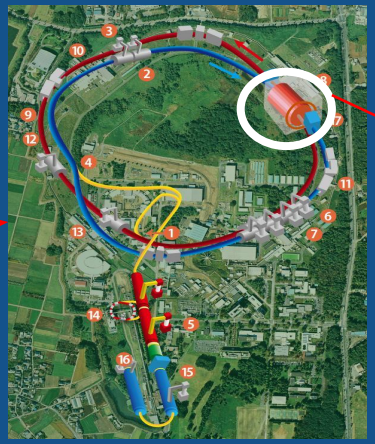
- NP/HEP experiments
- Astro particle physics
- Beam Diagnostics
- Plasma/fusion diagnostics
- Lidar
- PET imaging

WHERE WE STARTED

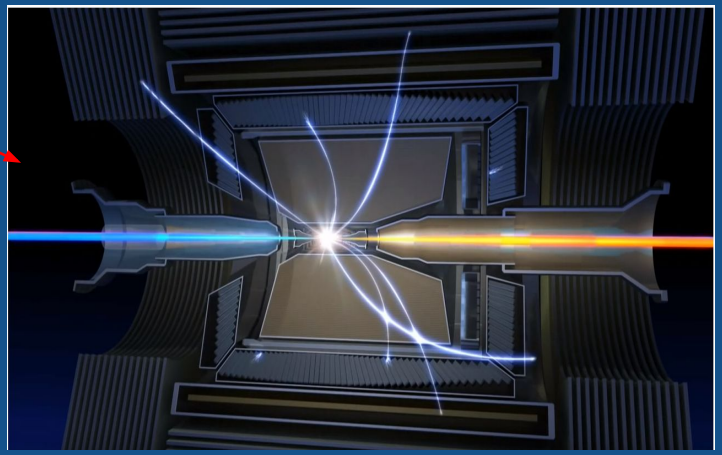
A Search for New Physics – The Belle II Experiment



Tsubuka City
Located 60 mi north of Tokyo



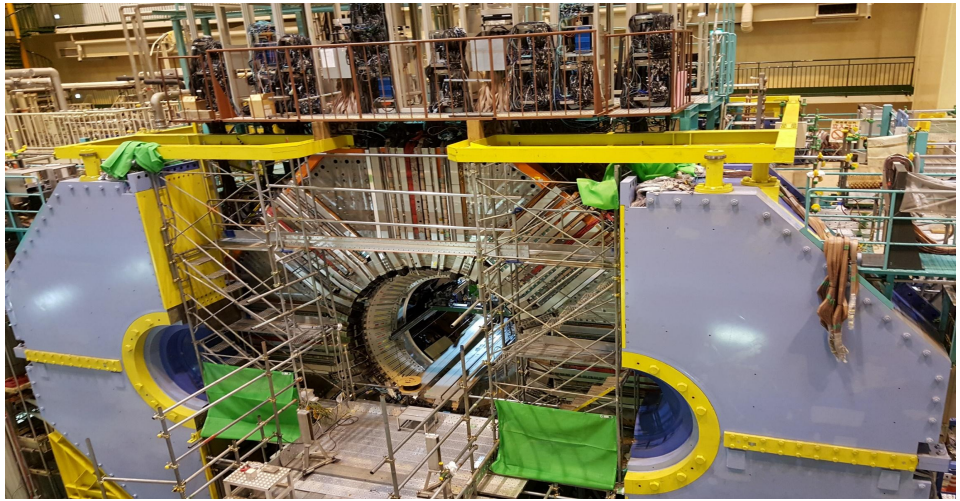
High Energy Accelerator Research Facility (KEK)
in Tsukuba



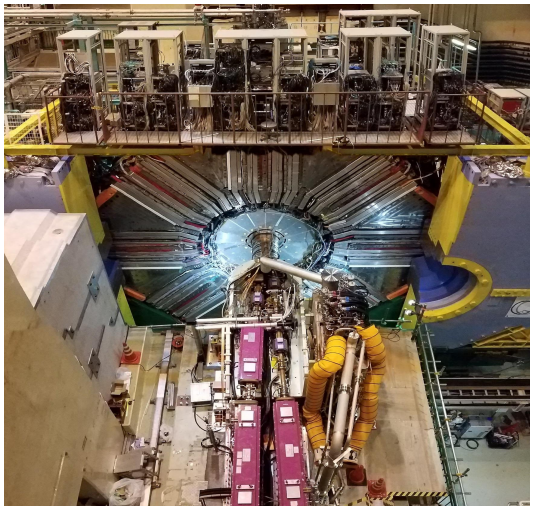
Interaction point inside the electron/positron collider

HISTORY - BELLE II

Belle II Upgrade is a 26+ Country, 900 Member Collaboration



2015



2018

Nalu Staff designed and implemented front-end electronics and FW for KLM (muon system) and iTOP (Cerenkov-based PID) sub-detectors.

Belle II: e+ e- experiment at 40x luminosity of Belle -> Detector needs to operate at severe beam background. L1 trigger at 30 kHz

NALU SCIENTIFIC
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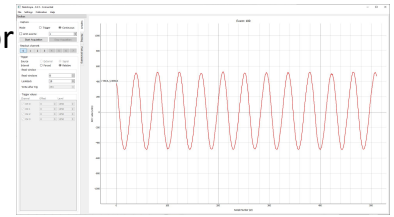
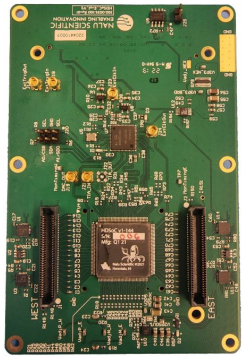
Current ASIC Projects

Project	Sampling (GHz)	BW (GHz)	Buffer (Samples)	Number of Channels	Timing Res. (ps)	Available Date
ASoC	3-5	0.8	16k	4	35	Rev 3 avail
HDSoC	1-2	0.6	2k	64	80-120	Rev 2 avail
AARDVARC	8-14	2.2	16k	8	10	Rev 4 avail
AODS	1-2	1	8k	1-4	100-200	Rev 2 avail
UDC	8-10	1.5	4k	16	10	Rev 1 avail

- DOE Phase I/II SBIRs
- Low SWaP-C specialty digitizers for
  - Radiation detection
  - Photonic sensors
  - Time of Flight (ToF)
  - Medical imaging
  - Space
  - Rad hard and harsh
- Evaluation PCBs available
- Extensive suite of software tools
- All microchips and tools available through CAEN Technologies USA

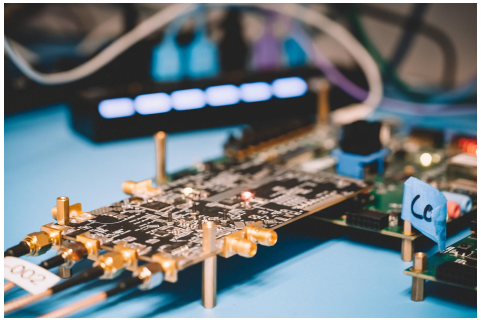


Software



Eval PCB

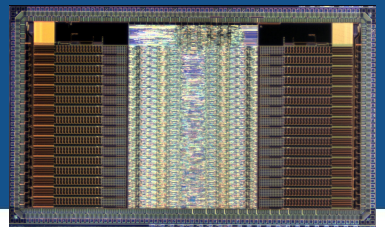
Microchips



HDSoC DESIGN CONCEPT DETAILS

High density waveform digitizer

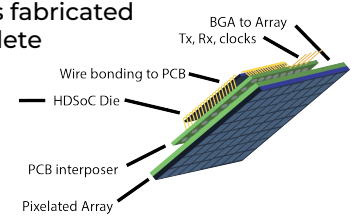
- High Density: 64 channels (V1:32, V2:64)
- Full waveform sampler and digitizer
- Highly integrated, SiPM gain + bias
- Commercially available, low cost CMOS

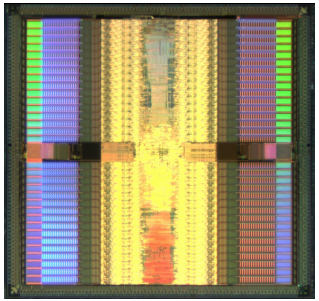


HDSoC v1 die shot

Parameter	Target Spec
Sampling Rate	1-2 GSps
ABW	> 600MHz
Depth	2k Sa
Trigger Buffer	~2 us (@1Gsps)
Deadtime	0**
Channels	32/64
Supply/Range	2.5
ADC bits	12
Timing accuracy	80-120ps
Technology	250 nm CMOS
Power	20-45mW/ch

- On chip TIA
- Serial interface (up to 500 Mbps)
- Discriminator for self-triggering and zero suppression - exported in dedicated serial stream
- Virtually dead-timeless (buffer virtualization)
- Feature Extraction
- 32 ch and 64 ch proto chips fabricated
- Phase II SBIR almost complete





HDSoC v2 die shot

**If average rates compatible with maximum limits - see below for current measurements

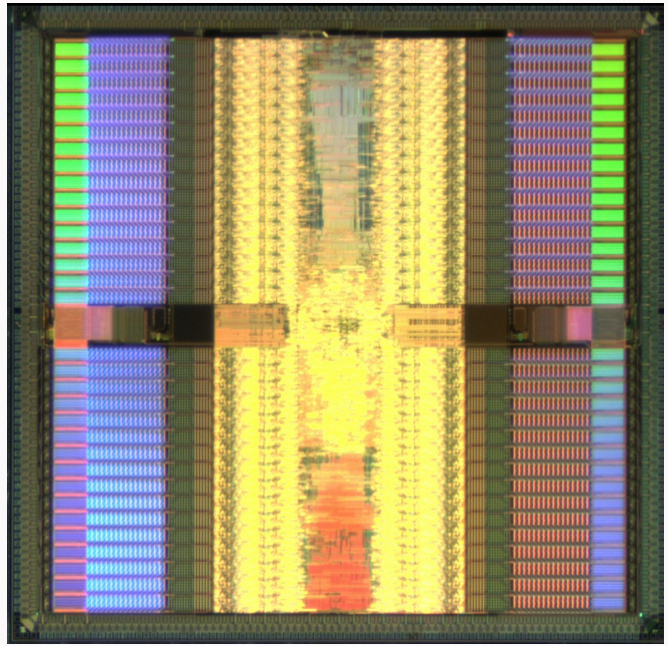
HDSoC Rev. 2 - Streaming Features

- **Channel independence**:
  - Each channel can perform digitization autonomously using dedicated resources (Wilkinson counter, ramp generator)
  - End of digitization marked by last sample converted (save conversion time for non rail-to-rail signals)
  - Each channel can use internal self trigger (not all channels need to be activated at the same time)
- **“ROI mode”**:
  - Even with global triggering, if so desired, only snippets of observation window (32-2k samples) will be marked, digitized and output
  - Very effective zero suppression for signals over threshold
- **Trigger flexibility**:
  - Each threshold is individually configurable
  - Trigger is exported via serial interface to form basis for global triggering to cut on accidentals
- **“Window Level Control”**:
  - Mechanism to permit continuous storage during processing of previous triggers
  - Orthogonal to other modes (i.e. ROI, self triggering)
  - Permits operation at instantaneous rates higher than maximum sustainable rate
- **Pipelining** mechanisms to speed up rate (e.g. data in transmit buffer while new data gets packetized)

HDSoC Rev. 2 - I/O and Fabrication

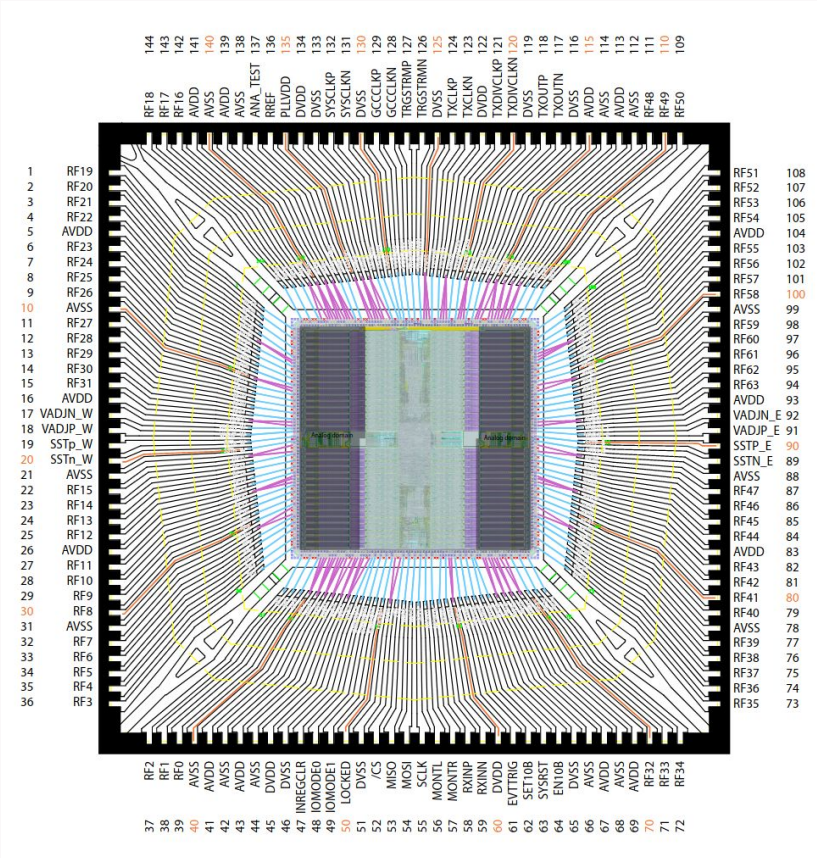
Overall I/O organization:

- Left/Right sides:
  - 32 analog inputs per side (5+5 on top/bottom)
  - Reference voltages for timing generators
- Top/Bottom:
  - Configuration I/Os:
    - Serial input
    - SPI-like interface
  - Clock references
    - Can select between PLL or externally provided
  - Some static configurations:
    - Selection of serial interface (raw 8 bits/parity encoded 10 bits/8b10b encoded)
    - Selection of configuration mode (serial/SPI)



Bonding diagram and packaging

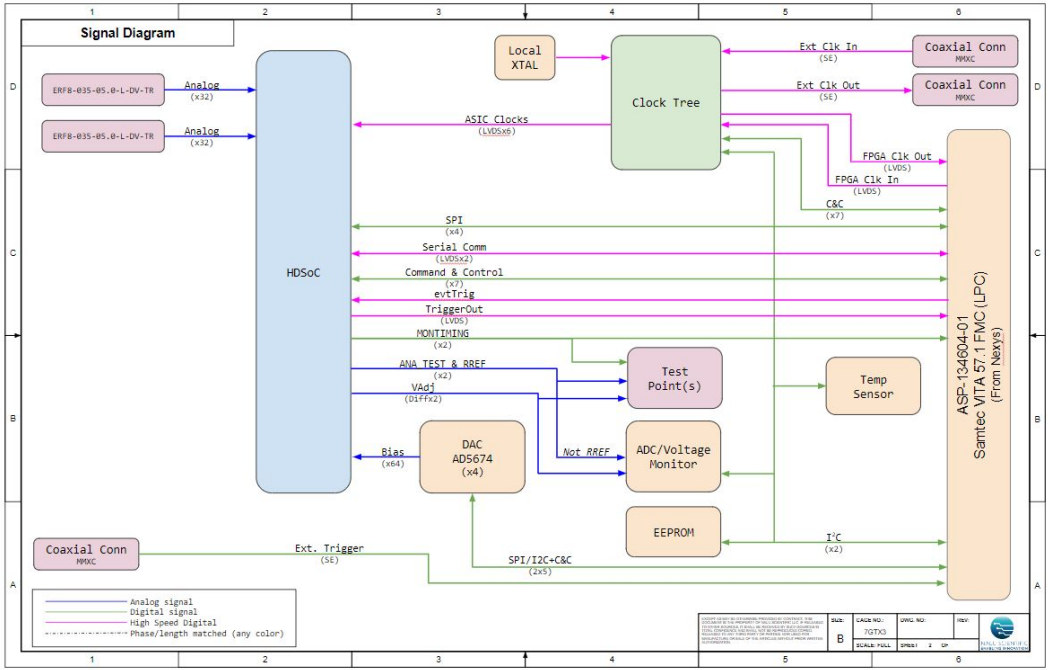
- All I/Os bonded:
  - Pull-ups for leaner bonding (custom packaging) possible (e.g. configuration)
- Double bonds for power whenever possible
- Fits in same package as V1:
  - TQFP-144 - 20 mm side



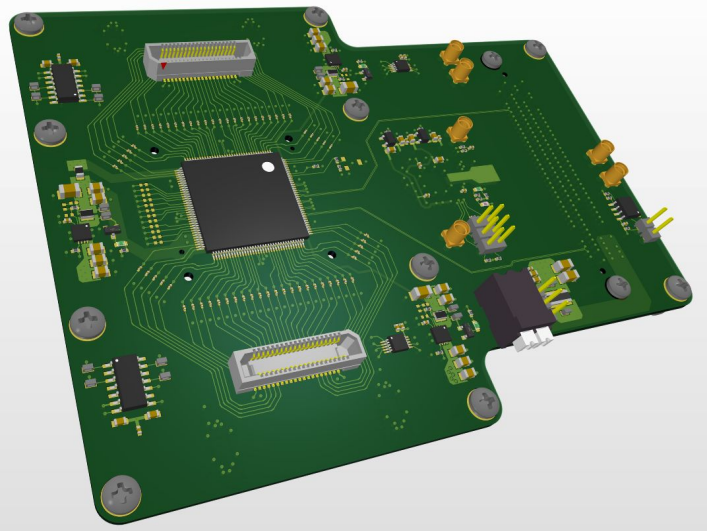
Evaluation Board Design

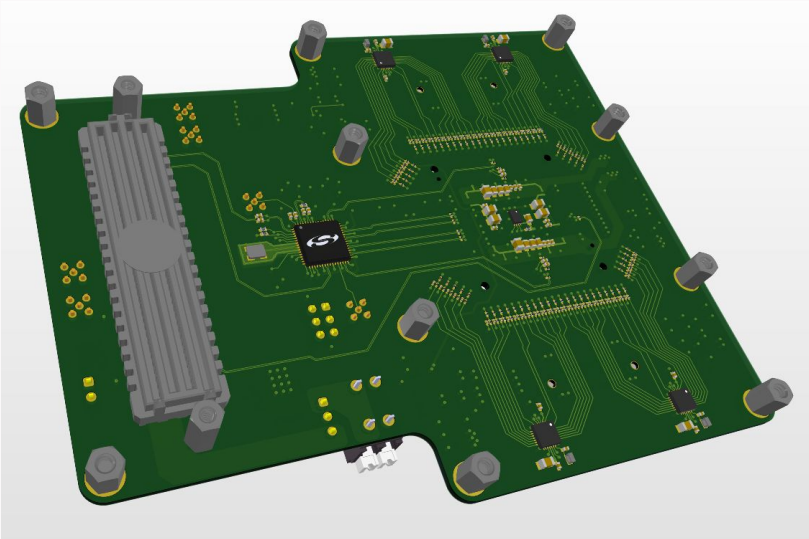
To provide full testing coverage:

- Accurate reference clock generation:
  - Input for external reference
  - Output for triggering synchronization
- External trigger input
- Temperature sensor
- Connection to SiPM array or standalone input signals
- Reference voltage to all channels for standalone biasing
- Traditional serial and SpI interface
- Interface to off-the-shelf FPGA readout board (FMC standard connector)



HDSoC V2 - EVB





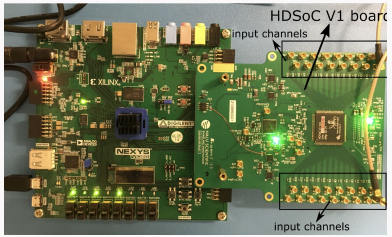
Pulse difference resolution

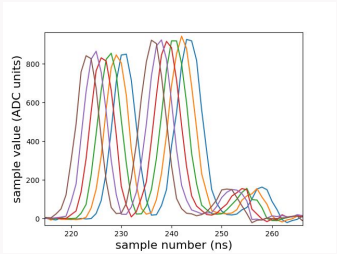
Experimental setup:

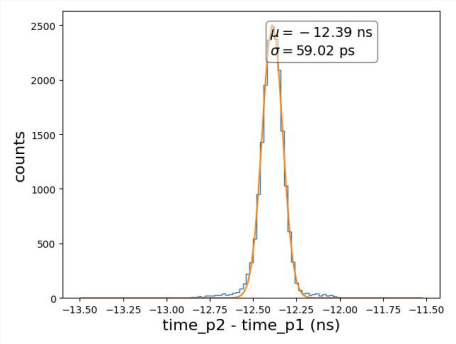
- Evaluation HDSoC board operating at 1 Gsps
- Rigol DG4162 sto generate a short pulse - uncorrelated with digitizer clock
- Pulse is split into two pulses with ~12 ns delay between them.
- The combined signal is connected to channel 0 of HDSoC.

Data taking and Analysis

- Data collected for large number of events
- Data is timing calibrated using a simple calibration algorithm
- Histogram of the difference in timing between the leading edges of the two pulses was estimated
    - Large pulses permit a much finer resolution than the sampling rate with ~60ps standard deviation

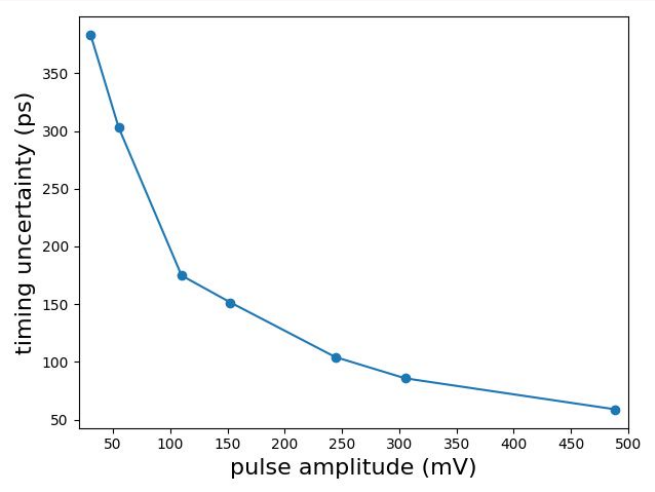






HDSoC V1 - Timing Resolution as a Function of SNR

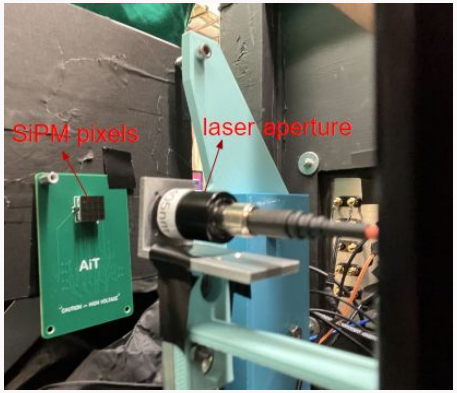
- Uncertainty in timing estimate increases with as the pulse height decreases
- A scan for different pulse amplitude was performed:
- 59 ps at 500 mV pulse height
- 383 ps at 30 mV pulse height

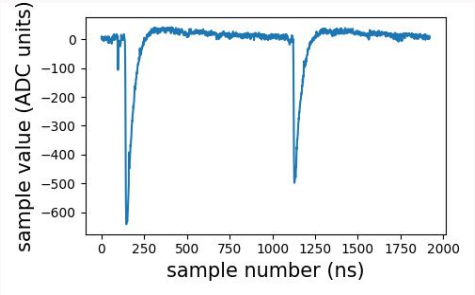


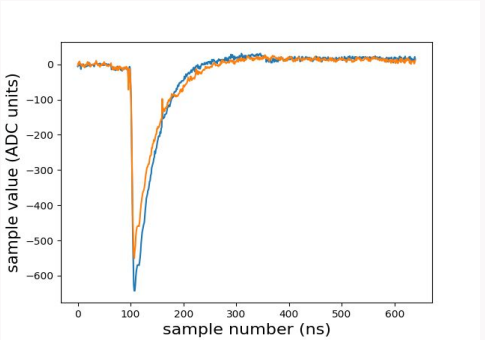
Laser-induced SiPM pulse timing

Setup:

- A PILAS DX laser diode module in a dark box to generate photons at a repetition rate of 1 MHz.
- Aperture of the laser output was set up to point at one pixel of an Onsemi J-Series 4x4 array of 3 x 3 mm^2 SiPMs
- Another set of experiments illuminated 2 pixels at the same time
- An AiT Instruments amplifier board was used to amplify the signals produced by the first pixel of the SiPM array before connecting it to channel 0 and 1 of HDSoC.







SiPM PULSE MEASUREMENTS

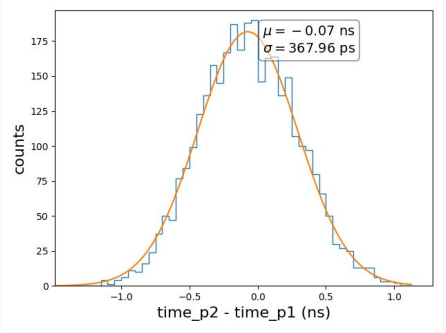
Pulses on same channel:

- 1 us is still within the full record length so time estimate could be performed
- Same-channel result show uncertainty of ~360ps
- It is believed that uncertainty is due to the accuracy of the laser rate control.

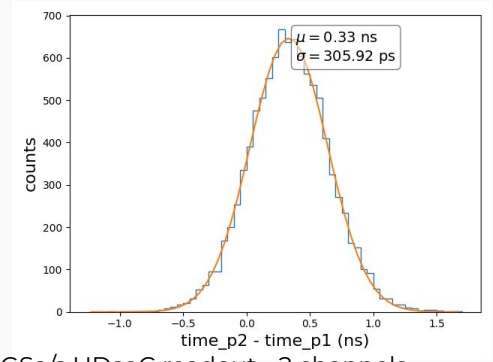
2-channel experiments:

- For the cross channel results, an relatively large timing uncertainty of 306 ps was observed.
- To verify, measurements on the same setup with a 2Gsps oscilloscope was performed and showed similar accuracy.

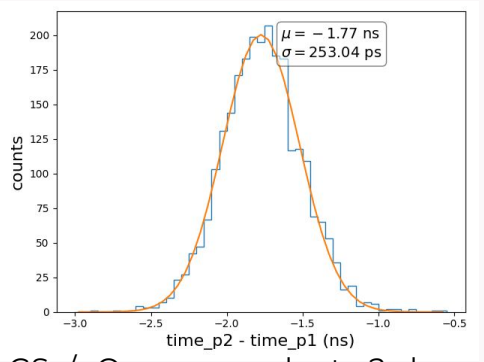
Work in Progress: We are trying to troubleshoot the setup.



HDsoC readout - pulses 1 us apart



1 GSa/s HDsoC readout - 2 channels

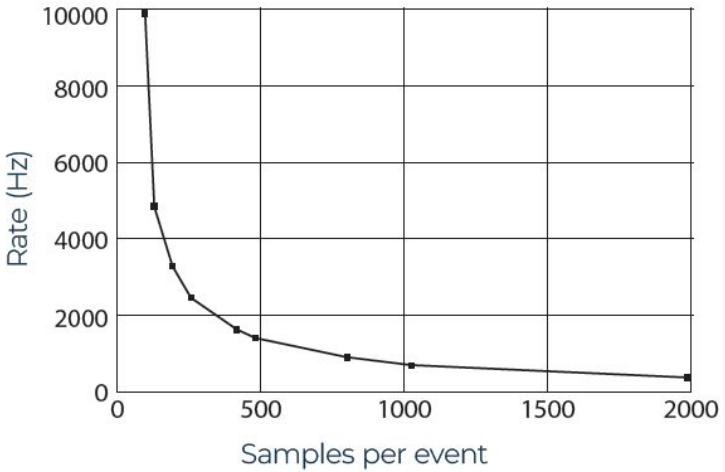


2 GSa/s O-scope readout - 2 chann

HDSoC V1 - RATE MEASUREMENTS

Trigger Rate with Gigabit Ethernet

We implemented the Gigabit ethernet module in the firmware to read out data. It significantly improved the data throughput of the DAQ system, which in turn improved the acquisition rate handling of the digitizer. Right shows the trigger rate as a function of record length for a pulse with a repetition rate 10 KHz; record length is expressed in number of samples (collected for all 32 channels), from 96 to 1984. We were able to digitize at the rate of more than 2 KHz for the record lengths of less than 10 windows (320 ns).



Events digitized for a 5s data acquisition as a function of record length. The record length is given in the terms of windows, where 1 window = 32 samples.

HDSoC Conclusions and future work

Status of HDSoCv2:

- Full channel coverage
- Timing range
- Power reduction mechanisms
- Crosstalk-aware placement and power routing
- SPI-like interface
- Final chip designed, fabricated and packaged
- Evaluation board being sent out for fabrication

Future work:

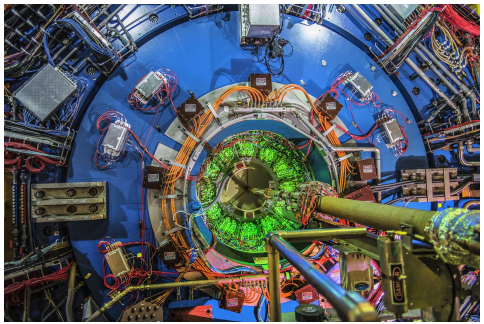
- Individual channels assessment (bypassed TIA)
- TIA assessment (standalone and with channel readout)
- Power trimming
- Rate measurements
- SiPM readout

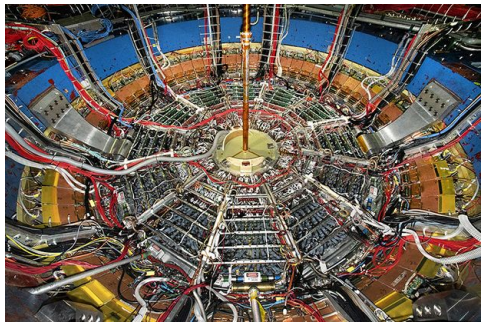
Compact Data Acquisition Module - Benchtop

NALU SCIENTIFIC
ENABLING INNOVATION

Product Name: **DSA C10-8+**
Product Description: 8 channel, 10 GSa/s digitizer with built-in amplifier
Dimensions: ~ 6” x 4” x 1”
Gain: 19.5dB, replaceable
Bandwidth: ~1.8 GHz
Digitizer Chip: AARDVARC V3
Data: USB/UART, Gb Ethernet (UDP)
Integration: Amps, chip, FPGA, clock, regulators, comm, FW, SW
Trigger: Internal, External, Software

Designed and vertically integrated at Nalu Scientific
Under evaluation for Electron Ion Collider at Brookhaven Lab
Available for sale via distribution partner (CAEN)



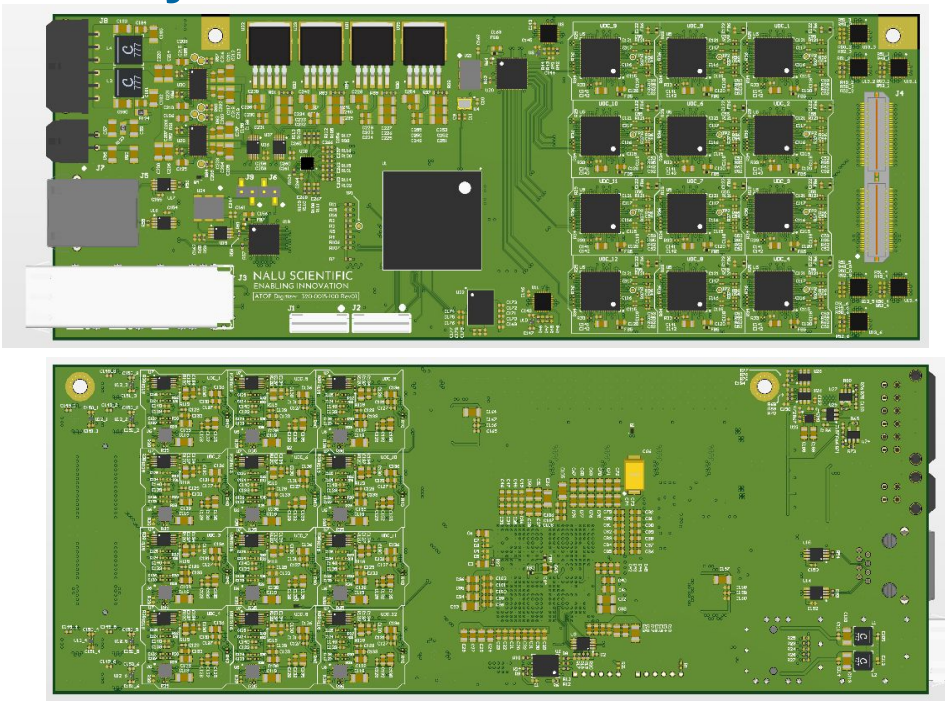


Funded by DOE Phase I/II SBIRs

48 ch ASOC based Readout for ALERT ATOF

Other applications for NP - under fab/assy at Nalu

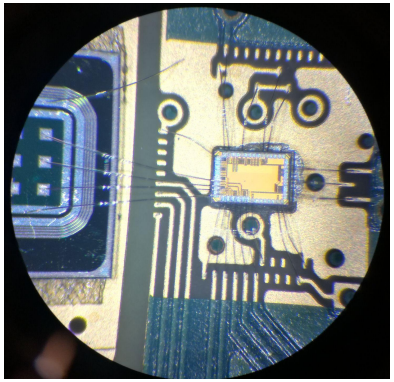
- Upgraded high luminosity ALERT
  - ATOF would require more front-end processing with feature extraction
  - Only possible with ASOC (not possible with petiroc2A)
- EIC Detector R&D
  - Readout for prototype SciFi EM calorimeter proposed EPIC detector
  - Readout for other detectors for EIC: MCPPMT with timing
- SOLID Detector
  - Could provide readout of MAPMTs for Cherenkov system
  - Could help prototype large angle EM calorimeter
- Engineering investment – Readout System architecture (backend) can be reused with different frontend ASICs
  - Quickly standup new applications/experiments
  - Faster digitizer, higher channel densities, etc.



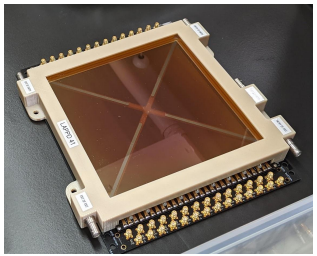
Summary

- **Products:**
  - Digitizer microchips
  - Hardware integration
  - Firmware and software
- **Services:**
  - Custom chip/HW design
  - Software and firmware design
  - Custom readout system development
  - Prototyping
- **Expertise:**
  - Electronics engineering
  - Radiation detection
  - Integration and testing
- **Collaborations:**
  - National Labs/ FFRDCs
  - Universities
  - Large Scientific Experiments

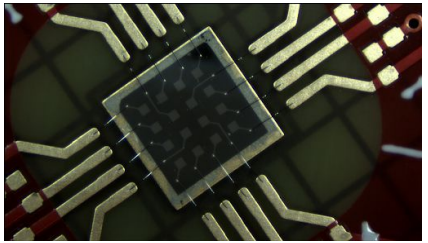
CAEN Technologies Inc.



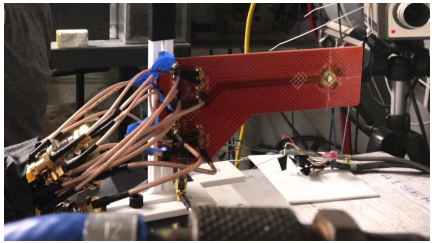
AC-LGAD readout

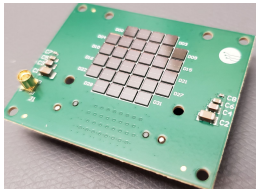


Large Area Photodetectors



Diamond detector





SiPM Arrays

Advanced Sensor Integration

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