Readout Electronics for LGAD Detectors

Streaming Readout Workshop XI (11/28-12/2/2023)

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Readout Electronics for CMS ETL (LGAD)
 Readout Electronics for ePIC TOF (AC-LGAD)
 With a focus on frontend readout ASIC

Low Gain Avalanche Diode (LGAD)

ATLAS and CMS experiments will be equipped with **precision timing detectors** based on **Low Gain Avalanche Diode** to suppress pile-up and identify low-momentum particles at HL-LHC





E field Traditional Silicon detector

Ultra Fast Silicon Detector E field









CMS ETL



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• fluence at 3 ab⁻¹: $\sim 2x10^{15} n_{eq}/cm^2$

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per track: <50 ps per hit $\rightarrow <35$ ps per track

ETL Readout Chip (ETROC) - Fermilab



- Delicate balance act from:
 - Low noise & fast rise time (~0.5 ns)

$$\sigma_{jitter} \sim \frac{e_n C_d}{Q_{in}} \sqrt{t_{rise}} < 40 \ ps$$

- Power budget: 1 W/chip, ~4 mW/channel
- ETROC innovation:
 - Very low power TDC using simple delay cells with self-calibration



- ✓ ETROC0 : single analog channel
- ✓ ETROC1: with TDC and 4x4 clock tree
- ✓ ETROC2: 16x16 full size full functionality
- **ETROC3:** 16x16 preproduction chip

ETROC - Fermilab



- Analog front-end only
- Wire-bonded with LGAD sensor reached ~33 ps time resolution per hit with preamp. waveform at room temp.
- Passed 100 Mrad TID

12/2/2023

arXiv:2012.14526

- Added low-power TDC and 4x4 H-tree for clock distribution
- TOA bin size: ~20 ps achieved
- TOT bin size: ~40 ps achieved
- Bump-bonded with LGAD sensor reached ~42 ps time resolution per hit with TDC data

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- First full-size chip (16x16) with all desired functionalities included
- All analog blocks silicon-proven; all digital blocks were verified in FPGA emulator
- Performance under study





Diagnostic RO: continuous readout at 1.28 Gbps **Simple RO (not shown)**: triggered readout mode

ETROC TDC design optimized for low power

• A simple delay line without the need for DLL's to control individual delay cells, with a cyclic structure to reduce the number of delay cells, to measure both TOA and TOT at the same time.

In-situ delay cell self-calibration technique

- For each hit, use two consecutive rising clock edges to record two time-stamps, with a time difference of the known 320 MHz clock period for self-calibration.
- Crucial to reach the required precision using a tapped delay line with uncontrolled delay cells (thus lower power) 12/2/2023 Zhenyu Ye @ LBNL/UIC



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ETROC2 Submitted in Oct. 2022, Received in Apr. 2023

New in ETROC2 compared to ETROC1

- Shift readout clock among pixels; extra shielding
- Fast command
- Phase-Locked Loop (PLL)
- Waveform sampler

- L1 Buffer
- eFuse
- Temp sensor





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- \checkmark I2C communication to global circuit and individual pixels
- \checkmark Automatic threshold calibration; Phase-Locked Loop; Fast command
- \checkmark Digital readout with pattern generator
- \checkmark Initial check on power consumption; detailed study will follow
- ✓ Initial test of ETROC2 with charge injection, infrared laser, and beam test in 9/2023 (SPS), more beam tests in 12/2023-6/2024 Initial waveform sampler test done; detailed check on-going
- \checkmark Initial wafer probe test; planned for production QA/QC
- \checkmark Initial total irradiation dose (100 Mrad) test; detailed check on-going
- Single Event Upset test planned



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CMS ETL - Service Hybrid



- Service Hybrid is an assembly of two PCBs, a Power Board and a Readout Board, servicing up to 12 modules.
- **Power Board** distributes low voltages provided by power supplies to ETROCs, slow control adapter chip (SCA), lpGBT, and VTRx+. The voltages are regulated by radiation hard and B-tolerant **DC-DC converters** on the board.
- **Readout Board** receives and distributes via **SCA**, **lpGBT** and **VTRx**+ fast and slow control signals to ETROCs, and route data and monitoring information from ETROCs to backend DAQ.

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CMS ETL - Readout and Power Boards

- Prototype V2 readout board
 - LpGBTv1+VTRX



- Prototype V2 power board
 - Efficiencies ~ 65-67%



- First system test with bare ETROC2 on the first functional module PCB successful;
- Full demonstration rely on complete system test





AC-coupled Low Gain Avalanche Diode (AC-LGAD)

AC-coupled LGAD provides both precise timing and spatial resolutions, with ~100% fill factor. Good candidate for **4D trackers** at future high energy experiments, e.g. EIC, HL-LHC, FCC.



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Electron Ion Collider (2031+)

EIC among the highest priority of US Nuclear Physics

- **High luminosity**: $L = 10^{33} 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, 10–100 fb⁻¹/year
- **Highly polarized** electron and light ion beams: ~70%
- Large center of mass energy range: $E_{cm} = 20-140 \text{ GeV}$
- Large ion species range: proton Uranium
- **Particle production rate**: O(5) @ ~500 kHz





AC-LGAD Detectors for ePIC



	Area (m ²)	Channel size (mm ²)	# of Channels	Timing Resolution	Spatial resolution	Material budget
Barrel TOF	10	0.5*10	2.4M	35 ps	$30 \ \mu m \ { m in} \ r \cdot \varphi$	0.01 X ₀
Forward TOF	1.4	0.5*0.5	5.6M	25 ps	30 μm in x and y	$0.05 X_0$
B0 tracker	0.07	0.5*0.5	0.28M	30 ps	20 μm in x and y	0.05 X ₀
RPs/OMD	0.14/0.08	0.5*0.5	0.56M/0.32M	30 ps	140 μm in x and y	no strict req.

Requirements on timing and spatial resolutions and material budget are still being evaluated and are subject to change as the design matures, and we will continue to explore common designs for these detectors where possible to reduce cost and risk.

Frontend Readout ASIC

- R&D Goals
 - 15-20 ps jitter with minimal (1-2 mW/ch) power consumption, match AC LGAD sensors for ePIC.
- Plan
 - Utilize the design and experience in ASICs for fast-timing detectors from ATLAS and CMS, and investigate common ASIC design and development for TOF and FF.



EICROC by Omega/IJCLab/Irfu/AGH

- Preamp, discri. taken from ATLAS ALTIROC
- I2C slow control taken from CMS HGCROC
- TOA TDC adapted by IRFU Saclay
- ADC adapted to 8bits by AGH Krakow
- Digital readout: FIFO depth8 (200 ns)



FCFD by Fermilab (this talk)

- Adapt the Constant Fraction Discriminator (CFD) principle in a pixel paired with a TDC, one time measurement gives the final answer.
- Charge injection consistent with simulations: ~30 ps at 5 fC, and <10 ps at 30 fC
- Tested with laser, beta source and beam

Leading Edge vs Constant Fraction Discriminator



- Time cross the threshold of a LE discriminator dependent on signal amplitude
- Time cross the threshold of a CFD independent on signal amplitude with same signal shape



• CFD can be realized by adding the delayed signal and an inverted and scaled signal, and checking the zero-cross point

Leading Edge vs Constant Fraction Discriminator



Table 2

 $50 \ \mu m$ pre-radiation LGAD sensor simulation: summary of best time resolution obtained for SNRs of 20, 30, and 100. Leading edge and constant fraction results are shown. The measured time resolutions have statistical uncertainty below 5%.

	Time resolution (ps)								
	Leading edge			Constant fraction (Ideal)					
ST (ns)	SNR = 20	SNR = 30	SNR = 100	SNR = 20	SNR = 30	SNR = 100			
0.5	38	35	29	37	35	30			
1.0	45	37	29	36	33	26			
2.0	63	48	31	48	34	29			
4.0	103	75	38	74	55	32			

Fermilab CFD ASIC v0 (FCFDv0)



- A Constant Fraction Discriminator ASIC for LGAD detectors is being developed at Fermilab
- First version (FCFDv0) with single channel analog frontend only has been extensively tested with internal charge injection, infrared laser, beta course, and 120 GeV protons.

FCFDv0 with Internal Charge Injection



- Jitter is smaller than 20 (10) ps for charge > 10 (20) fC
- Mean TOA changes by less than +/-10 ps for 3-26 fC charge

FCFDv0+LGAD with Infrared Laser and Beta Source







- Timing resolution obtained with infrared laser: around 25 (15) ps for signal ~10 (20) fC
- Timing resolution obtained with beta source ~35 ps, close to the best that the LGAD sensor provides

FCFDv0+LGAD with 120 GeV Protons



Timing resolution obtained with 120 GeV protons is around 35 ps, close to the best that the LGAD sensor provides

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Summary and Outlook

- On-going efforts to develop front-end readout ASICs for precise timing detector based on LGAD and 4D trackers based on AC-LGAD.
- Full-size full-functionality ETROC prototype for CMS ETL under intensive testing.
 - The ASIC functions as expected and no major problem found.
 - Charge injection, infrared laser, initial beam and TID tests completed
 - Additional beam and SEU tests scheduled in the coming months.
 - Submission of the next version for engineering run is anticipated in late 2024.
- Frontend ASICs (EICROC, FCFD) being developed for EIC AC-LGAD detectors
 - Excellent performance of FCFDv0:
 - Jitter less than 20 (10) ps for injected charge > 10 (20) fC;
 - Mean TOA changes by less than +/-10 ps for injected charge between 3-26 fC;
 - Timing resolution when ASIC is connected to a LGAD sensor is around 35 ps for MIP particles.
 - A new version FCFD with larger number of channels (FCFDv1) submitted in August 2023.
- Other electronics also under development for CMS ETL (triggered) and EIC AC-LGAD (SRO).

High-Luminosity LHC



The HL-LHC will have x3-4 instantaneous and x10 integrated luminosity, requiring **detector upgrades** to

- deal with enhanced pileup interaction and radiation damage levels at the HL-LHC
- improve the experiment for better discovery potential and/or measurement precision



Role of Precise Timing at HL-LHC



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time [ns]



BTL: LYSO bars + SiPM

- $|\eta| < 1.45$; ~38 m²; 332k channels
- fluence at 3 ab^{-1} : $2x10^{14} n_{eq}/cm^2$

This talk: ETL: Si with internal gain (LGAD)

- $1.6 < |\eta| < 3.0; ~14 \text{ m}^2; ~8.5 \text{M}$ channels
- fluence at 3 ab⁻¹: $\sim 2x10^{15} n_{eq}/cm^2$

LGAD+ETROC0 – Test Beam Results





ator

- Our setup
 - Independent scintillator provides trigger
 - Telescope provides proton track
 - Oscilloscope saves waveforms
 - Study Δt(LGAD,MCP)

Cold box

LGAD boards MCP (Photek) on cooling blocks time reference





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ETROC1: 4x4 Pixels

Designed to be bump-bonded with 5x5 LGAD sensor







Submitted in Aug. 2019, Received in Dec. 2019

New in ETROC1 compared to ETROC0

- **TDC**: new design optimized for ETROC low power consumption
- I2C (SPI in ETROC0): silicon proven IP from CERN
- **Clock distribution**: 4x4 H-tree distribution (a subset of 16x16)

Overall expected ETROC performance



Power consumption

Circuit component	Power per channel [mW]	Power per ASIC [mW]	
Preamplifier (low-setting)	0.67	171.5	
Preamplifier (high-setting)	1.25 – All confirmed	320	
Discriminator	0.71	181.8	
TDC	0.2 - achieved 0.1mW	51.2	
SRAM	0.35	89.6	
Supporting circuitry	0.2	51.2	
Global circuitry		200	
Total (low-setting)	2.13	745	
Total (high-setting)	2.71	894	

With some safety margin: design specification is ~ 1W per chip

LGAD+ETROC1 – Test Beam Results







LGAD+ETROC1 resolution is 42-46 ps from TDC digital outputs

$$\sigma_{i} = \sqrt{0.5 \cdot \left(\sigma_{ij}^{2} + \sigma_{ik}^{2} - \sigma_{jk}^{2}\right)}$$

LGAD+ETROC2

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LGAD+ETROC2



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Electron-Proton and -Ion Collider detector (ePIC)



AC-LGAD Detectors for ePIC

• Low-Q² tagger



AC-LGAD Detectors for ePIC

Tracking and Vertexing:

- MAPS
- MPGD

PID:

- AC-LGAD TOF (also for tracking)
- hpDIRC
- pfRICH
- dRICH

EMCal:

- PbWO EEMCal
- Pb/SciFi Barrel EMCal with Imaging
- W/SciFi FEMC

Hadronic Calorimeter

- Fe/Sc Backward HCAL
- Barrel HCal (sPHENIX re-use)
- Fe/Sc&W/Sc LFHCAL

Far-For/Backward

- Roman Pots/B0 Tracker/OMD
- Zero Degree Calorimeter
- Luminosity Tracker/Calorimeter

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• Low-Q<sup>2</sup> tagger
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AC-LGAD Detectors for TOF PID



AC-LGAD Detectors for TOF PID



AC-LGAD Detectors for Tracking



• BTOF with a spatial resolution of 30 μ m improves momentum resolution at high p

• TOF helps track reconstruction by rejecting beam background and pileup hits in Si-MAPSs

AC-LGAD Sensor

- Sensors with different configurations produced by BNL-IO and HPK, and tested with 120GeV protons
- Prototype strip sensors with \sim 35 ps time resolution and <15 um spatial resolution.
- Prototype pixel sensors with ~ 20 ps time resolution and $\sim 20^*$ um spatial resolution.

* \sim 50 um under metal electrodes. To be improved

Position

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-0.6

-0.4

-0.2

Fermilab Test Beam Setup



HPK Strip Sensor (4.5x10 mm²) HPK Pixel Sensor (2x2 mm²)





HPK_W11_22_3_20T_500x500_150M_C600, 116V resolution [µm] 0 08 09 Position resolution observed 70F Time resolution : multi-channel 60 50 30 20

Ω

0.2

0.4

Track x position [mm]



0.6

bs

Centimeter-Scale AC-LGAD Sensors

First results from 1-cm long 500-um pitch strip sensors from BNL were encouraging [1]



- Metal electrode width: 50 vs 100 um
- Active Si thickness: 20 vs 50 um





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Fermilab Beam Test with 120 GeV Protons

Reference Detectors

- 5 pairs of Si strip and 2 pairs of Si pixel planes: 5 um spatial resolution
- 1 Photek MCP-PMT: 10 ps timing resolution

DUT (AC-LGAD @ 20 °C)

- Signals amplified by two GALI-S66+
- Waveforms recorded by Lecroy Waverunner 8208HD (2 GHz, 10GS/s)



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Interpad HPK 2

Position Measurement

- Sensor efficiency to have a signal in at least one strip is ~100% with most of the hits having signals from two strips.
- Hit position perpendicular to strip (x) is reconstructed from leading strip signal fraction $f=a_1/(a_1+a_2)$
 - Two strip $(0.5 \le f \le f_{\text{thres}})$: leading strip center $\pm x(f)$
 - One strip $(f \ge f_{thres})$: leading strip center
- Spatial resolution in x: 12-16 um





Timing Measurement

- Signal arrival time at wire-bonds depends on the hit distance to the wire bond due to finite signal propagation speed along electrode: ~5 cm/ns
- This effect can be corrected using the hit position from external tracker.
- For hits with signals in two strips, TOAs are combined $t_{reco} = \frac{1}{2}$

Before delay correction:45 - 55 psAfter delay correction:35 - 44 psAfter combining TOAs:34 - 35 ps





 $a_1^2 t_1 + a_2^2 t_2$





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Varying n+ Resistivity and AC-coupling Capacitance



- Increasing n+ layer resistivity reduces signal sharing, and thus increases signal amplitude.
- Little effect from varying the AC-coupling capacitance.

Varying Sensor Active Silicon Thickness



$$\sigma_t^2 = \sigma_{sensor}^2 + \sigma_{jitter}^2 + \sigma_{TDC}^2 + \sigma_{clock}^2 + \sigma_{walk}^2$$

 σ_{sensor} : Landau fluctuation in energy deposition in the sensor. It gets smaller with thinner sensors

 σ_{iitter} : contribution from frontend electronics

$$\sigma_{jitter} \sim \frac{e_n C_d}{Q_{in}} \sqrt{t_{rise}}$$

Decreasing active Si thickness for 1-cm long 500-um pitch strip HPK sensor from 50 to 20 um degrades the timing and spatial resolutions due to reduced signal amplitudes (and higher capacitance).

Fermilab Beam Test with 120 GeV Protons

Reference Detectors

- 5 pairs of Si strip and 2 pairs of Si pixel planes: 5 um spatial resolution
- 1 Photek MCP-PMT: 10 ps timing resolution

DUT (AC-LGAD @ 20 °C)

- Signals amplified by two GALI-S66+
- Waveforms recorded by Lecroy Waverunner 8208HD (2 GHz, 10GS/s)



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Interpad HPK 2