# Timing Synchronization System for the ePIC DAQ

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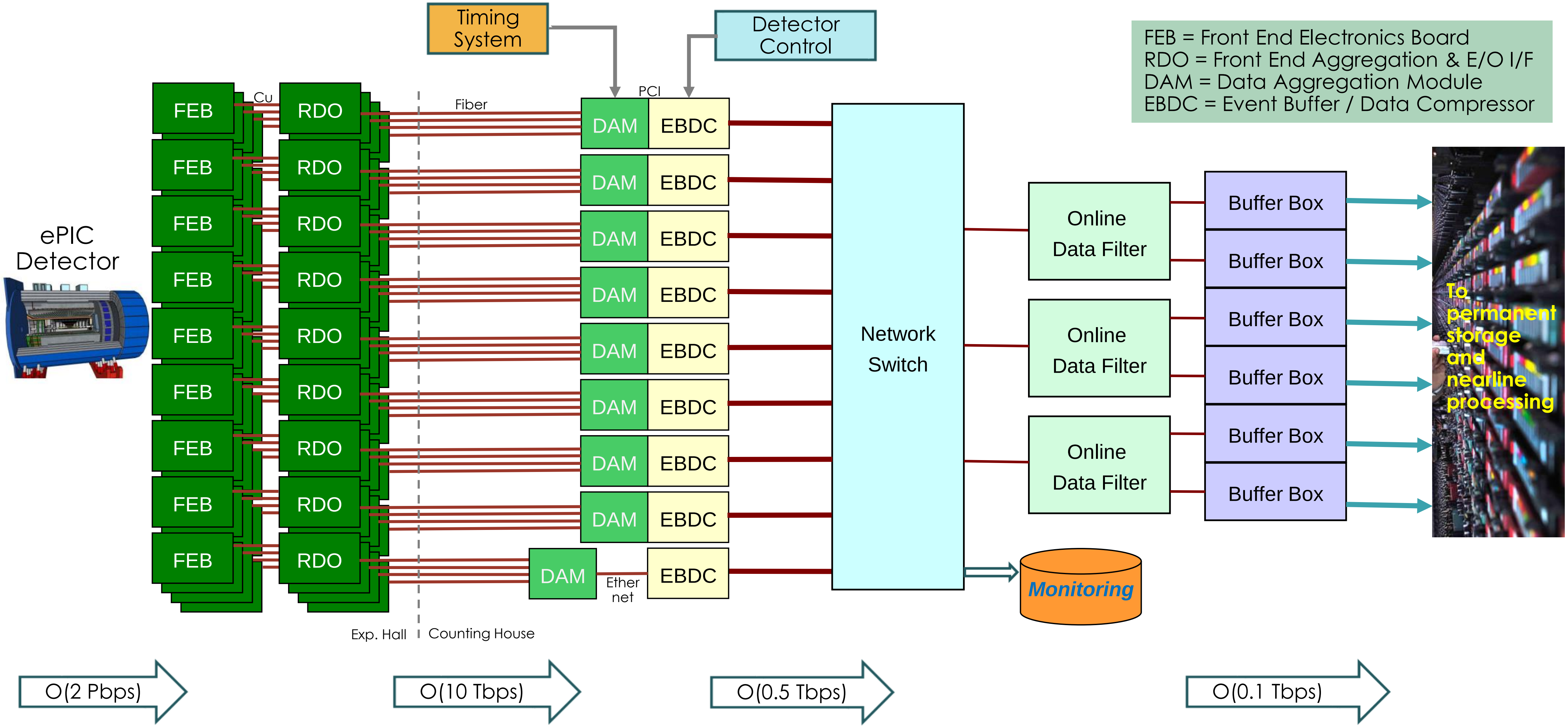
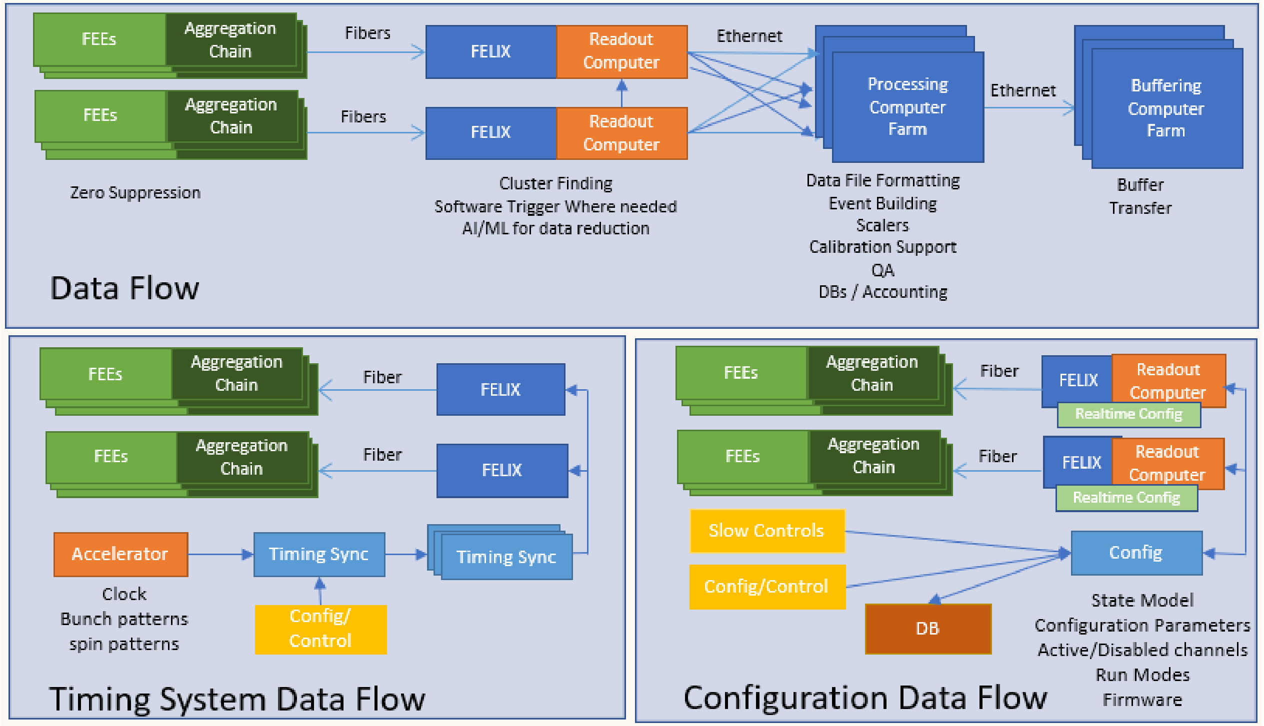
# ePIC Streaming DAQ



# ePIC Timing System

- The ‘Global Timing Unit’ board receives the accelerator clock plus any beam related information and fans this out via the DAM (FELIX) board
- The RDO boards use the reconstructed clock and the bunch crossing count (BX) from the transmitted data for digitization and synchronization, respectively
- Most detectors will need only a precision O(100ps), while some detectors (e.g. TOF) might need O(5ps)




- Where possible FEE ASICs should use the BX derived clock; where this is not possible, the RDO must provide sufficient information (drift measurements, phase differences, frequency differences) to allow time reporting in reference to the BX clock.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# ePIC Timing System Requirements

- Timing System must synchronize data between detectors. This requires a ~10ns resolution
  - 40m far forward and backward: ~135ns to calibrate
  - Need capability to set delays and monitor the synchronization
  - Absolutely critical if there is any sort of software trigger or filtering of data on one detector using info from another
- Timing System must provide high resolution 20ps phase stability to actual BX persisting over power cycles
  - Less than 100ps phase stability relative to EIC clock (possibly < 5ps jitter for TOF)
  - Account for transitive loading due to EIC acceleration (species/energy dependent phase correction)
  - Ability to set fine delays and monitor the synchronization
  - Implies higher resolution O(1ps) required between components
- Timing System is the only source for "real-time" global information
  - Rev-Tick (to identify bunch crossing 1 in each revolution)
  - 64bit unique bunch crossing ID (equivalent to 6k years, will never roll over in the lifetime of EIC)
  - Bunch structure
  - Spin State
  - Control zero-suppression, feature finding, AI/ML algorithms
  - Flow Control (start / stop / common busy)
  - Define time frames for packetization of detector data (protocol)
  - Fallback for handling hardware trigger for debugging, commissioning, handling specific detector problems (dRICH?)
  - FEE clock counter resets
- Possibly interleave with Slow Controls / Configuration data at DAM board level
  - All detectors need potentially complex configuration
  - Need real-time control for providing features like periodic raw data for checking bias
  - Need to monitor, and potentially adjust configuration in real time (pedestal drifts/hot channels/tracking failing electronics)
  - Automated power cycle / configuration recovery
  - AI/ML control of HV settings (to control gains, timing windows, phase shifts)



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# Timing System Components

- EIC Accelerator
  - 10ns (100MHz) bunch crossing rate
  - Interaction rates up to 500kHz
- EIC Clock System
  - Provided by the accelerator team
  - Interface to GTU board via fiber in the same room
- Global Timing Unit
  - Tree of boards splitting timing from EIC to O(100) DAM boards
  - Interface to DAM boards via fiber in the same room
  - Reads info from EIC clock system
  - Reads info from DAQ controls
  - User inputs from external systems
  - Transmits info to DAM boards
  - Possible feedback from DAM boards for flow control
  - Support for triggering (via input bits)
- DAM Boards
  - Accept and transmit timing info from GTU board set
  - Use timing input clock as clock for fiber transceivers
  - Use downlink also for detector control
  - ~5 – 10 Gbit/sec transfer speed
- RDOs
  - Accept timing protocol
  - Clock to FEE boards (ASIC) reconstructed from information stream from DAM boards
  - Format Data packets in appropriate time frames


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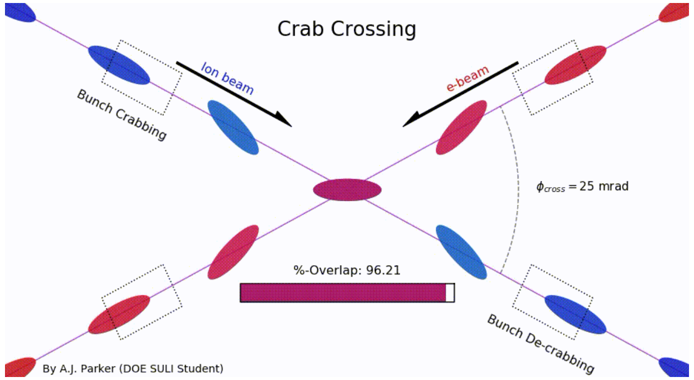
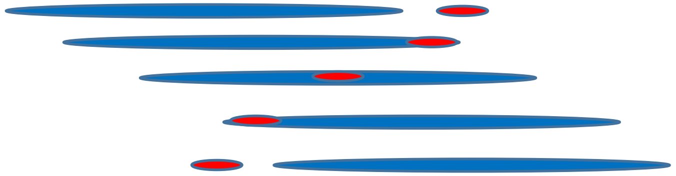
# EIC Beam Parameters (T. Satogata, JLAB/ODU):

- 1160 RF bunches, 98.5254 MHz beam crossing clock, 1015 ns gap (100 “no” bunches)
  - Clock originating from accelerator RF source, routed through the accelerator site to experiment
  - Clock has fixed frequency, without ramp variation
- Bunch spacing 10.150 ns
- Revolution period $T_{rev}$ = 12.7886 μs, dominated by electrons
  - Ion energies constrained to match $T_{rev}$, change orbit to match electron beam frequency

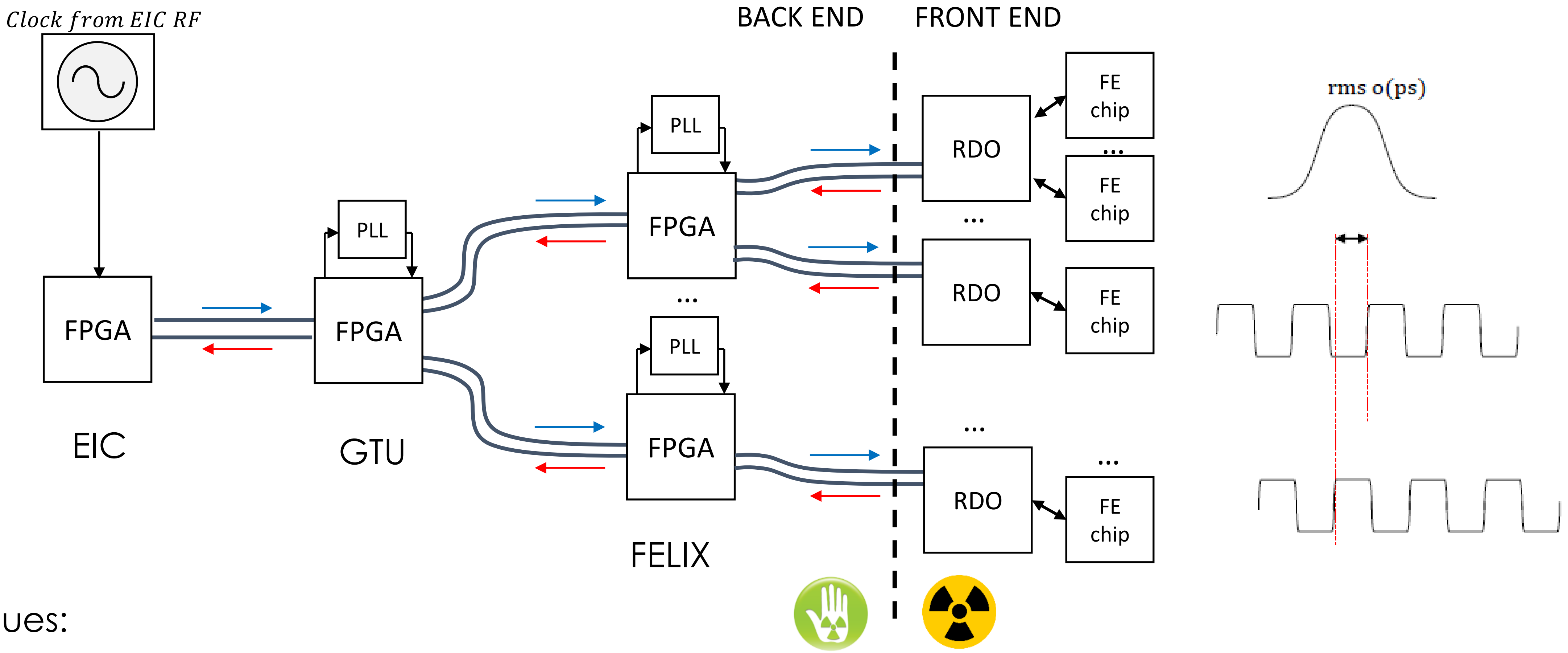
| | ESR | HSR |
|---|---|---|
| RMS bunch length $\sigma_z$ [mm/ps] | 7-9/23-30 | 75-60/250-200 |
| RMS momentum spread [$10^{-4}$] | 5.8-10.9 | 10.3-6.8 |
| RMS horiz beam size $\sigma_x$ [um] | 100-250 | |
| $\sigma_z/\sigma_x$ ratio [-] | 28-90 | 240-750 |




more like…



# Timing Distribution Concept




Issues:

- Jitter
- Wander – slow phase variations (temperature, power supply stability,…)
- Phase-determinism with resets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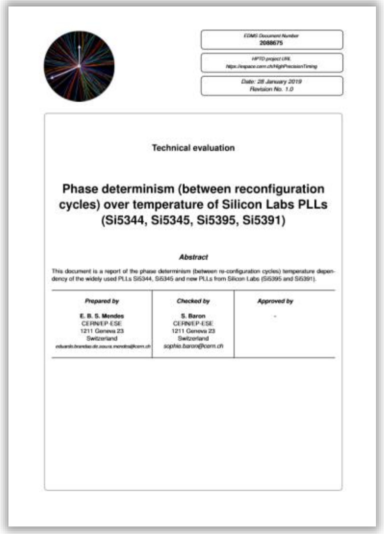
# Back-end COTS and CERN HPTD IP

- CERN started an R&D program to study the timing performance of the different components in a timing distribution system (FPGA, PLLs, LDO, …):
  - **H**igh **P**erformance **T**iming **D**istribution (HPTD) project
- Higher Phase-determinism for Xilinx Ultrascale FPGA Transmitters

Some results can be found here and IEEE TNS

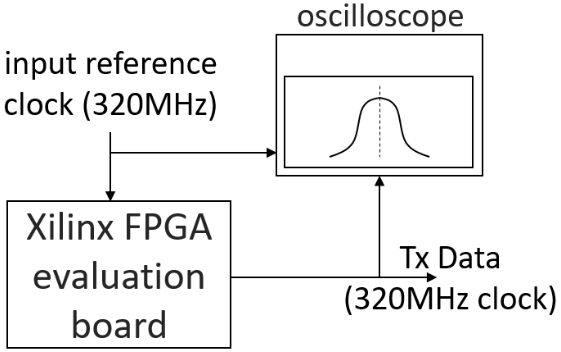


Technical evaluation

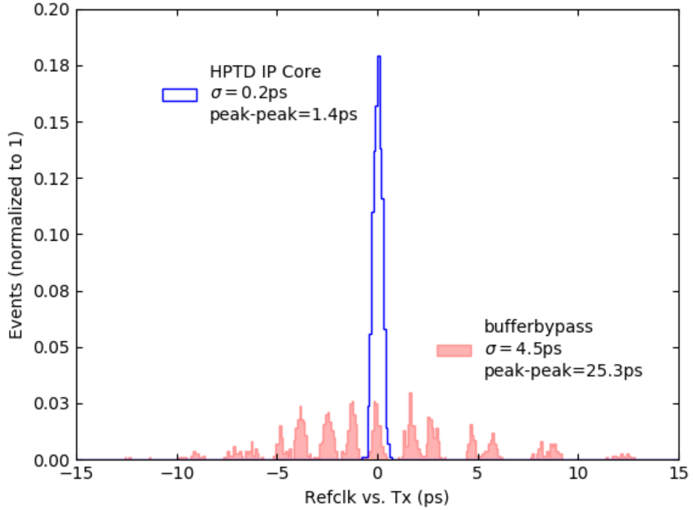
Phase determinism (between reconfiguration cycles) over temperature of Silicon Labs PLLs (Si5344, Si5345, Si5395, Si5391)

Abstract

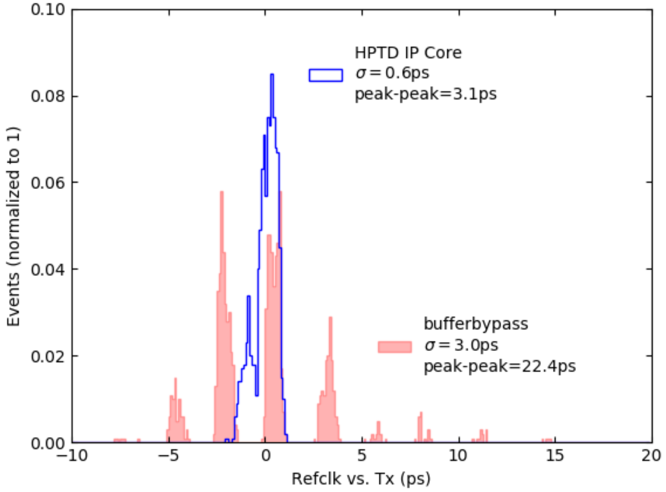
Transmitter Only:




GTH Ultrascale+

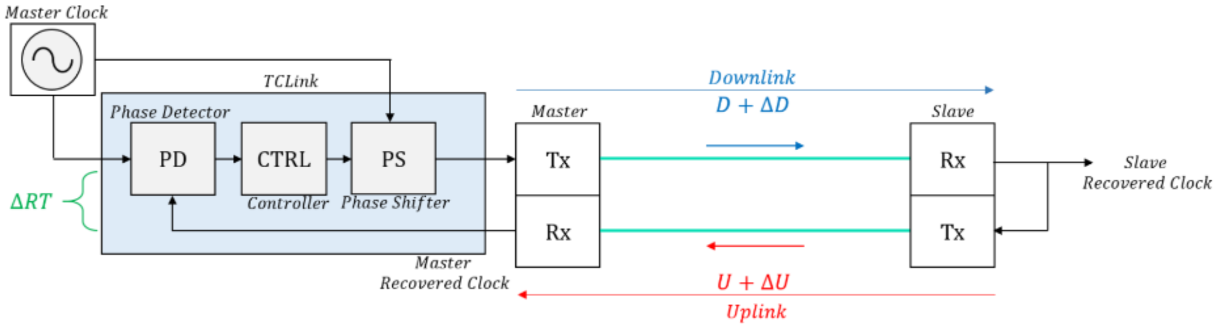


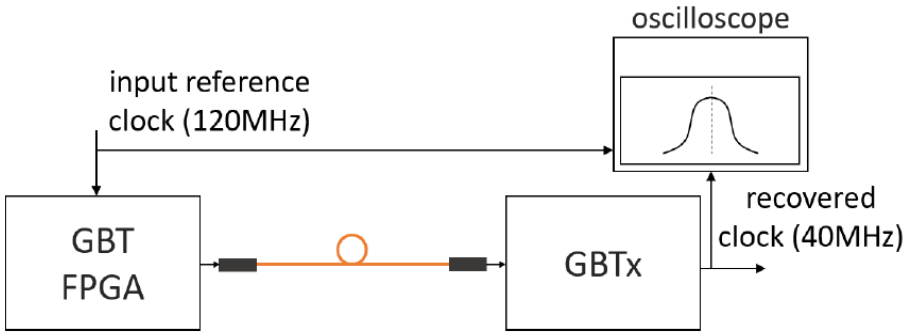

GTY Ultrascale+



# Timing Compensated Link (TCLink) with GBTx

- CERN developped an FPGA-IP to implement timing monitoring and compensation in FPGA-based links
  - Protocol-agnostic
  - Presented in TWEPP-19



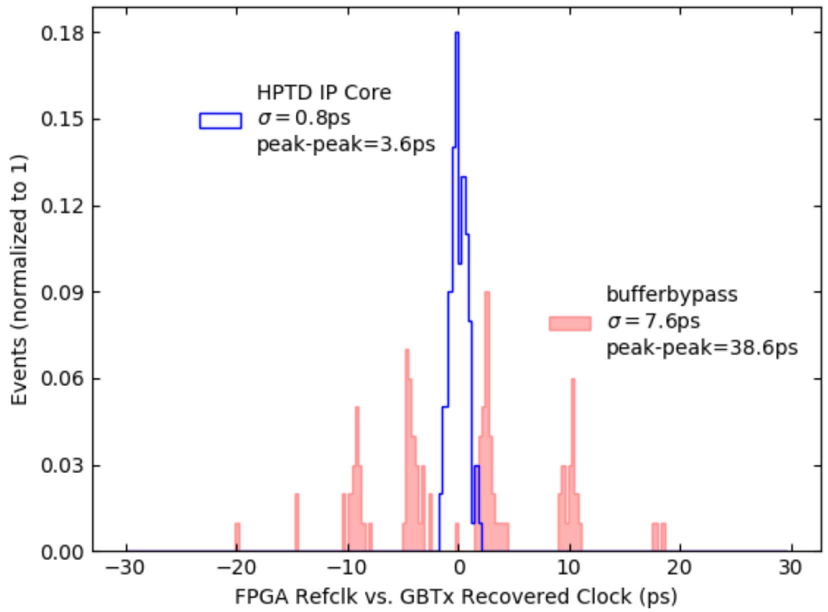
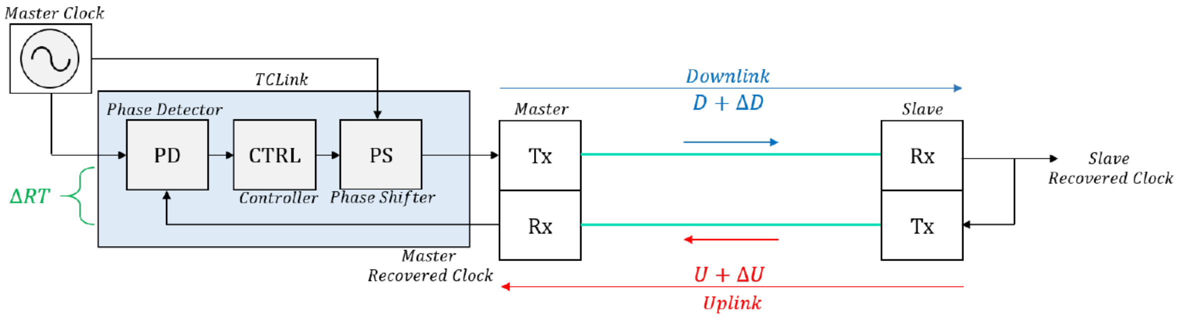
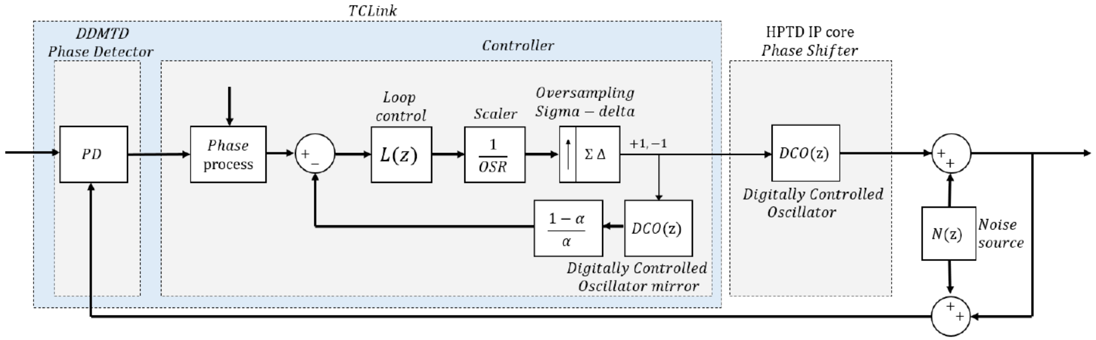



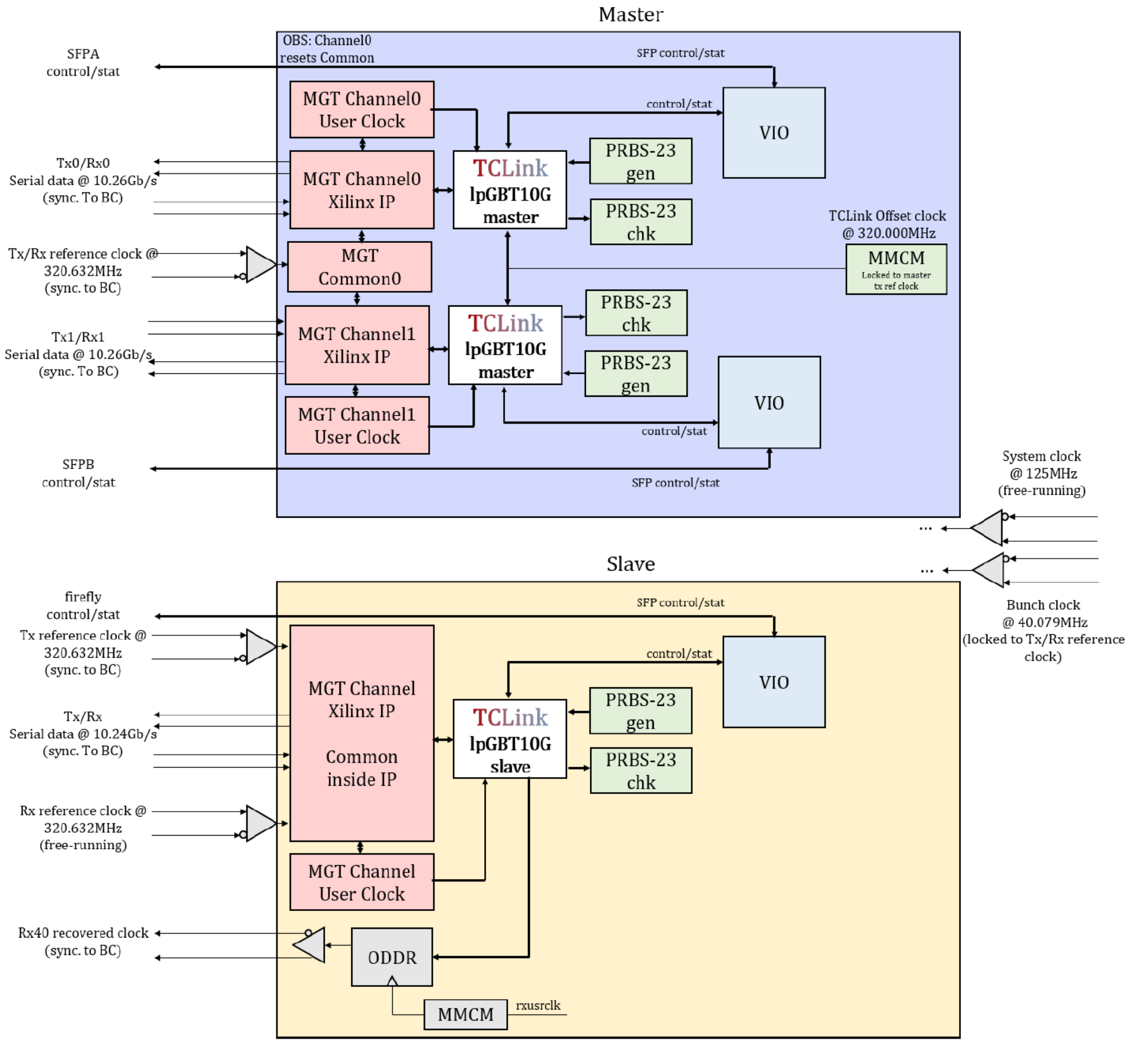

Fig. 8. Transmitter phase results for GTH Ultrascale-system tests with GBTx ASIC. Total number of events is 100.

# From the (HPTD) TCLink Reference Note:




- **Phase-detector:** The phase-detector used is the **Digital Dual Mixer Time Difference (DDMTD)** core created in the **CERN White-Rabbit** project (`https://ohwr.org/project/white-rabbit`). The **DDMTD** relies on a heterodyne mixing in order to perform a phase-measurement. Therefore, a third clock with a small frequency offset is necessary for the phase-measurement, it is recommended to use a clock from an external PLL for the mixing clock (the example design uses an internal MMCM for those purposes to ease the usage for a first approach with the core). It can have a resolution of $o(ps)$.
- **Controller:** Digital controller using sigma-delta modulation and capable of mirrorring the control plant in order to emulate different $\alpha$ coefficients.
- **Phase-shifter:** The phase-shifter used is the **HPTD IP** core created by the **CERN HPTD** project (`https://gitlab.cern.ch/HPTD/tx_phase_aligner`). It can have a resolution of $o(ps)$.



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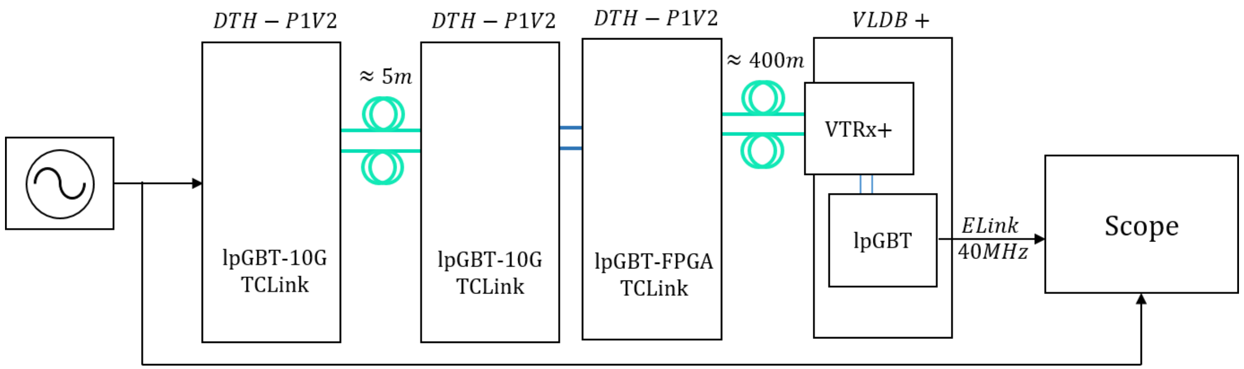
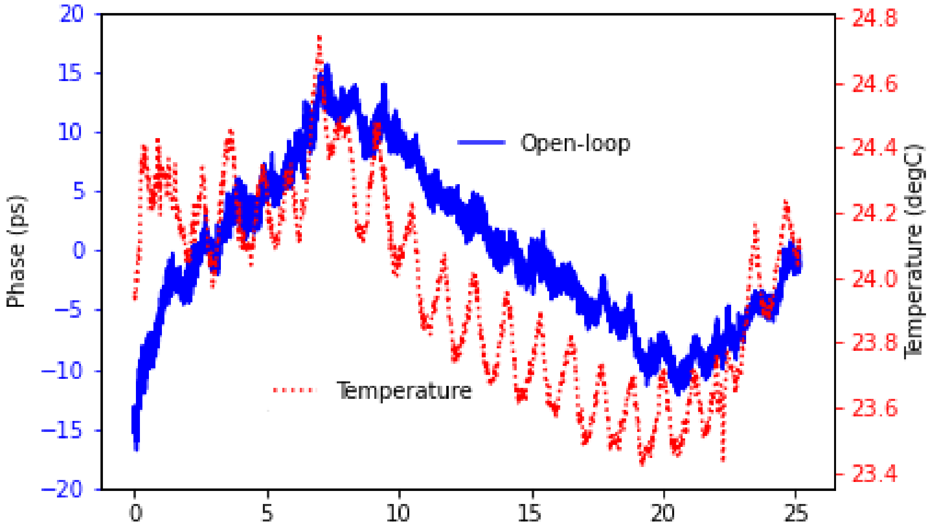
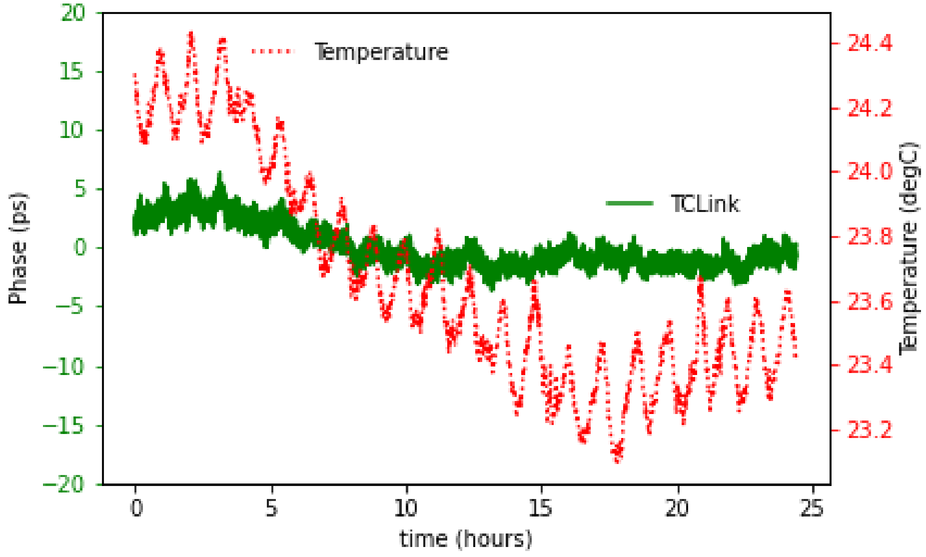
# TCLink Performance for cascaded links



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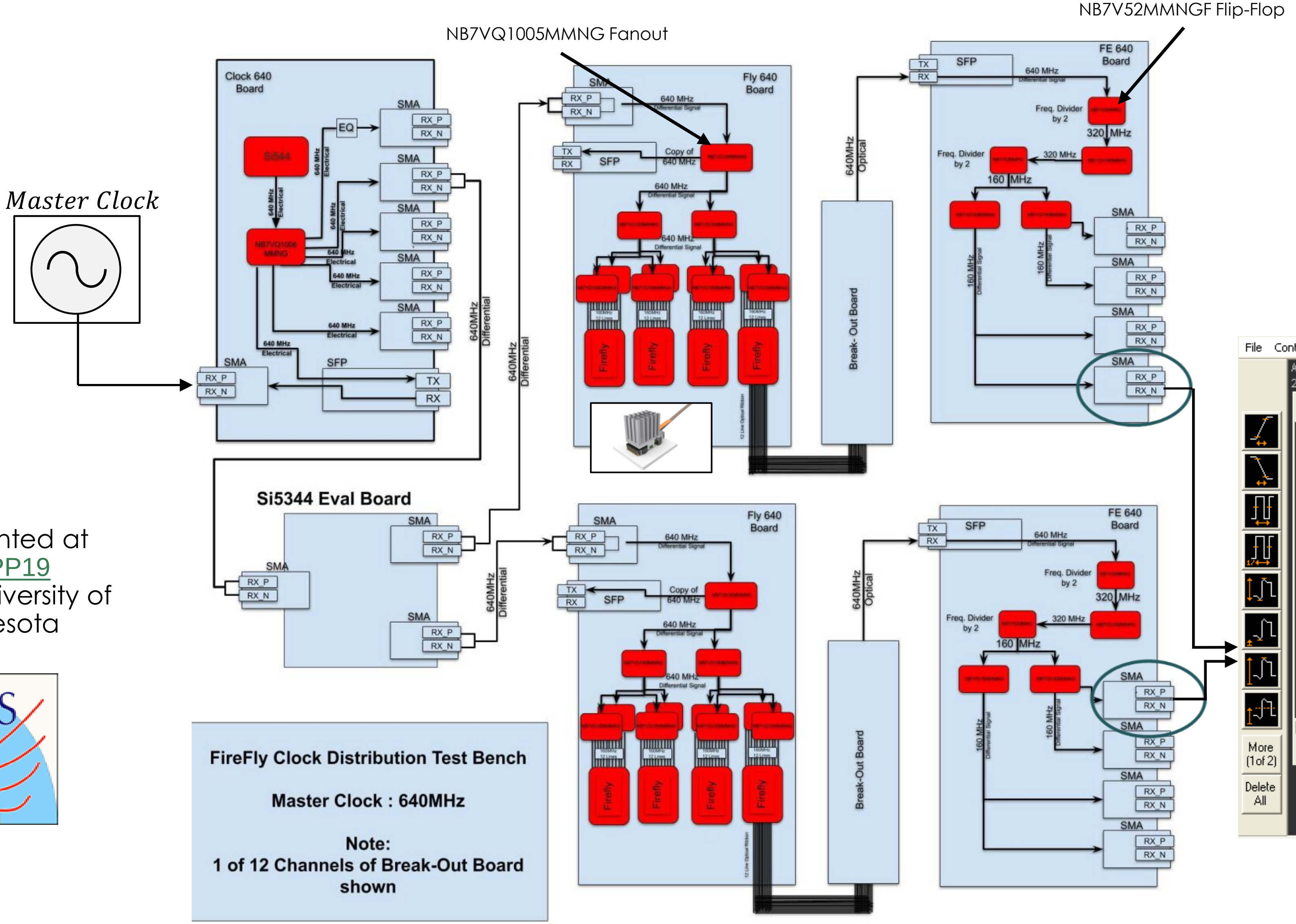
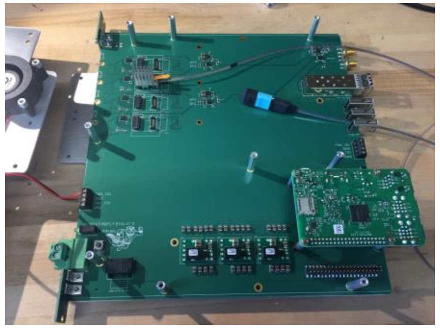
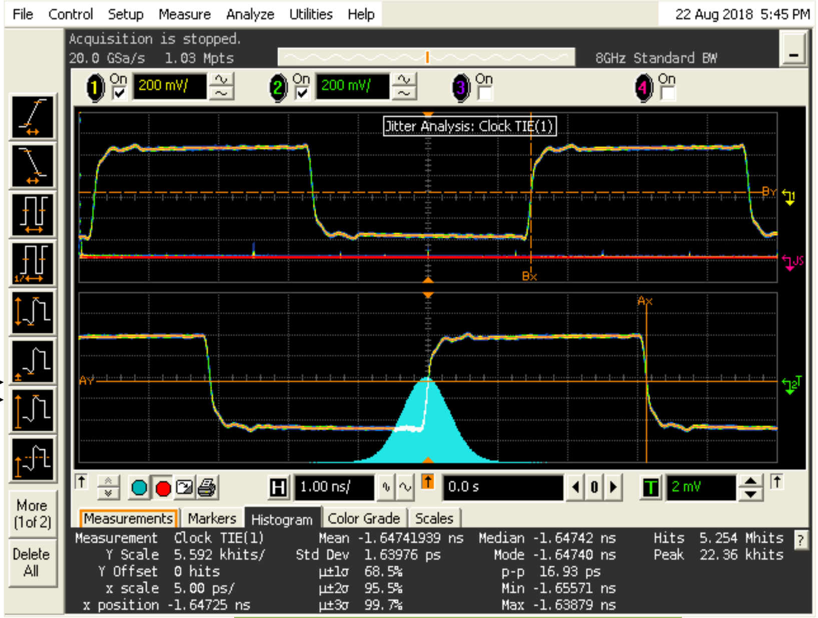
# Alternative: Pure Timing Distribution Example



FLY640

Presented at [TWEPP19](TWEPP19)
By University of Minnesota




Measure 1.6 ps *TIEss*



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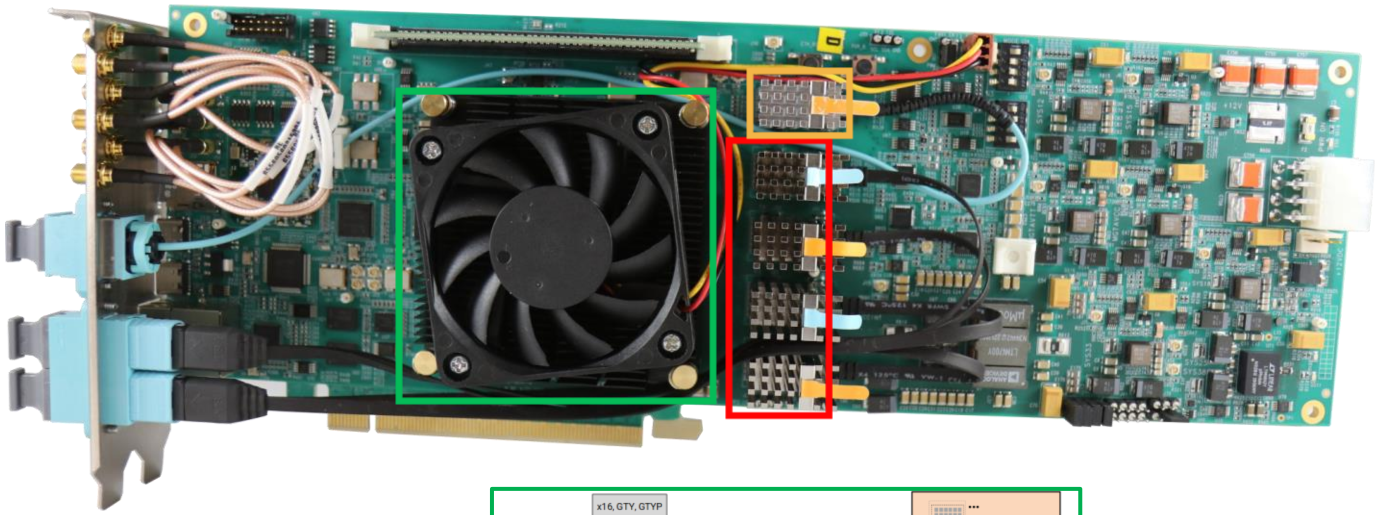
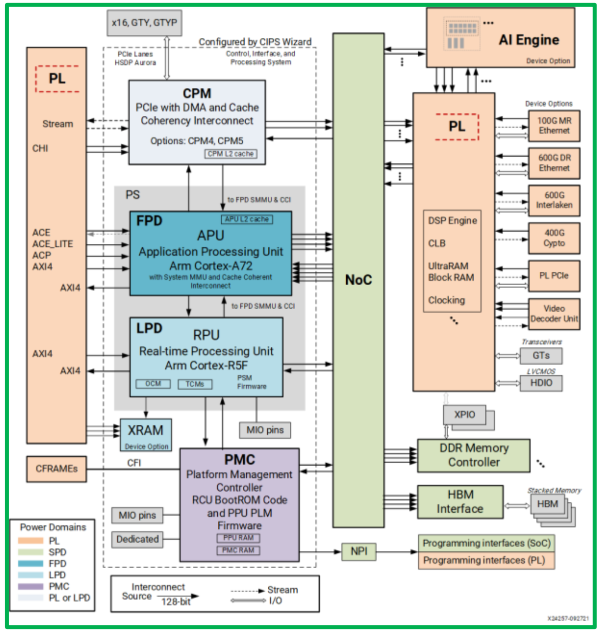
# ePIC DAM: ATLAS FELIX Phase II Run 4 hardware

- Based on Xilinx Versal Prime VM1802
  - Dual-core ARM Cortex-A72 Application Processing Unit
  - Dual-core ARM Cortex-R5F Real-Time Processing Unit
  - AI Engine
  - Programmable Logic
  - Future: Versal Premium
- 4 Samtec FireFly transceivers
  - 24 bi-directional optical links (future: 48 links)
  - 10 / 25 Gbps bandwidth per channel
- 1 Samtec FireFly for LTI/TTC link
  - Trigger, Timing and Control (4 links)
  - 100 GbE Networking
- PCIe Gen4 x16 (240Gbps)
  - 2 x8 lanes bifurcated
  - Future: PCIe Gen5 up to 16 lanes

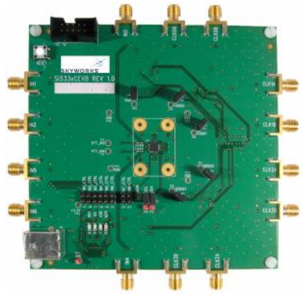
BNL FLX-182 Prototype



Versal Prime



# ePIC Timing Test Setup Proposals



Silicon Labs clock generator
160kHz to 700MHz in
LVPECL/LVDS, <1 ps RMS Typ
Jitter, Zero ppm Freq Error

6-10 Gbps link, e.g., 10b8b encoding
Would provide 8 bytes in 10ns

Use some of the bits as “DCS” commands;
e.g., 40bits EIC bx counter; some bits for
“trigger commands”

Other, more
efficient
encodings?

Other, more
efficient
encodings?
FEC?

Precision
Clock
Generator;
e.g., SiLabs
SI5338-EVB
eval board

RefClk:
~100MHz?

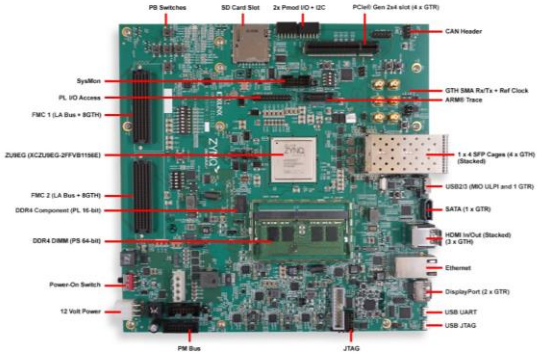
**GTU**
e.g. Zync
Ultrascale+
eval board

**FELIX**
(Versal Prime
class board)

**RDO**
(Artix-
Ultrascale+
class board)

“busy”
feedback?

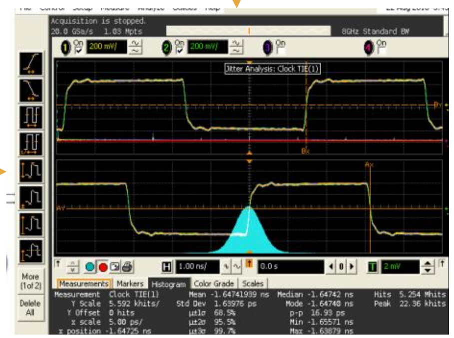
Do we need
better clock
generator here?



5 Gbps or 10 Gbps for
data and interleaved
slow controls response

Recovered
100 MHz
clock

800 MHz = 8 times EIC clock
to transmit eight 8bit
nibbles in one EIC clock



Fast Scope (and spectrum analyzer?)



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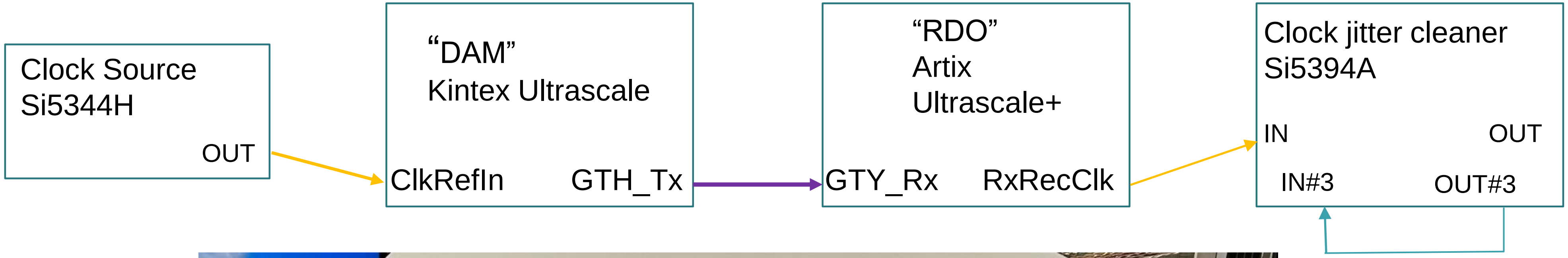
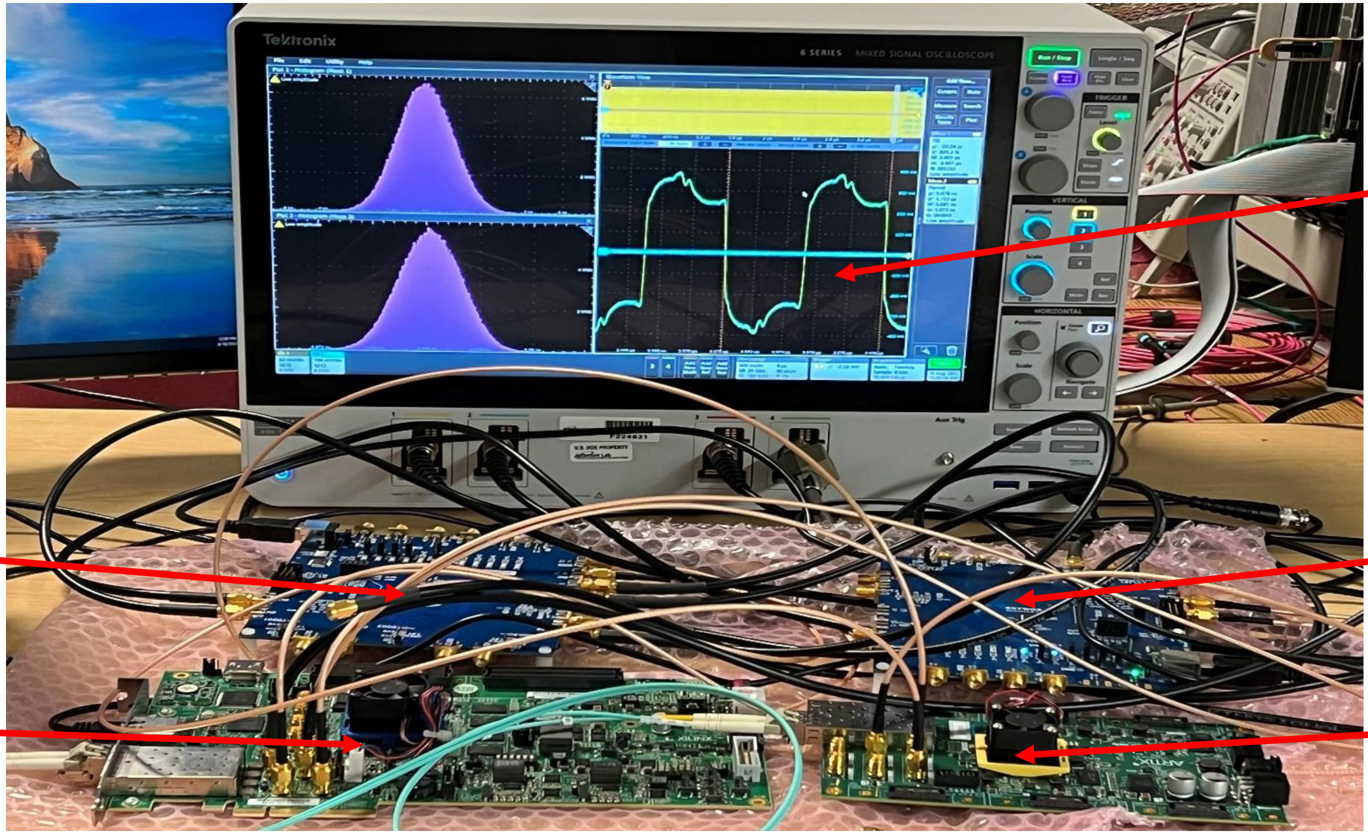
# First ePIC Timing Tests (W. Gu, Jefferson Lab)




Tektronix
MSO64
8 GHz, 25 GSps

Jitter
Cleaner

Clock Source
"GTU"

"DAM"

"RDO"



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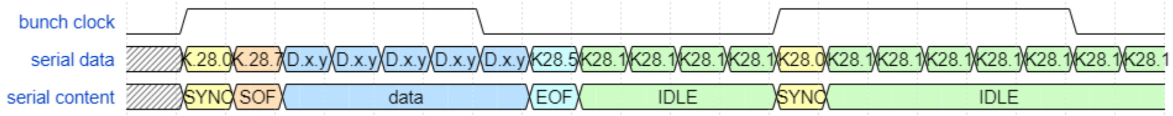
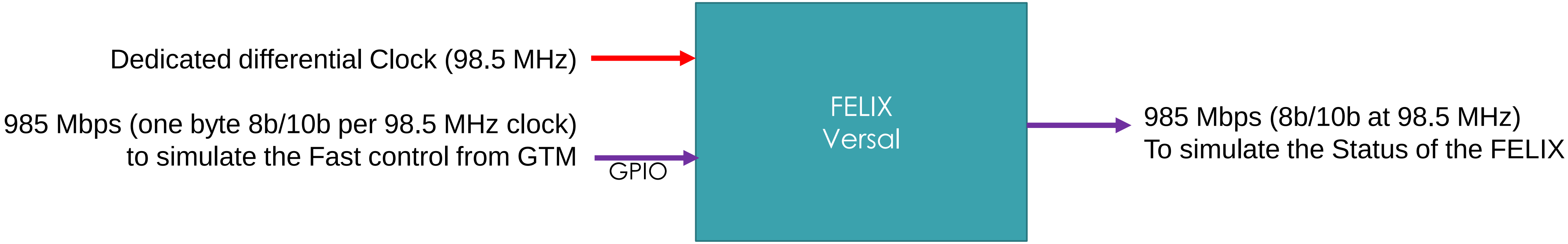
# First Results (W. Gu, Jefferson Lab):

- Downlink Custom Protocol:
  - Eight bytes (8b10b) payload per Clock (98.5 MHz)
  - **7.88 Gbps** line rate (6.304 Gbps payload rate)
  - Clock embedded transmission via **GTH** transmitter
- **GTY** Clock recovery works OK
  - The TIE (σ) is below **4ps**
  - Phase is stable, recovered clock reproduces the original (GTH_Ref) Clock
- A **Clock Jitter Cleaner** further improves recovered clock with a TIE (σ) below **2ps**
- Future Tests: Use (Versal based) FELIX prototype

Encoding:




7.88 Gbps line rate
Eight 8b/10b payload per clock (98.5 MHz) equivalent (downlink)
control words: 6.304 Gbps
Control symbols as frame delimiters, BC markers, and IDLEs





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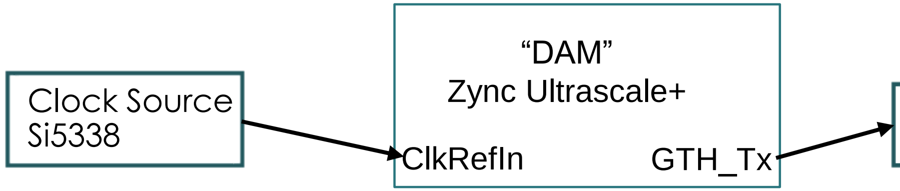
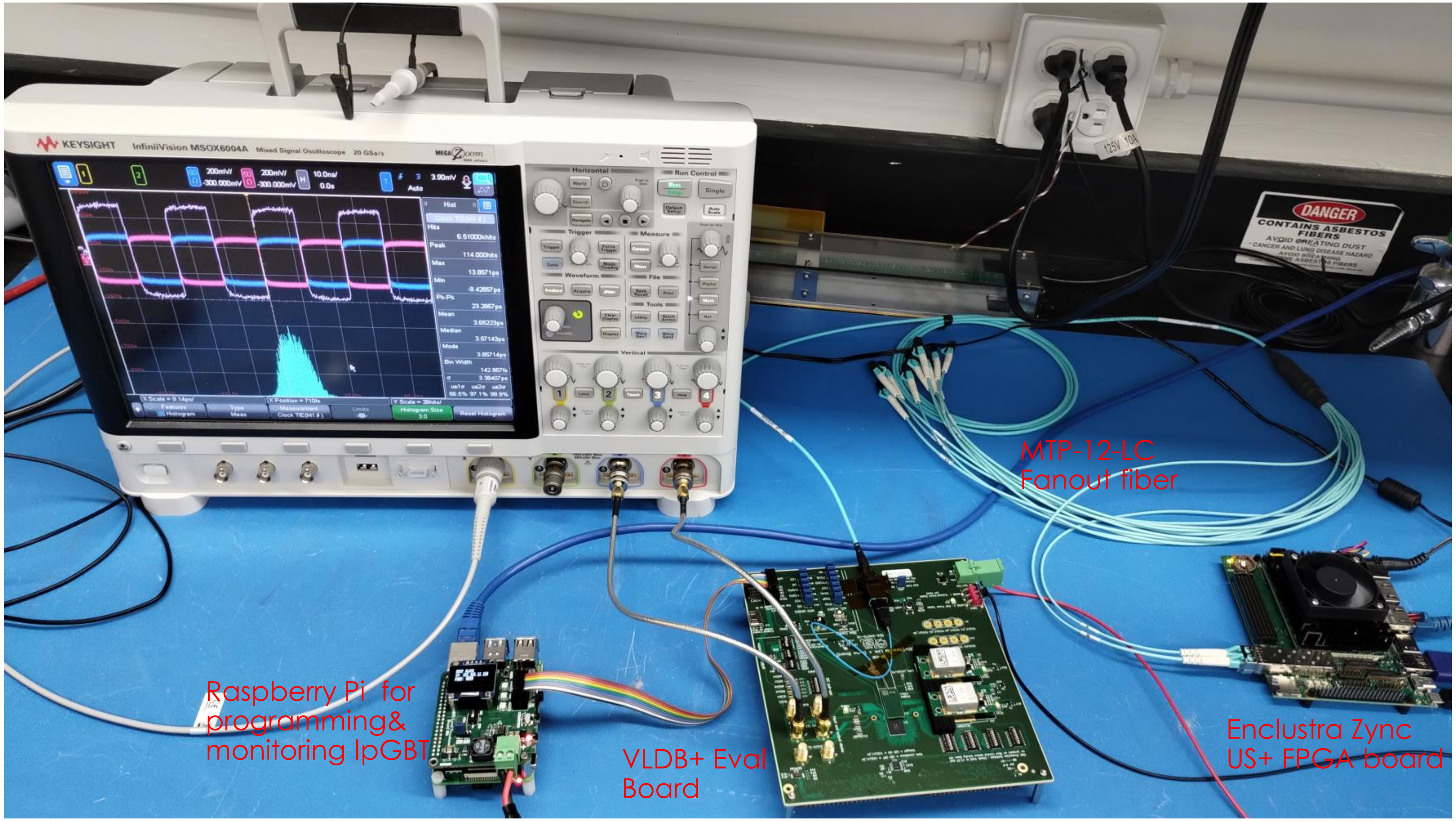
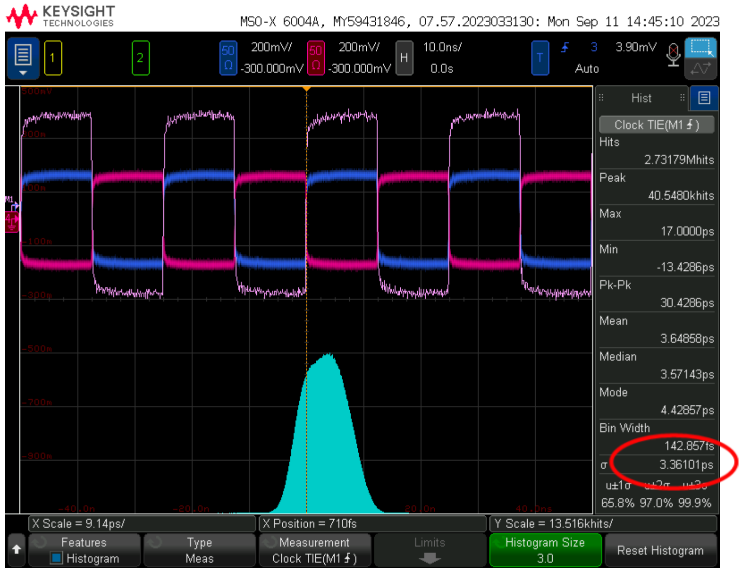
# First ePIC Test with lpGBT / VTRx+ based Timing Distribution




- RefClk in: 315.27 MHz (EIC x 2 / 5)
- Phase Adjustable Clock output from lpGBT: 39.4MHz
- TIE: **3.36ps**

# Next Steps

- Initial tests show that jitter for an embedded clock distribution via custom protocol or lpGBT protocol with either FPGA transceiver-based clock recovery or clock recovery in the lpGBT chip achieves the necessary jitter performance
- We need to  investigate the phase determinism over power cycles
- We need to investigate the phase drift vs environmental parameters
- Investigate if the TCLink and HPTD IP methods work in the Versal FPGA considered for the FELIX
- Investigate “direct” clock distribution in a separate link with fan-out, need for jitter cleaning, ….
- Develop ePIC timing and DCS protocol (in addition to Data protocol)
- Test setups with ”realistic” RDO prototypes (using ARTIX FPGA) interfaced to ASICs considered
- Test Cascaded setups (GTU -> FELIX -> RU)