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Silicon MAPS Streaming Readout in ALICE, sPHENIX, and ePIC

J. Schambach

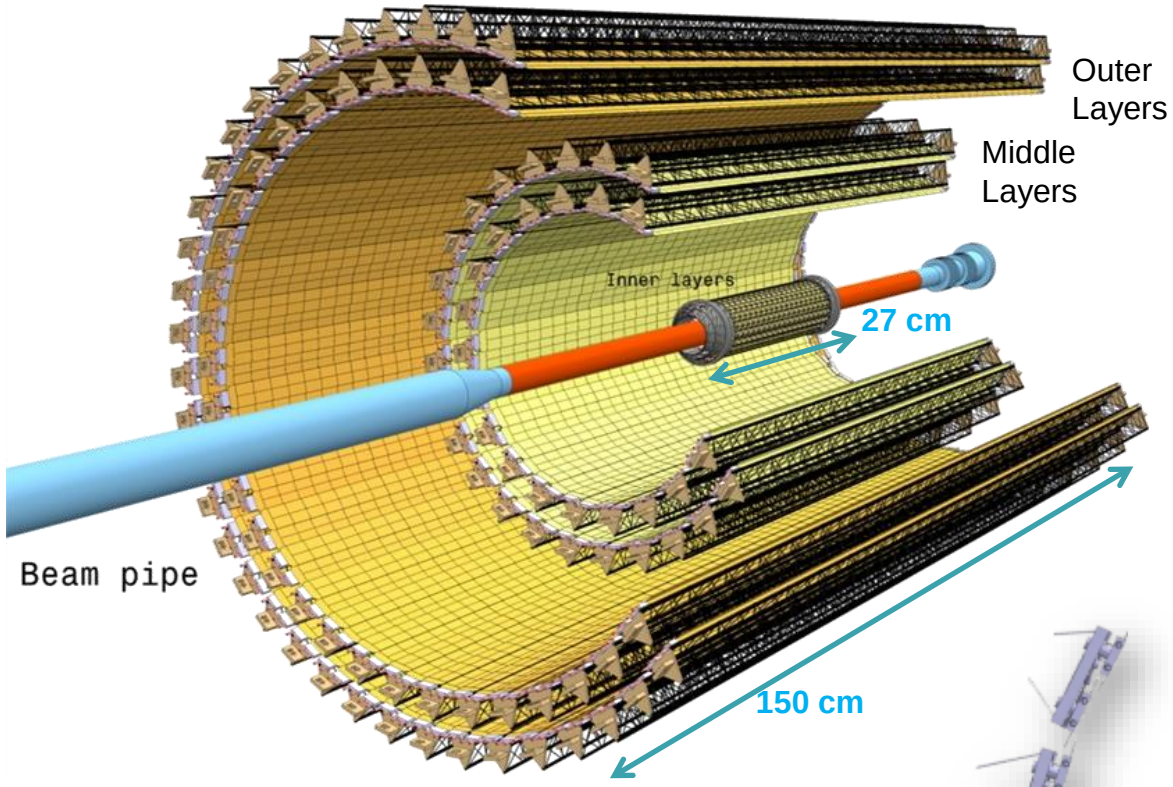
Oak Ridge National Laboratory

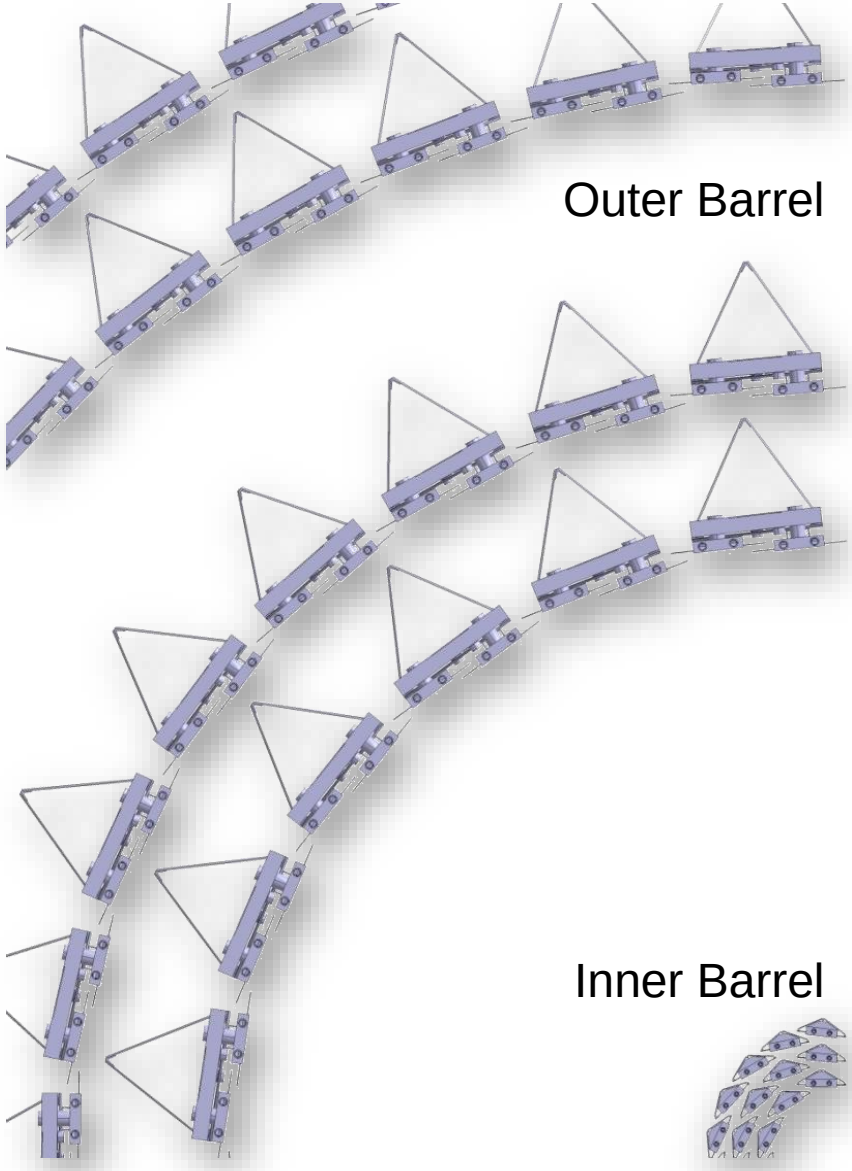
- ALICE ITS-2
- sPHENIX MVTX
- ALICE ITS-3
- ePIC SVT

ORNL is managed by UT-Battelle, LLC for the US Department of Energy

U.S. DEPARTMENT OF ENERGY

ALICE ITS-2 Layout





2 Outer layers

1% X_0

2 Middle layers

3 Inner layers

0.3% X_0

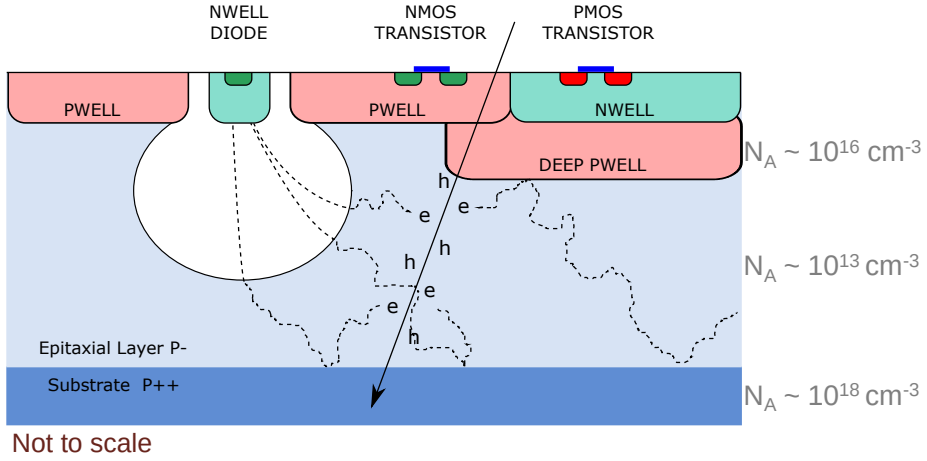
= **192** Staves in Total

- 7-layer barrel, based on CMOS MAPS sensors ("ALPIDE")
- Coverage: r 22 – 400 mm, $|\eta| \leq 1.22$
- ~24k pixel chips (a 12.5 G pixel camera)
- ~10m^2 active area

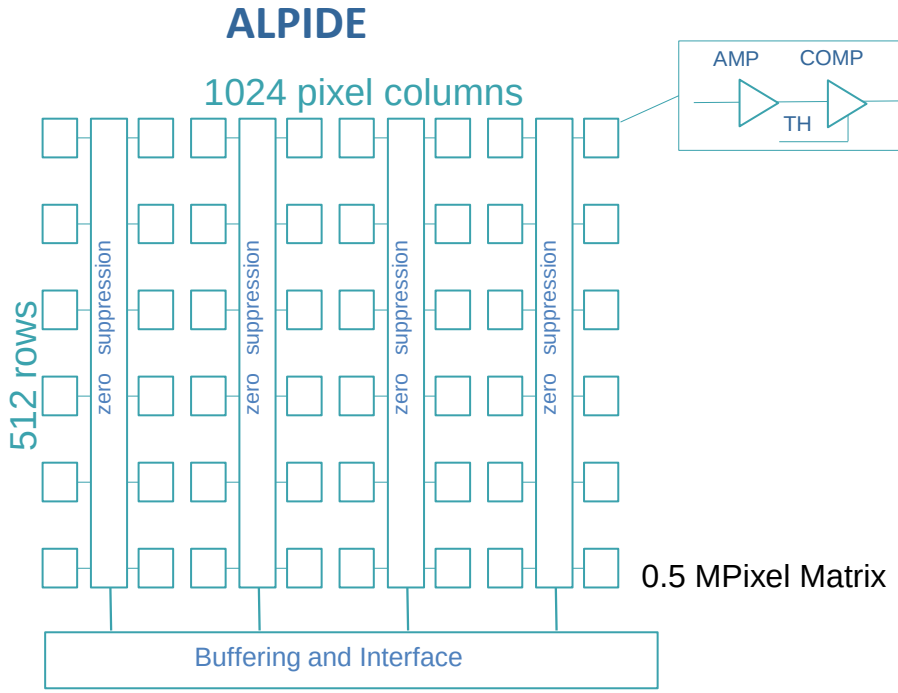
ALPIDE Sensor Technology

Pixel Sensor CMOS 180 nm Imaging Process (TowerJazz)

3 nm thin gate oxide, 6 metal layers



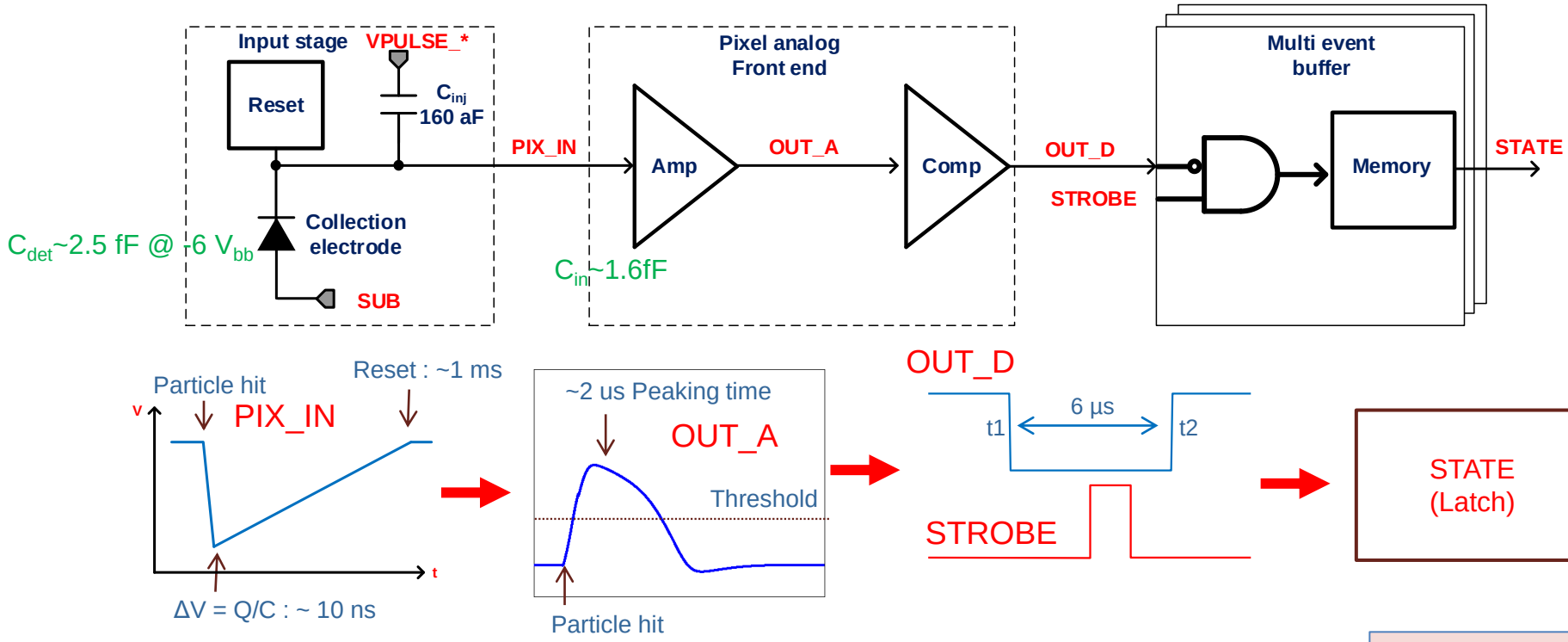
Not to scale



Key Features

- 29 μm x 27 μm pixel pitch, chip size 30 mm x 15 mm, 50 μm (IB) / 100 μm (OB) thick
- Continuously active, ultra-low power front-end (40nW/pixel)
- Ultra-low power matrix readout (< 200mW whole chip)
- Global shutter: triggered acquisition or “continuous readout”
- High speed output serial link: 1.2 Gbit/s (IB), 400 Mbit/s (OB)

ALPIDE Principle of Operation



ultra low-power front-end circuit
40nW / pixel

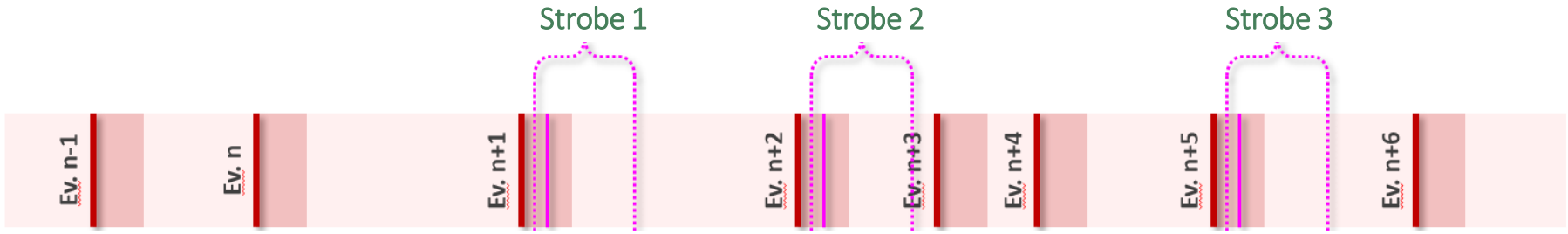
Front-end acts as delay line

- Sensor and front-end continuously active
- Upon particle hit front-end forms a pulse with ~1-2µs peaking time (“analog delay”)
- Threshold is applied to form binary pulse
- Hit is latched into memory if strobe is applied during binary pulse

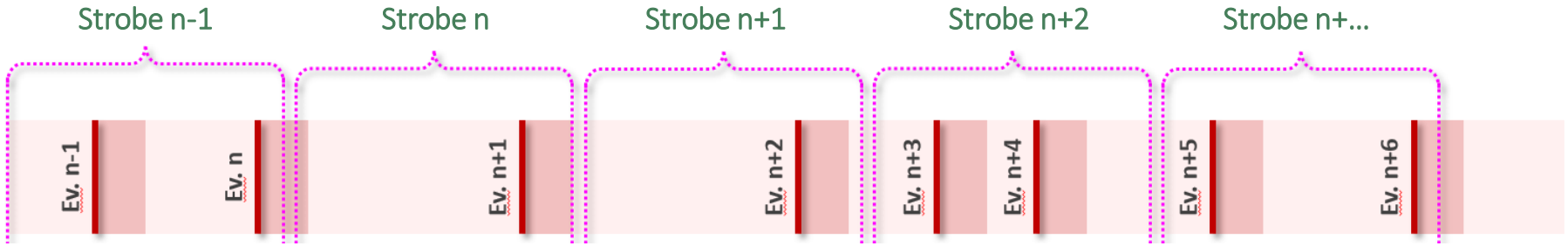
Triggered and "Continuous" Mode Operations

- ITS-2 can operate in two modes:

  Triggered mode: Pixels are latched with a short (~100 ns) strobe window, followed by read out, based on an external trigger.



  Continuous mode: Pixels are latched using long, periodic strobe windows (~10 µs) with short inter-strobe periods (≈100 ns) to initiate read out.



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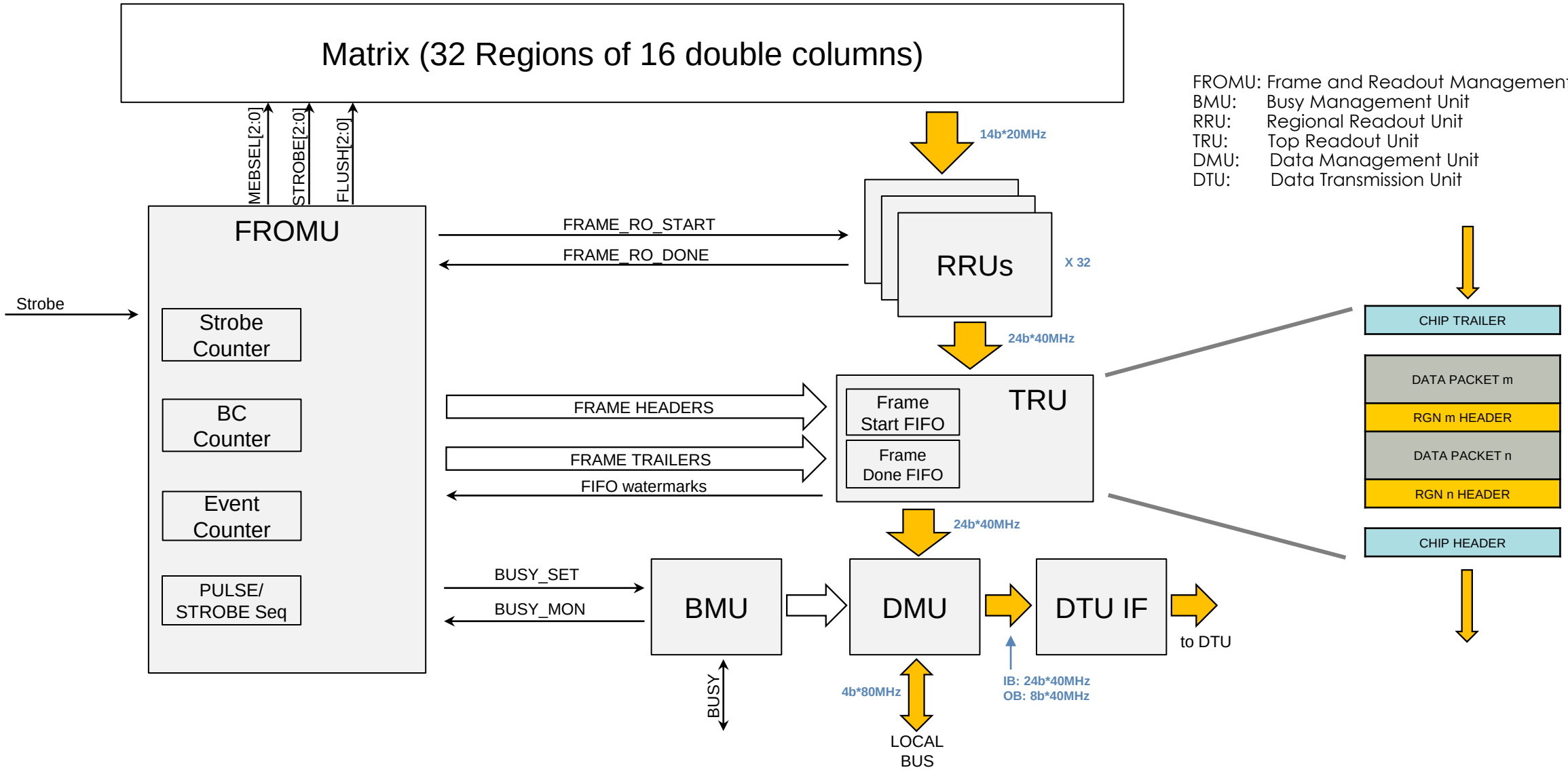
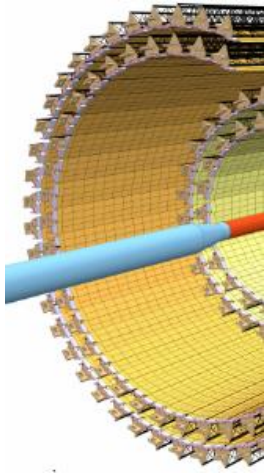
ALPIDE Readout Architecture



ALICE ITS-2 Readout Hierarchy



IL
9×960 Mb/s

ML
16×320 Mb/s

OL
28×320 Mb/s

DETECTOR LINKS

ALICE Timing and Trigger
LHC Bunch Clock (40.08 MHz)
Timing and Trigger messages

LTU / CTP

RU

One READOUT UNIT for each *STAVE*

3× GBT LINKS/RU

3200Mb/s

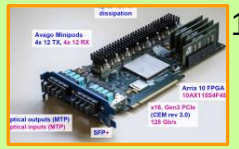
8× RU/CRU
24× LINKS

GBT LINKS

13× FLP

CRU

110 Gb/s



110 Gb/s

RAM

NIC

100 Gb/s

EPN

<40 GB/s

CRU to FLP

FLP to EPN

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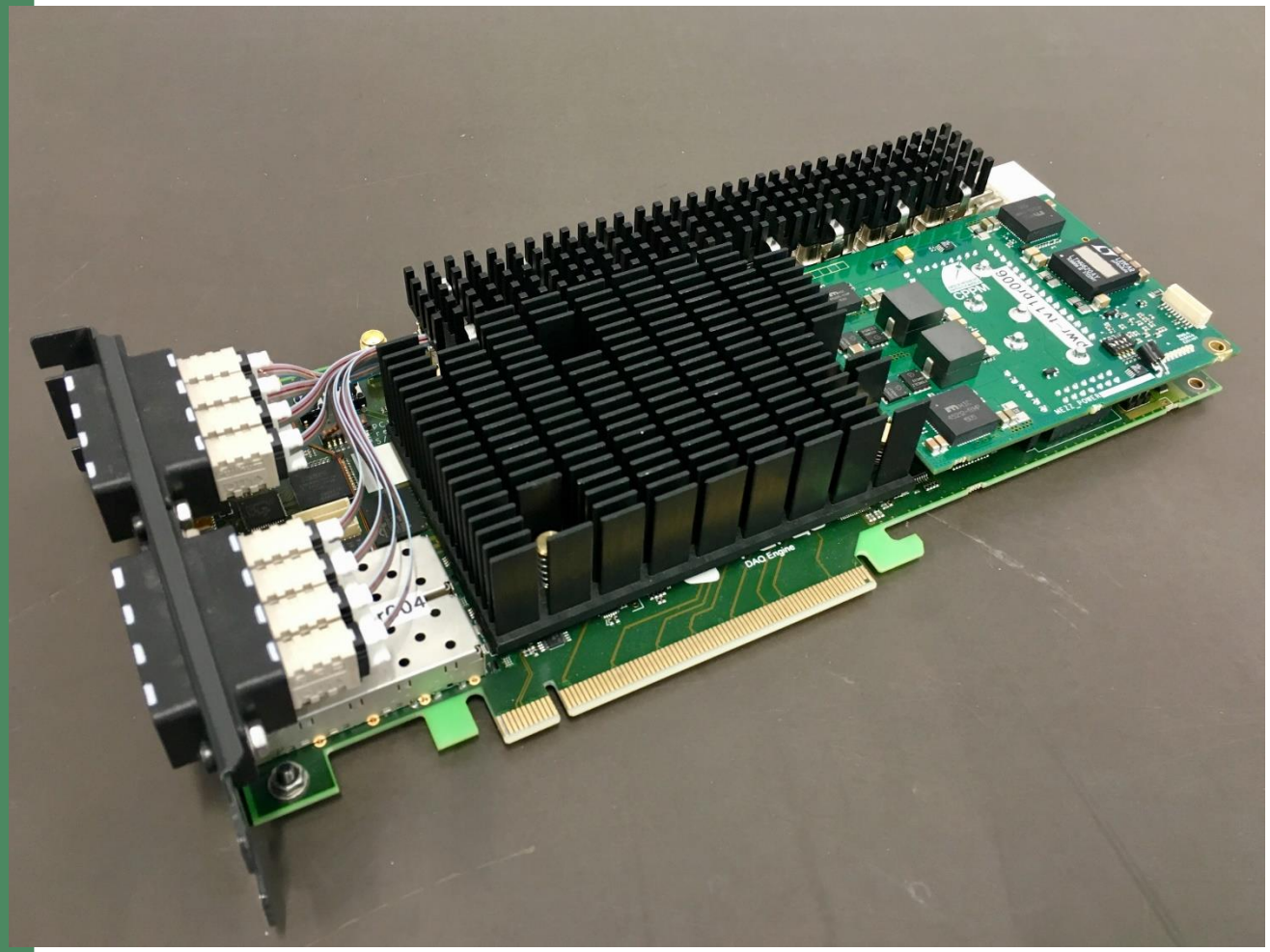
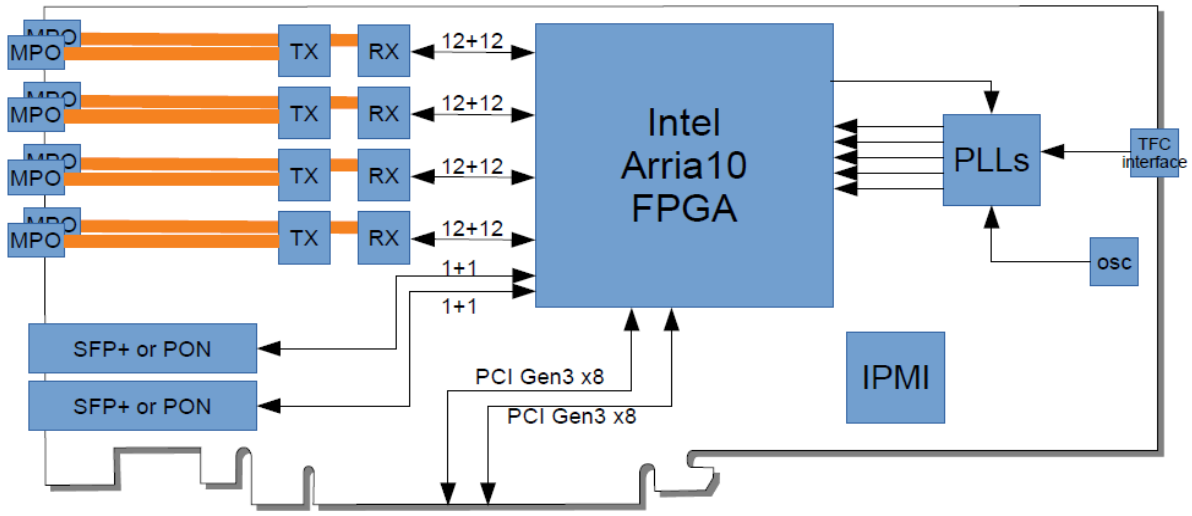
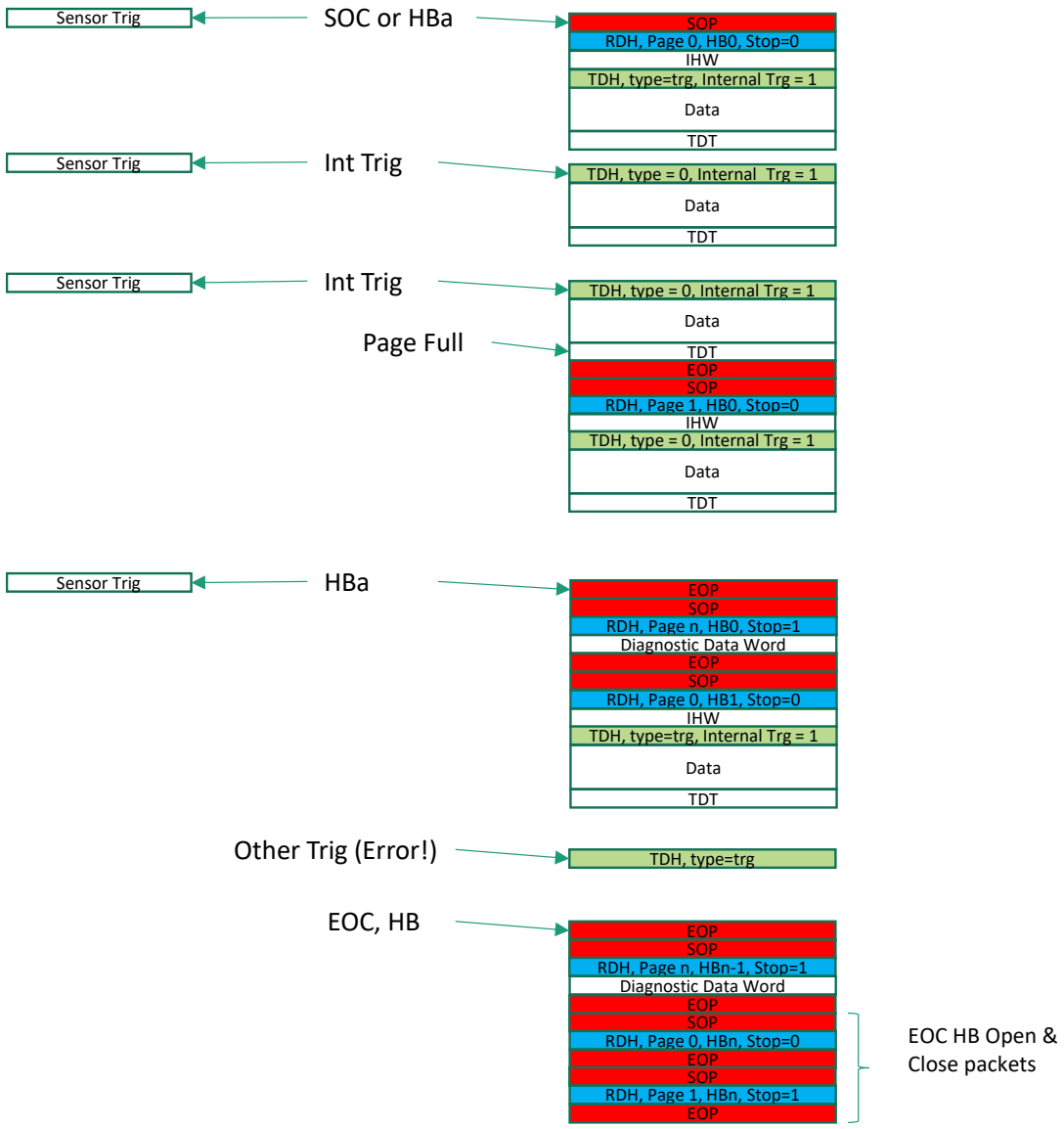
ALICE Common Readout Unit (CRU) v2



- Altera Arria 10 FPGA
- Custom designed cooling
- Avago Minipods:
  - 4x 12 TX
  - 4x 12 RX
- 48 optical outputs (MTP), 48 optical inputs (MTP)
- USB Blaster II
- X16, Gen3 PCIe (CFM rev 3.0); 128 Gb/s

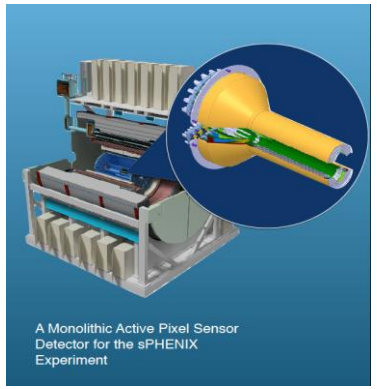


MAPS Streaming Readout Data Format



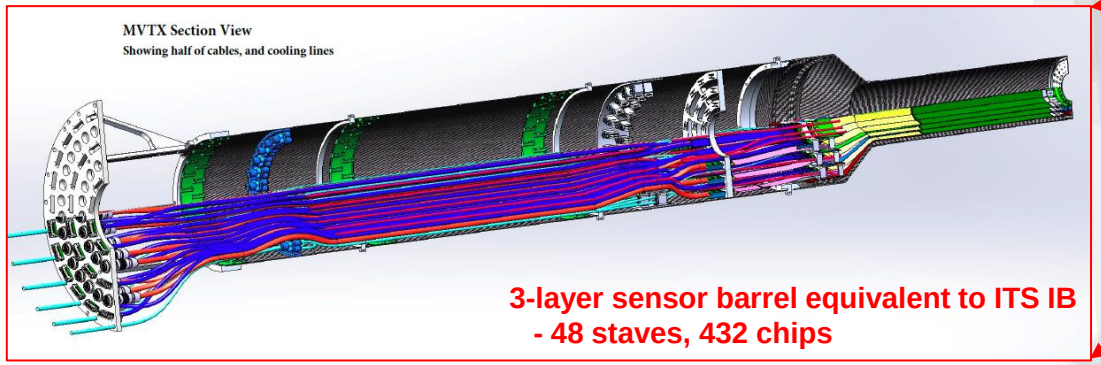
SOC: Start of Continuous
EOC: End of Continuous
TDH: Trigger Data Header
TDT: Trigger Data Trailer
RDH: Raw Data Header
IHW: ITS Header Word

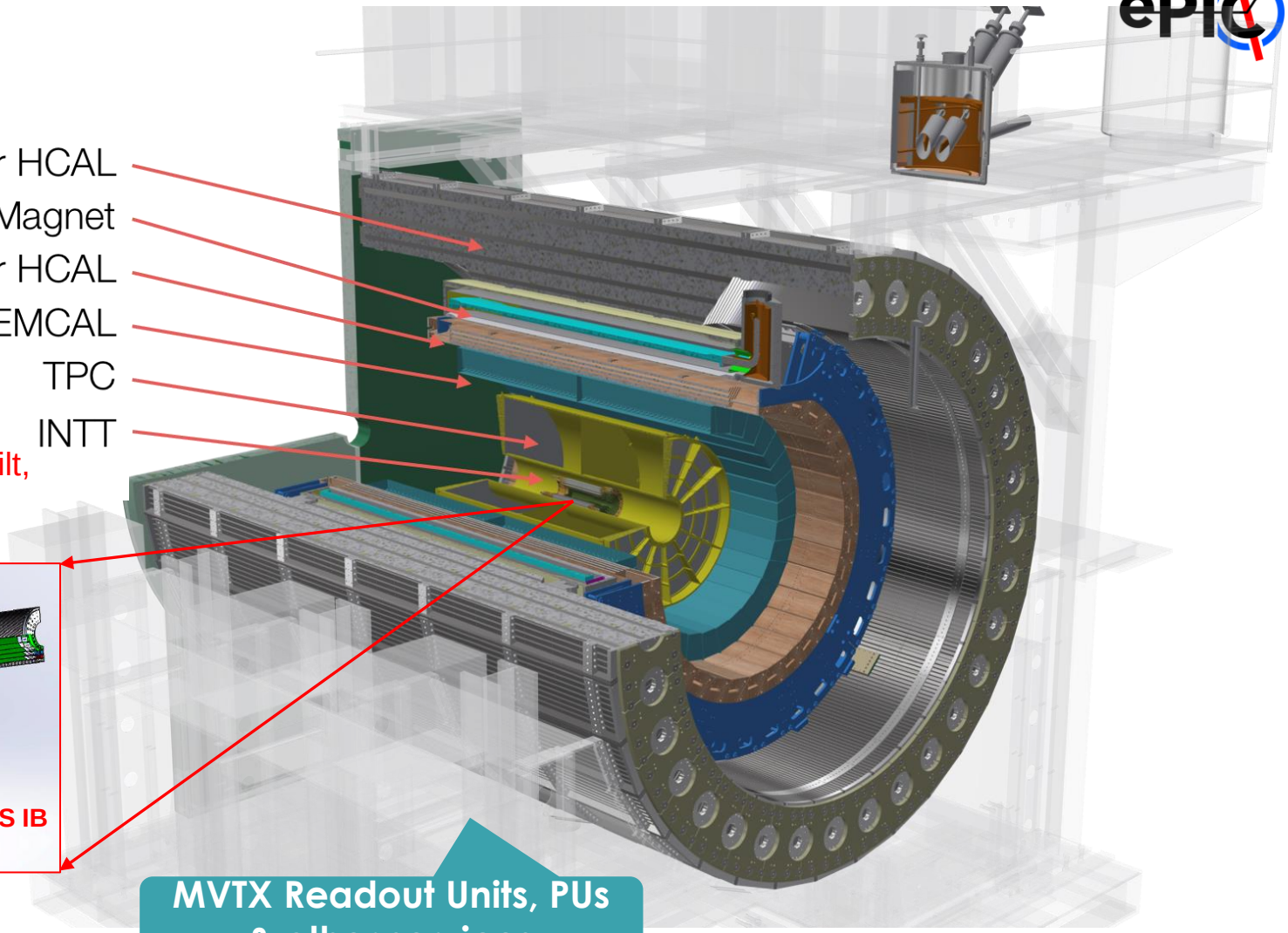
sPHENIX - MVTX



Proposal Document: sPH-HF-2018-001
https://indico.bnl.gov/event/4072/

- sPHENIX cost-effectively reuses the ITS electronics as built, replacing the ALICE CRU with the ATLAS FELIX backend
- Modified ALICE ITS mechanics to fit it into sPHENIX



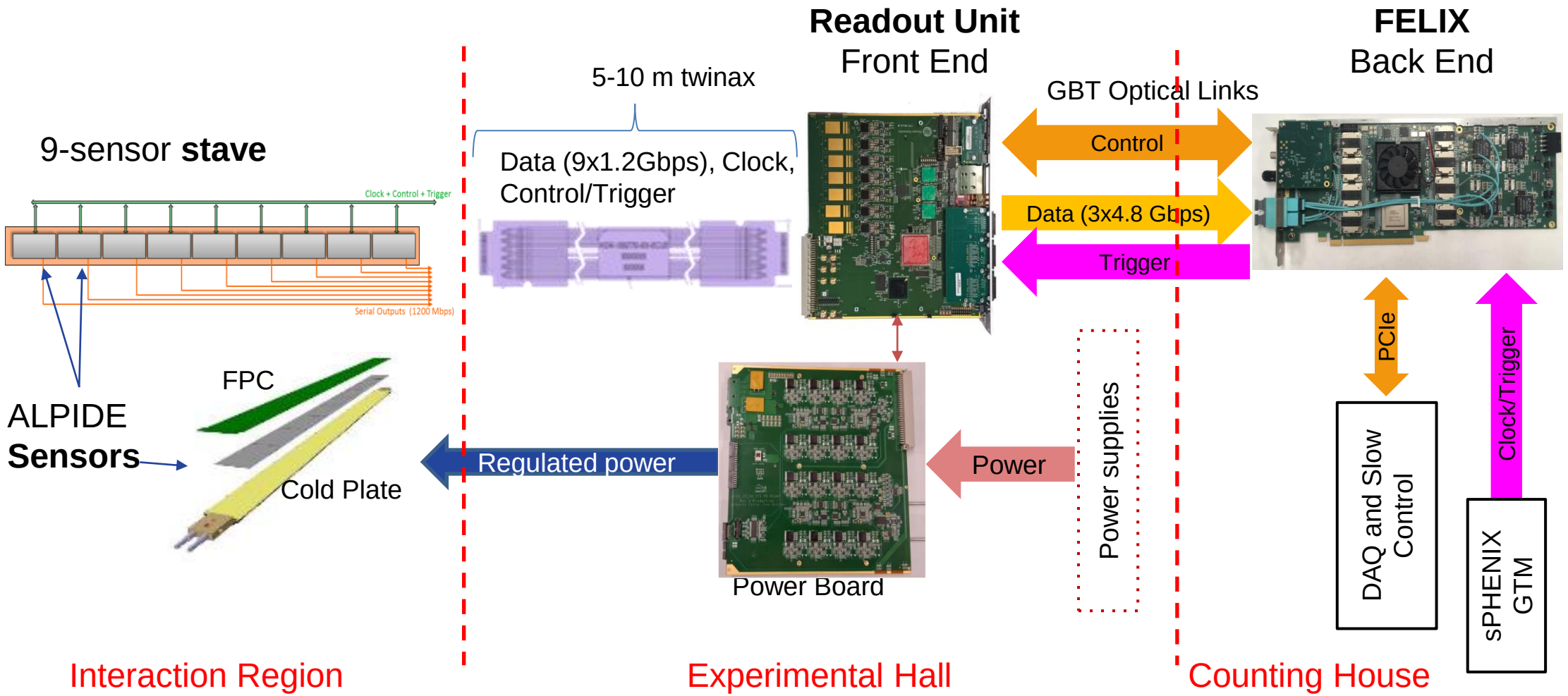


Located Outside Magnet on Platform:
Much lower Radiation than ITS

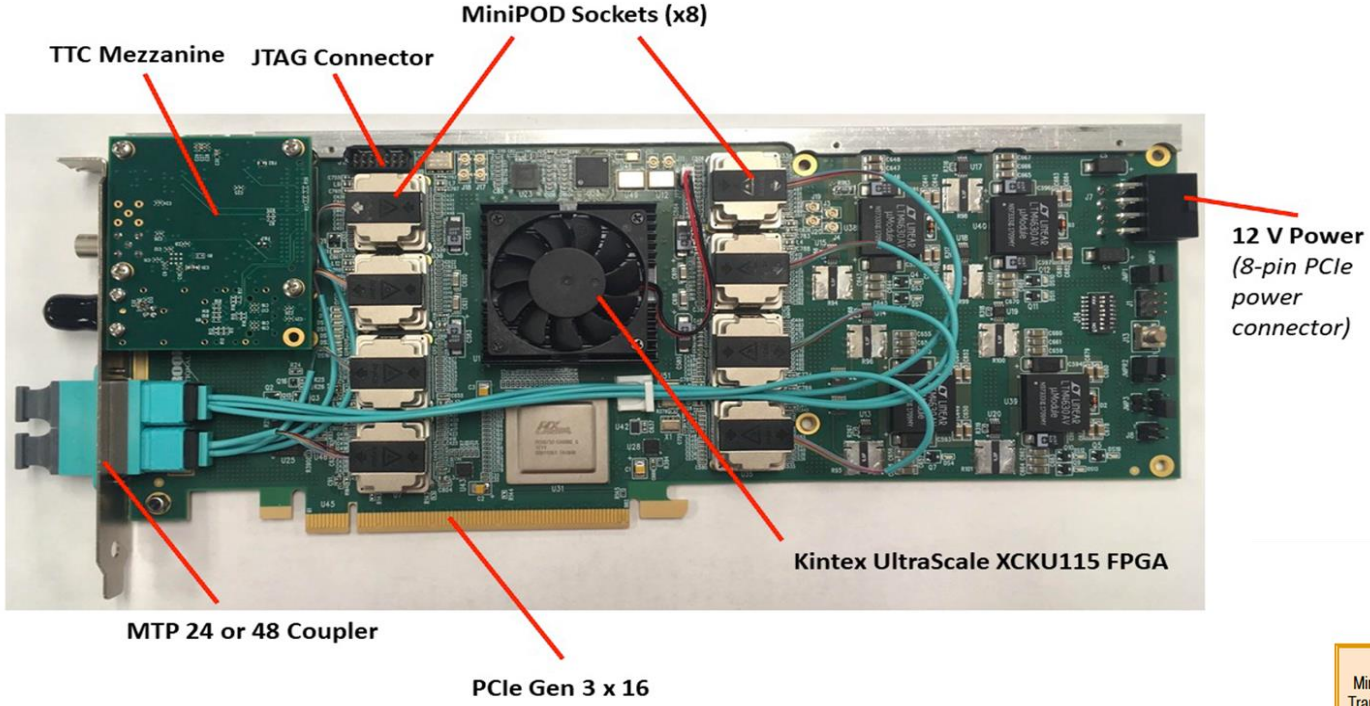
MVTX parameters: L = 271 mm

	R_min (mm)
Layer 0	24.61
Layer 1	31.98
Layer 2	39.93

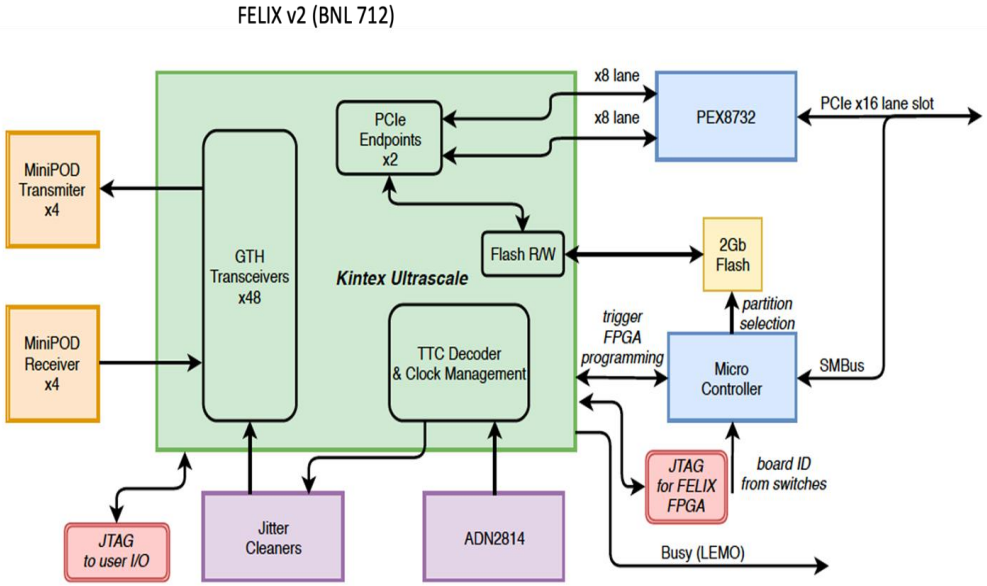
MVTX Readout System



sPHENIX "BackEnd": ATLAS FELIX 712v2



sPHENIX Timing Mezzanine



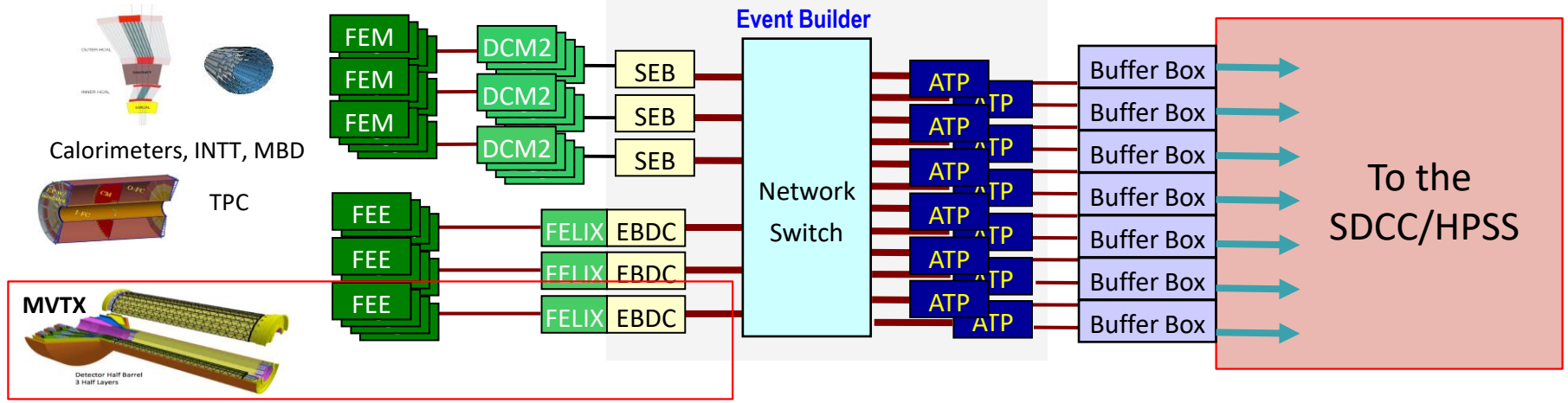
Architecture Highlights:

- Xilinx Kintex Ultrascale KU115 FPGA
- 48 **bi-directional** GBT links
- 16 lane Gen 3 PCIe
- Mezzanine site for sPHENIX timing system card

Performance:

- PCIe Tx > 100Gb/s

sPHENIX DAQ Architecture



MVTX Hardware:

- 48 Staves
- 48 FEE (Readout Units)
- 6 FELIX BNL-712v2
- 6 EBDC servers

Acronyms:

FEE	Front End Electronics
FELIX	Front End LInk eXchange
EBDC	Event Buffer and Data Compressor
ATP	Assembly and Trigger Processors
Buffer Box	Interim storage
FEM	Front End Module
DCM2	Data Collection Module
SEB	Sub-Event Buffer

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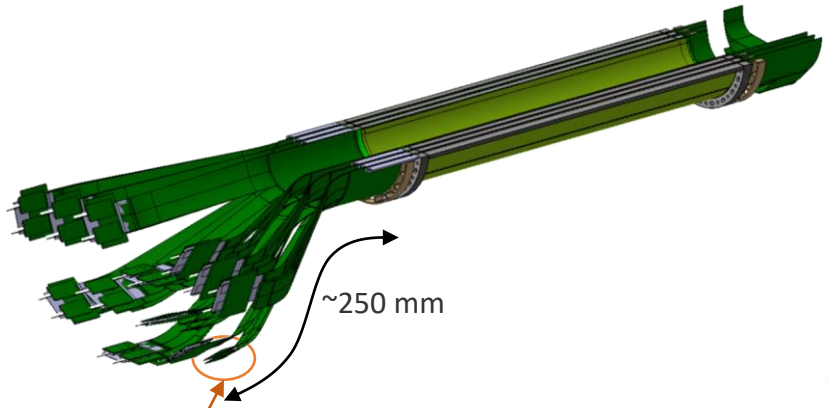
ALICE ITS-3 Streaming Readout



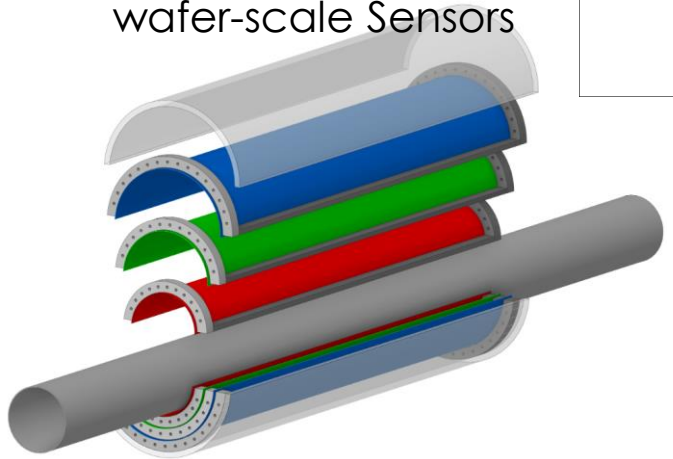
small PCB, one per sub-module

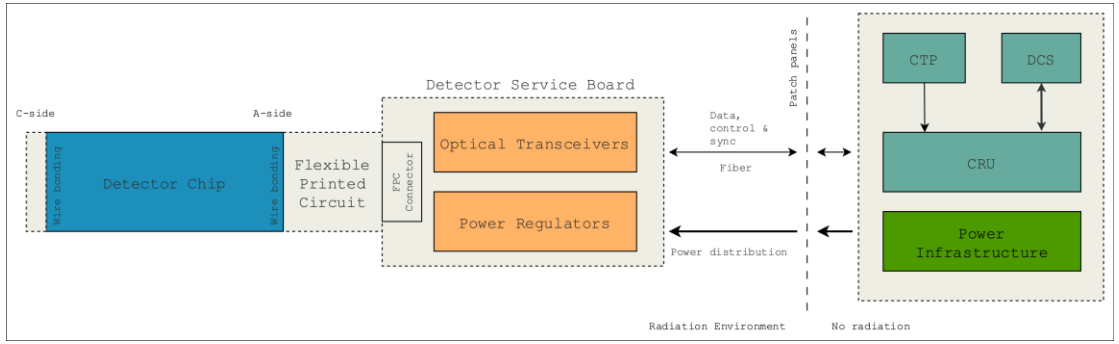
This board will host the two VTRx+ modules

VTRx+ to be placed as close as possible to sensor edge

The approximate dimensions are 30 mm x 30 mm.

TPSCo 65nm CMOS imaging process wafer-scale Sensors



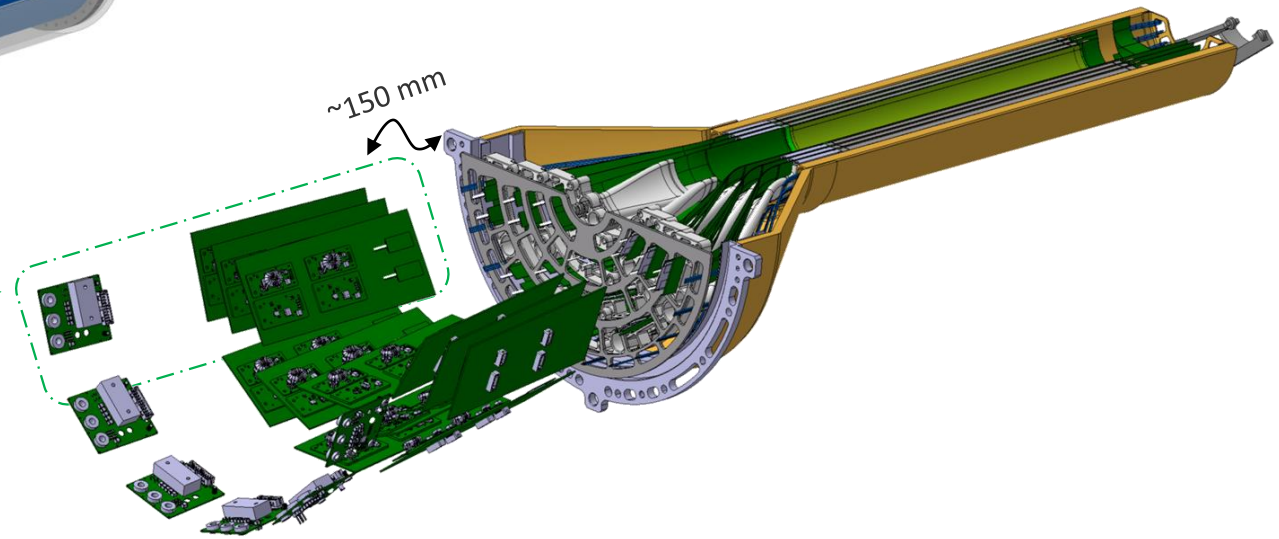


ITS-3 Readout Concept

Control Board

Contains all the remaining electronics

It is divided into several segments avoiding acceptance cone



*VTRx+ (Versatile TransReceiver)= Optical Link Module for Data Transmission

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ALICE ITS-3 “MOSAIX” Stitched Sensor

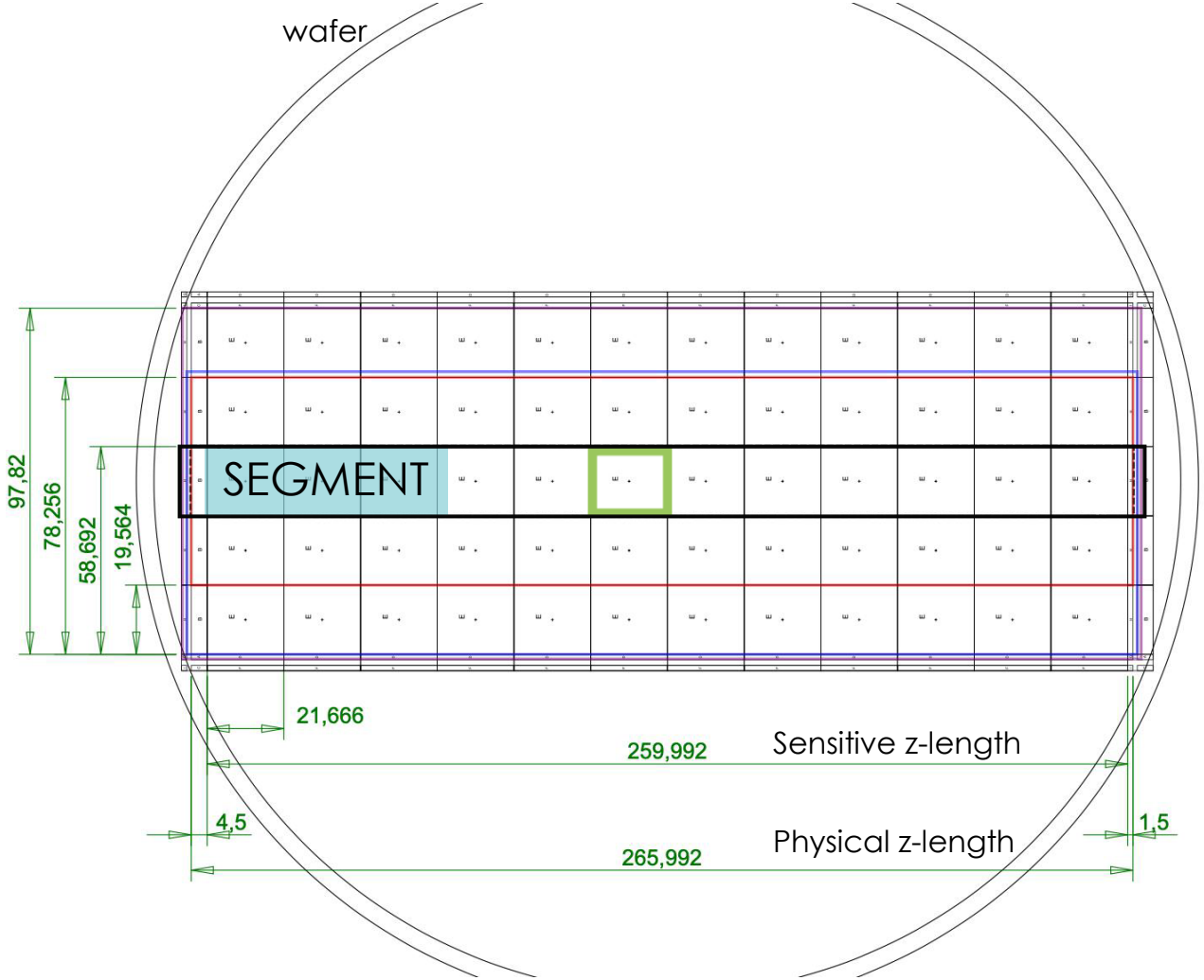
Layer 0: 12 x 3 repeated units+endcaps
Layer 1: 12 x 4 repeated units+endcaps
Layer 2: 12 x 5 repeated units+endcaps

Repeated (Stitched) Sensing Unit (RSU)

ITS-3

IB Layer Parameters	Layer 0	Layer 1	Layer 2
Sensor length [mm]		265.992	
Sensitive length [mm]		259.992	
Sensor azimuthal width [mm]	58.692	78.256	97.820
Radial position [mm]	19.0	25.2	31.5
Equatorial gap [mm]		1.0	

Table 3.2: Design dimensions of the sensor dies and radial position.



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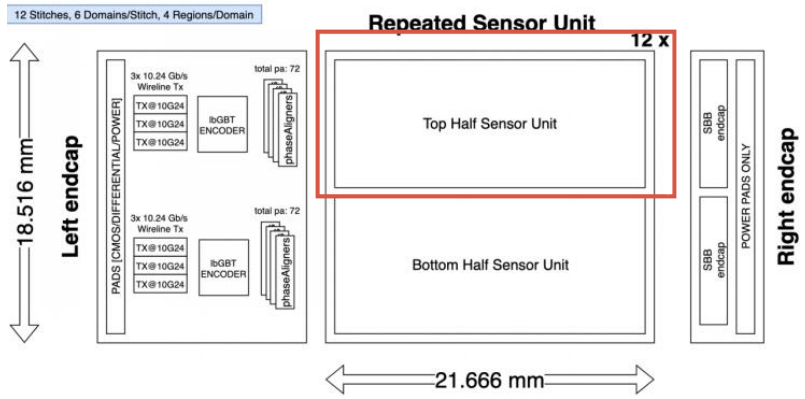
Half Repeated Sensor Unit

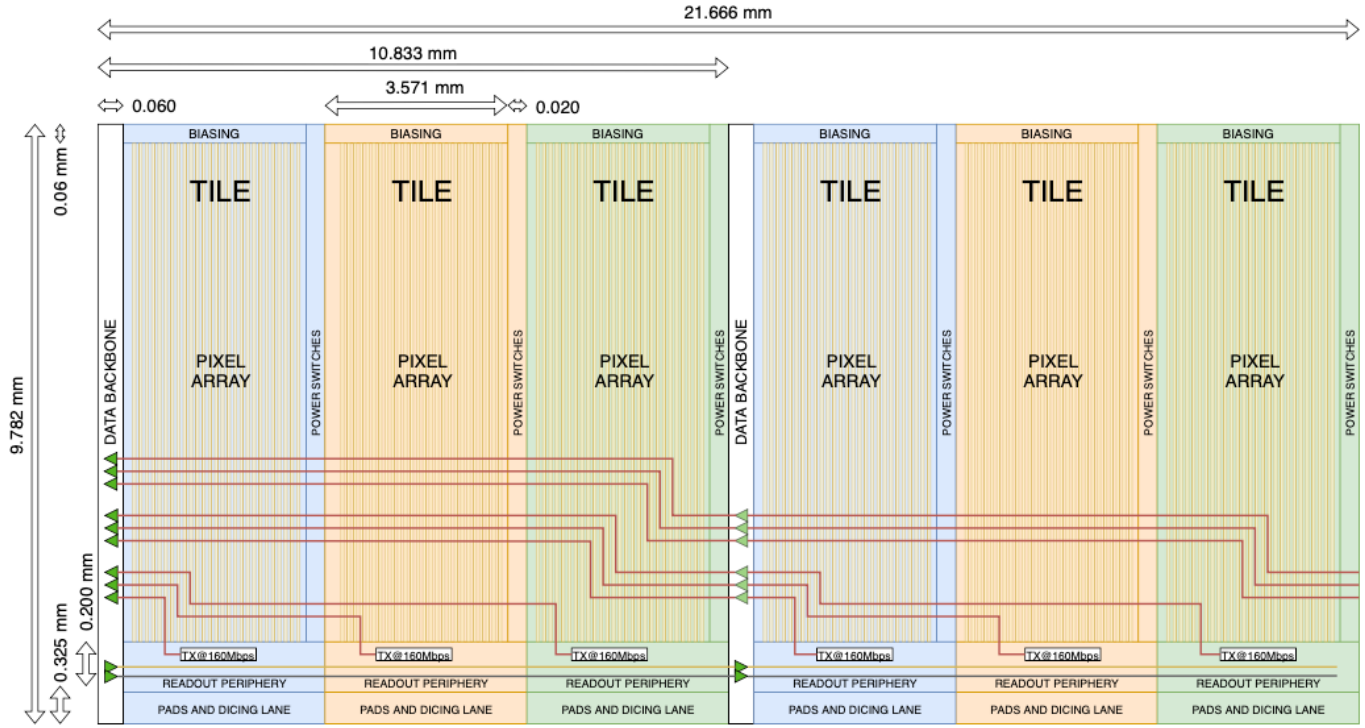


Block	Width [mm]	Height [mm]	Block Area [mm^2]	Instances	Percent area
RSU	21.666	19.564	423.873	1	100 %
Pixel Matrix	3.571	9.197	32.843	12	92.98 %
Biasing	3.571	0.060	0.214	12	0.61 %
Power switches	0.020	9.257	0.185	12	0.52 %
Data Backbone	0.060	9.257	0.555	4	0.52 %
Readout periphery	3.591	0.200	0.718	12	2.03 %
Test pads	21.666	0.250	5.416	2	2.56 %
Seal ring and dicing lane	21.666	0.075	1.625	2	0.77 %

Table 3.4: Plan of dimensions of the blocks composing one Repeated Sensor Unit and percentage of the RSU area occupied by the instances of the block.

Each Half Unit is segmented in **Tiles** (Domains)

Each **tile** acts as an
independent sensor
Separate Local Power
Configuration
Readout Link (160 Mb/s)
Each **Tile** data output has
direct connection to the **left endcap**



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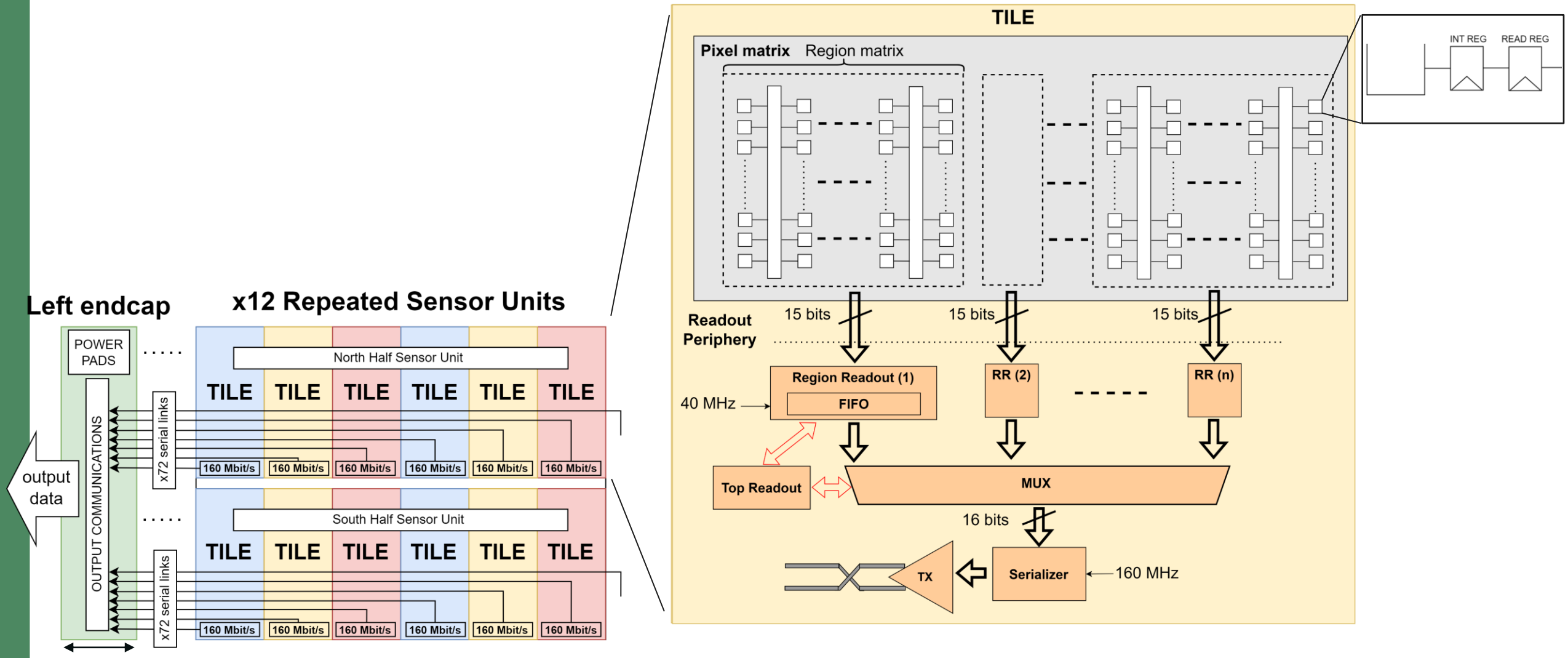
On-Chip Readout Scheme



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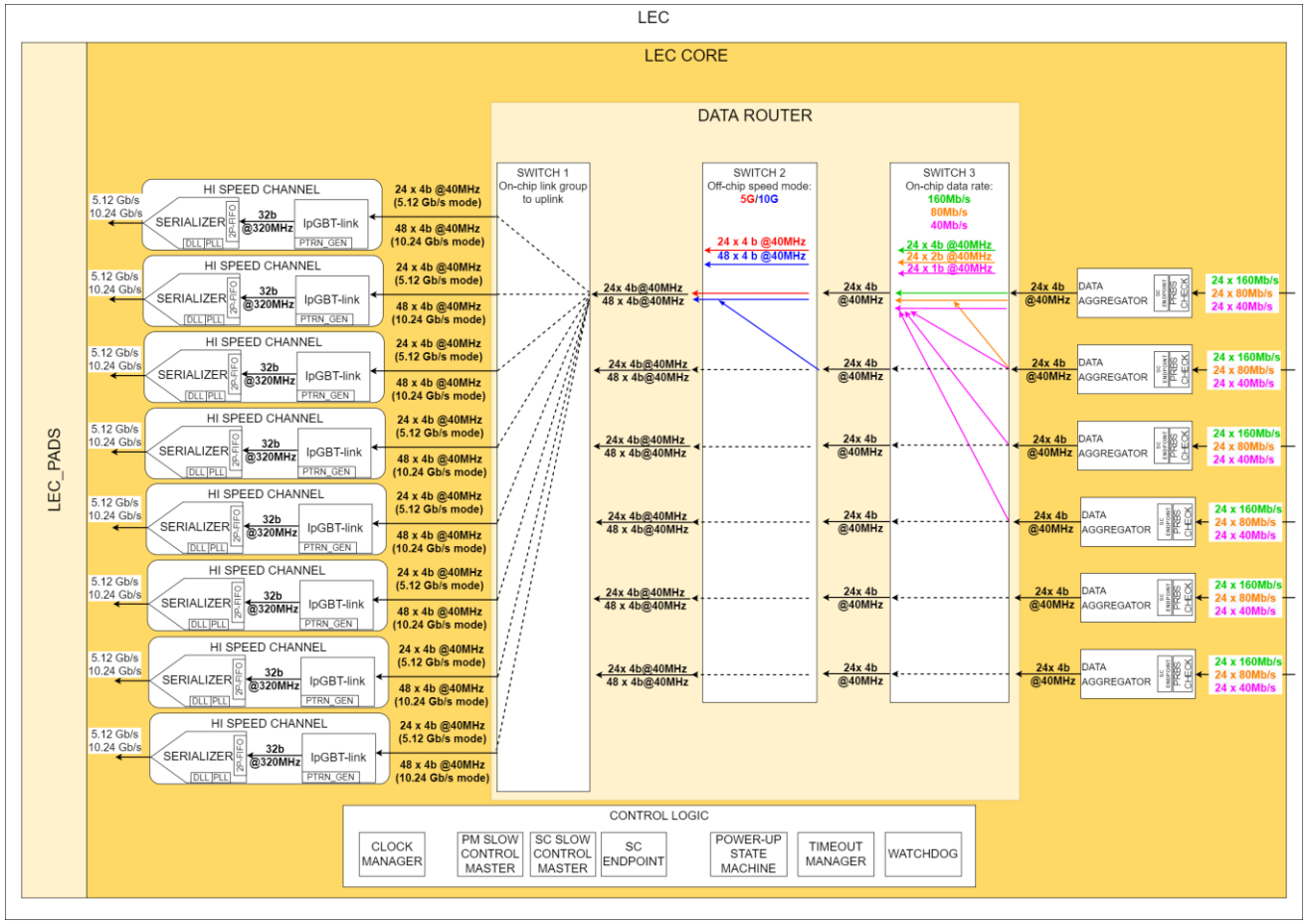
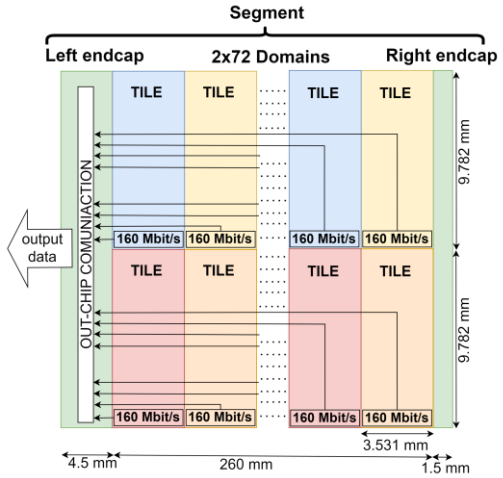
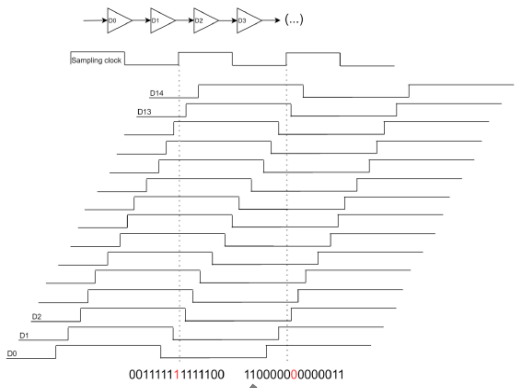
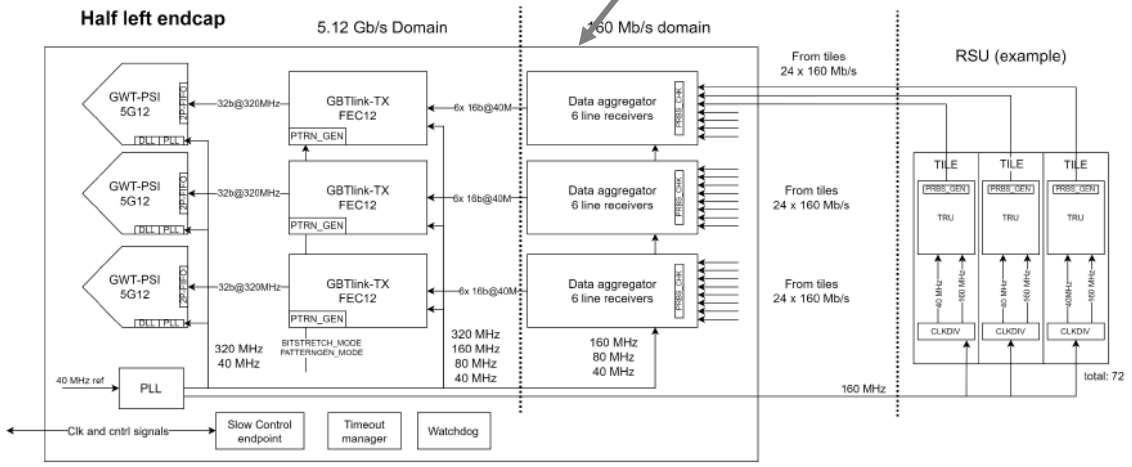
Data Flow – From Tile to Left Endcap



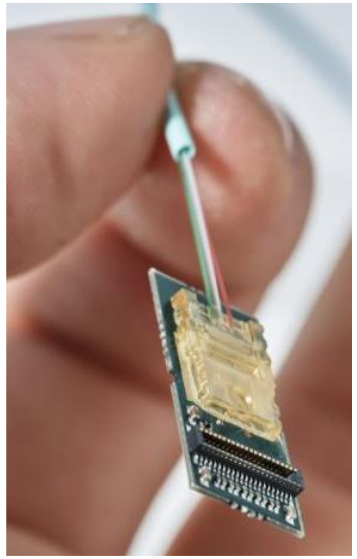






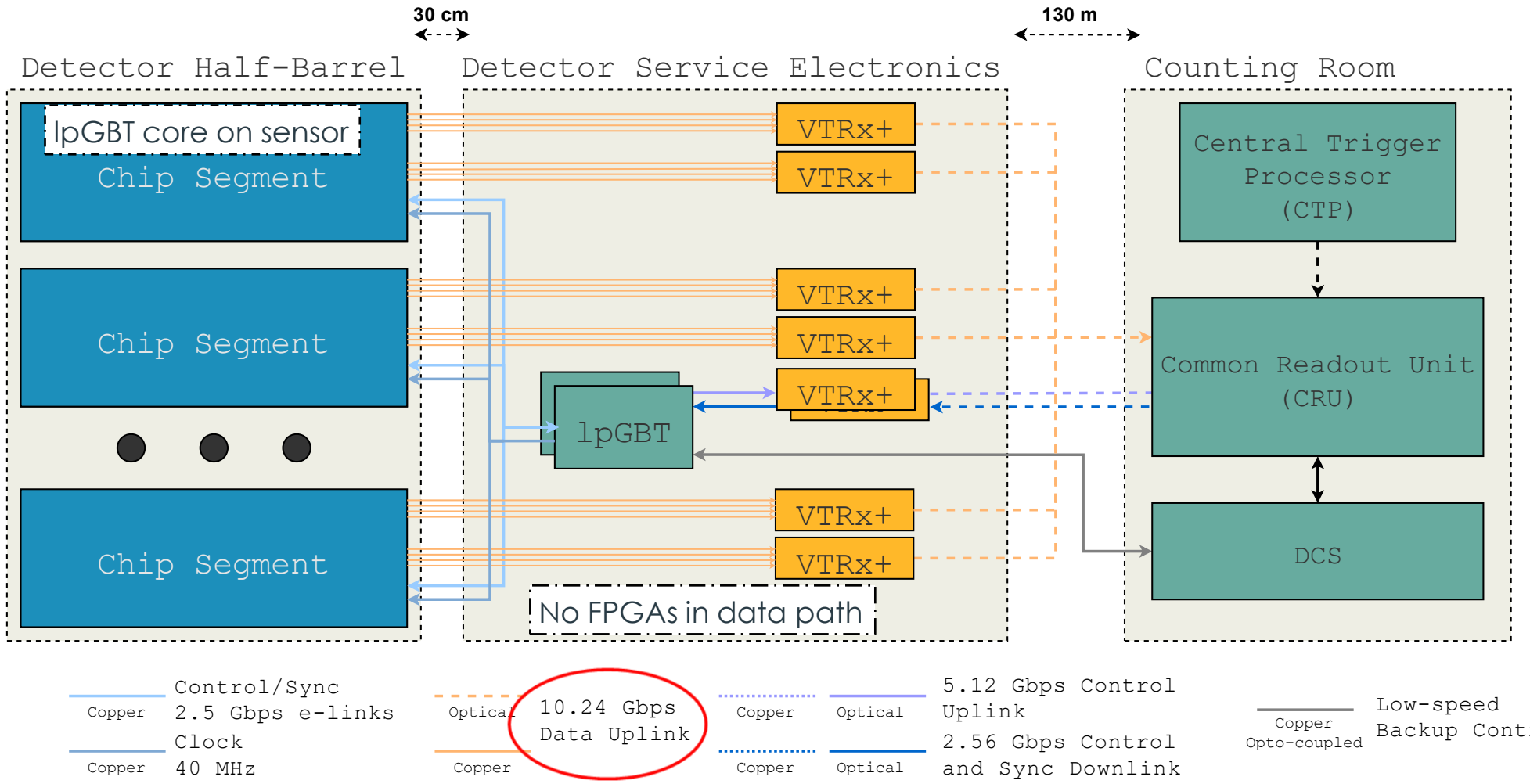
160 Mbps x 144 = 23.04 Gbps (ITS3 expected: 15.55 Gbps)

ITS-3 Detector Electronics – Data & Control



VTRx+

lpGBT



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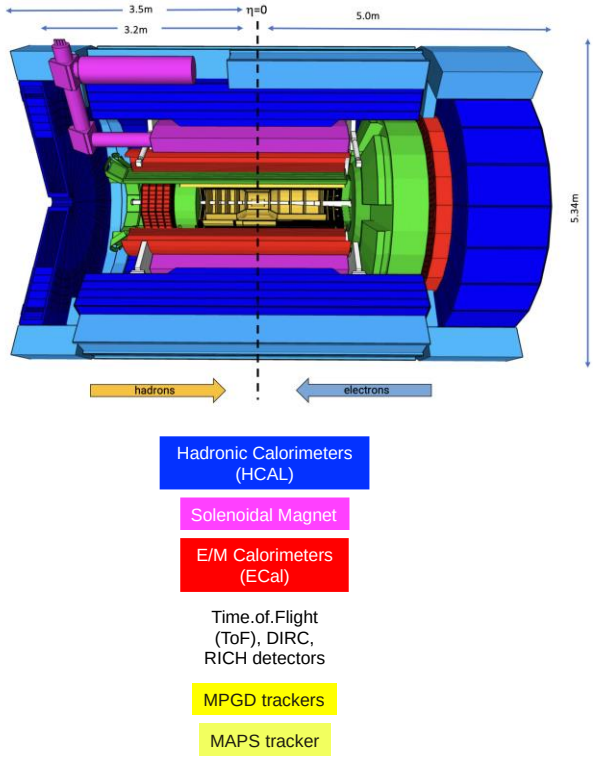
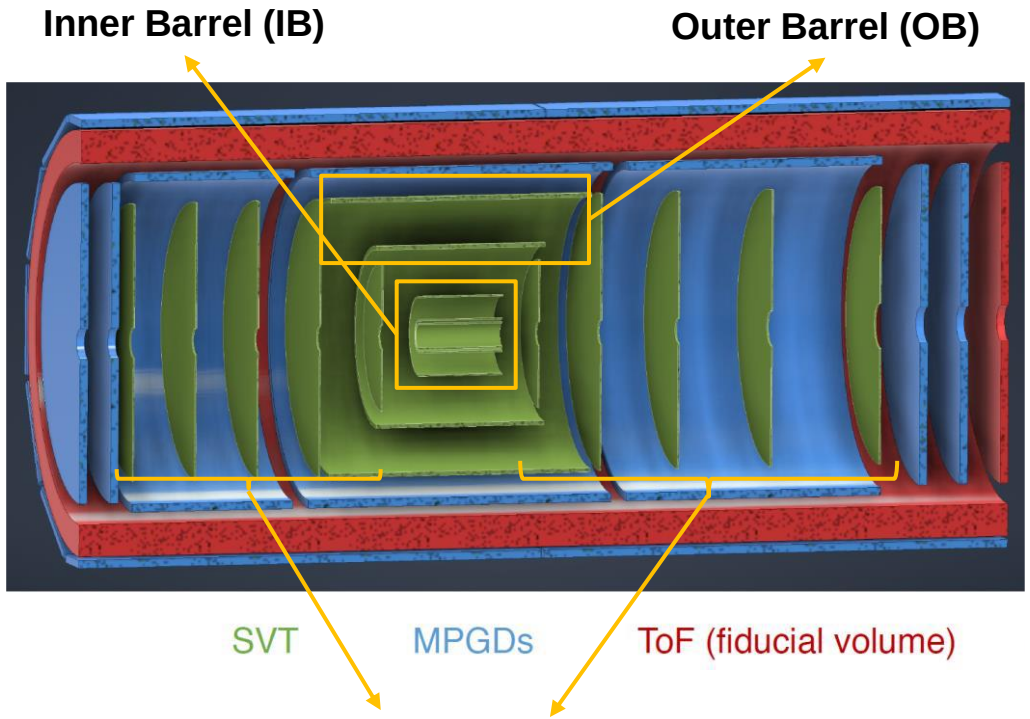
ePIC Silicon Vertex Tracker (SVT)

- Well integrated, large acceptance, high precision Silicon Vertex Tracker based on large area, low power MAPS in 65 nm CMOS imaging technology



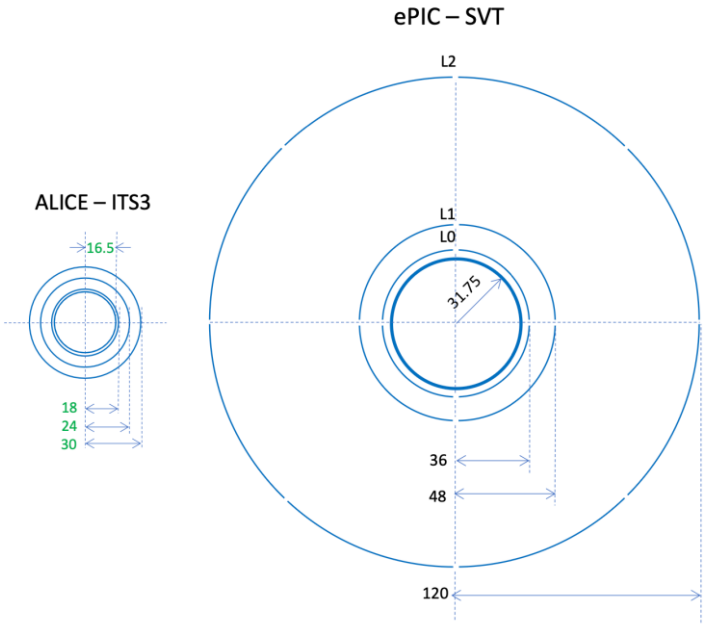


SVT Total (active) area **~ 8.5 m²**

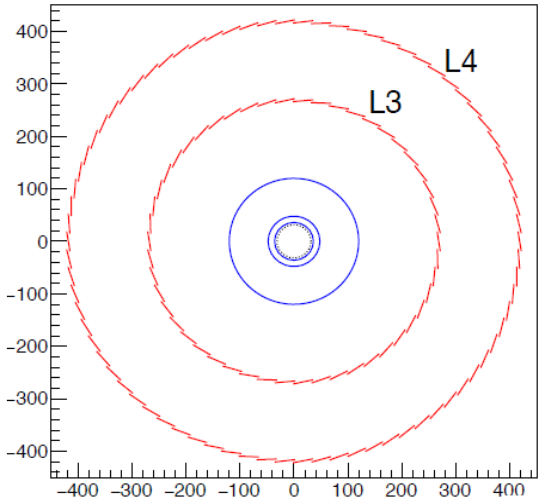
ePIC SVT target specifications	
Spatial resolution	~ 5 um
Power	< 40 mW/cm²
Frame rate	≤ 2 μs
Material budget (per layer)	IB: **0.05%** X/X_0 OB: **0.25, 0.55%** X/X_0 EE/HE: **0.25%** X/X_0

ePIC SVT Barrel & Disks

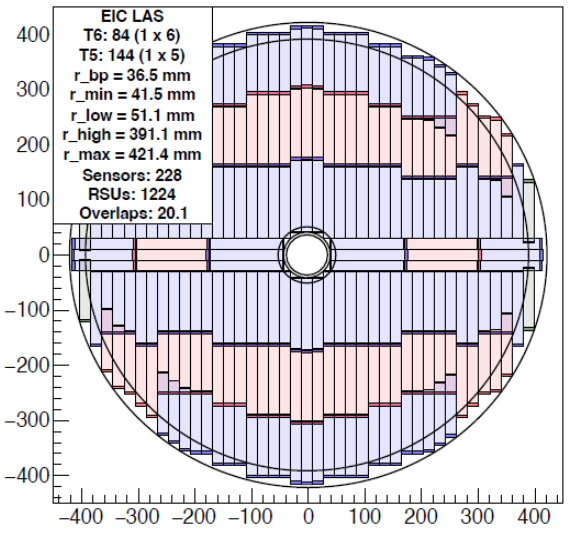
Region	Layer	radius [mm]	length [mm]	X/X0
IB	L0	36	270	0.05 %
	L1	48	270	0.05 %
	L2	120	270	0.05 %
OB	L3	270	540	0.25 %
	L4	420	840	0.55 %



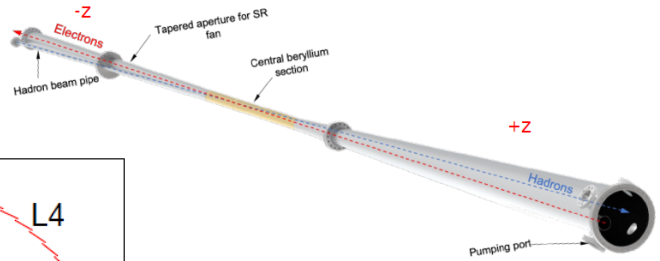
Inner Barrel

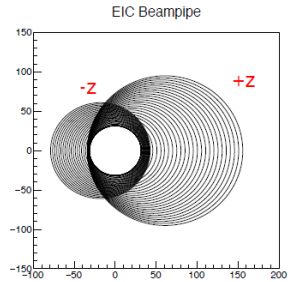


Outer Barrel



ePIC Large Area Sensor (LAS)



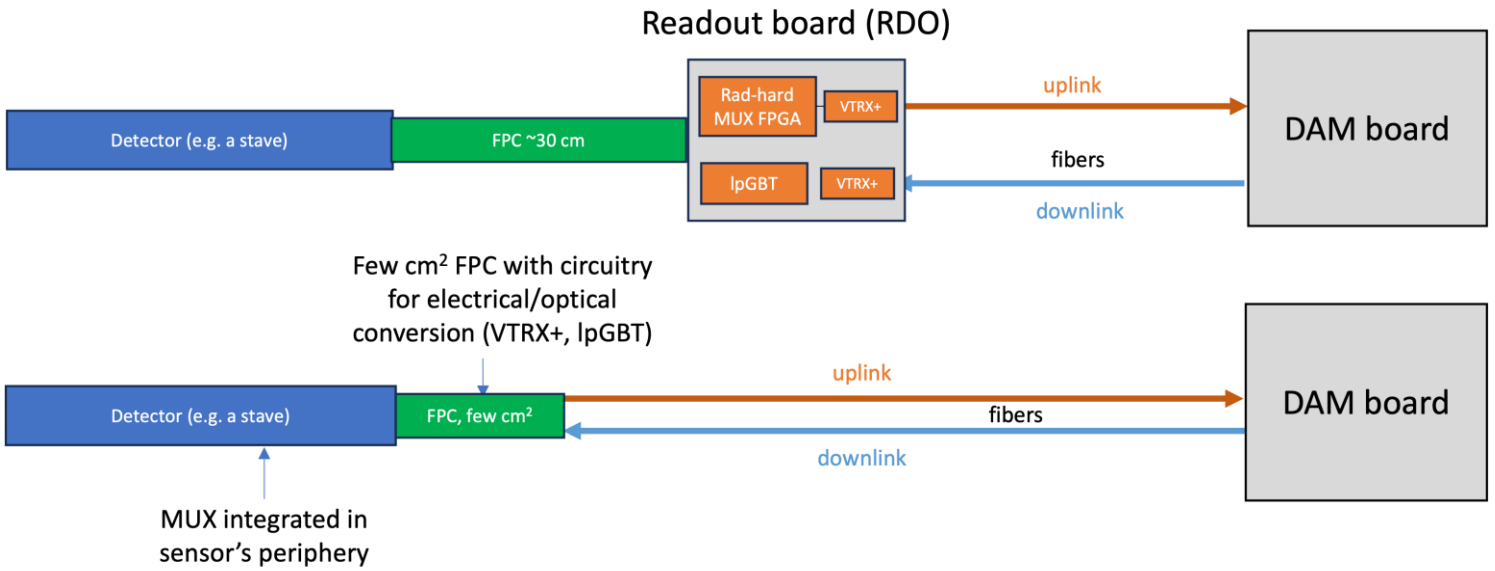


EE/HE	+z [mm]	-z [mm]	r_out [mm]	X/X0 %
ED0/HD0	250	-250	240	0.24
ED1/HD1	450	-450	420	0.24
ED2/HD2	700	-650	420	0.24
ED3/HD3	1000	-900	420	0.24
ED4/HD4	1350	-1150	420	0.24

h & e Disks

ePIC MAPS Readout

- Development of a multiplexing strategy for the output links of the EIC LAS
  - Multiple 5 Gbps links in ITS3 sensor, not needed for the (much lower) data rates at ePIC
- Tow options under consideration
  - External multiplexing using commercial (radiation tolerant) FPGA
  - Multiplexing integrated into sensor ASIC



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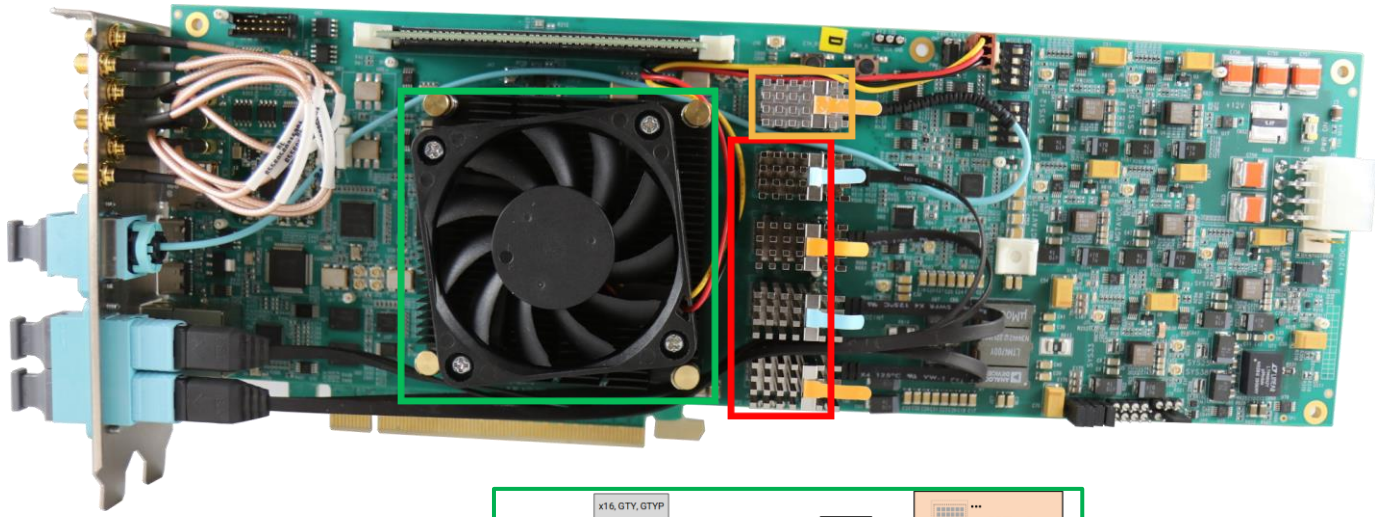
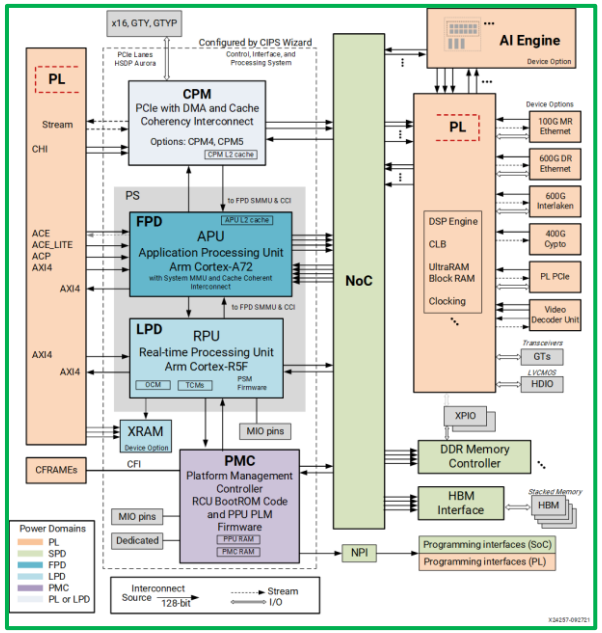
ePIC Backend: ATLAS FELIX Phase II Run 4 hardware

- Based on Xilinx Versal Prime VM1802
  - Dual-core ARM Cortex-A72 Application Processing Unit
  - Dual-core ARM Cortex-R5F Real-Time Processing Unit
  - AI Engine
  - Programmable Logic
  - Future: Versal Premium
- 4 Samtec FireFly transceivers
  - 24 bi-directional optical links (future: 48 links)
  - 10 / 25 Gbps bandwidth per channel
- 1 Samtec FireFly for LTI/TTC links
  - Trigger, Timing and Control (4 links)
  - 100 GbE Networking
- PCIe Gen4 x16 (240Gbps)
  - 2 x8 lanes bifurcated
  - Future: PCIe Gen5 up to 16 lanes

BNL FLX-182 Prototype



Versal Prime



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BACKUP

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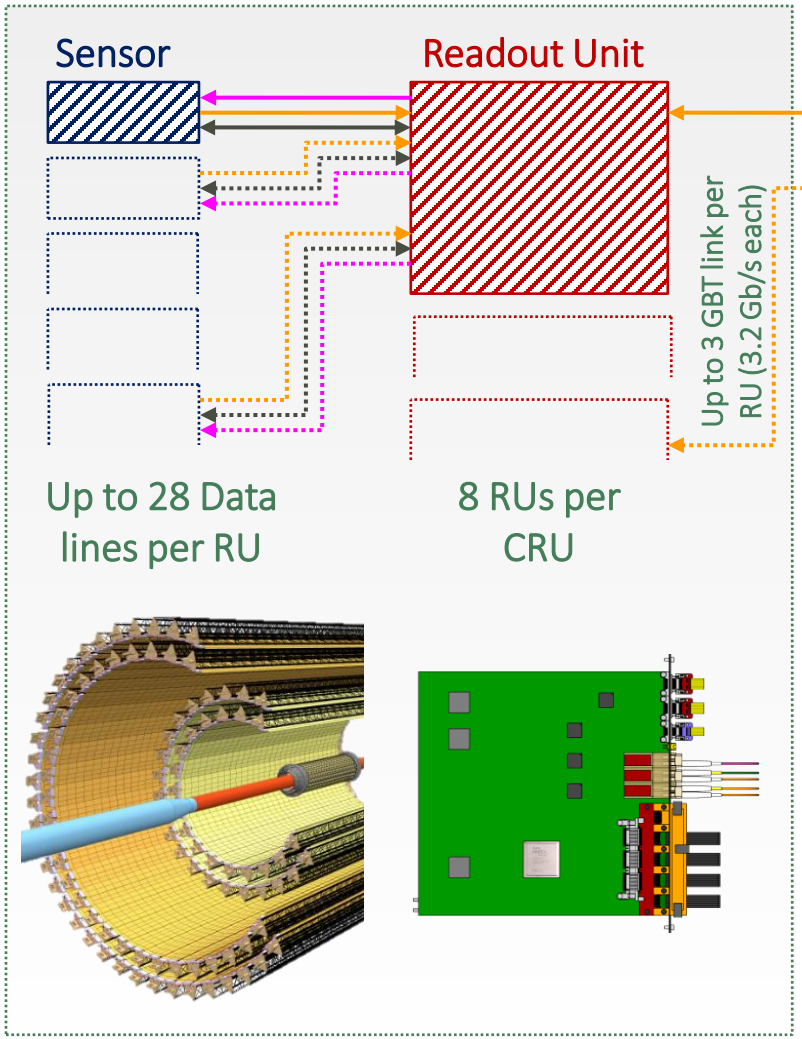
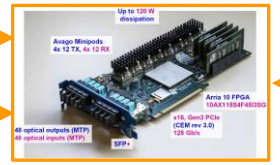
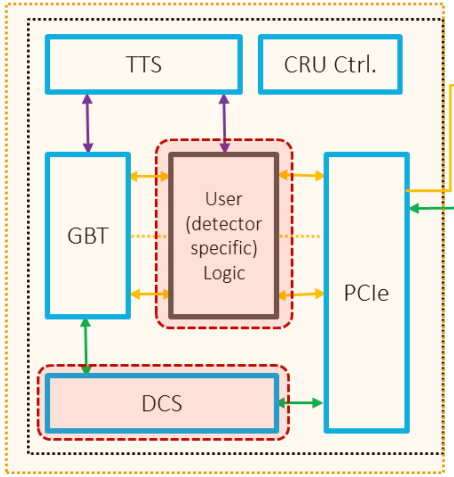
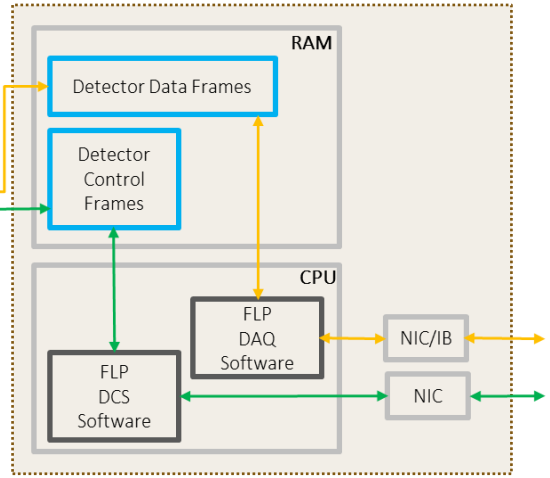
ALICE Data Acquisition: First Level Processors with CRUs





2 CRUs per FLP





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FELIX Firmware

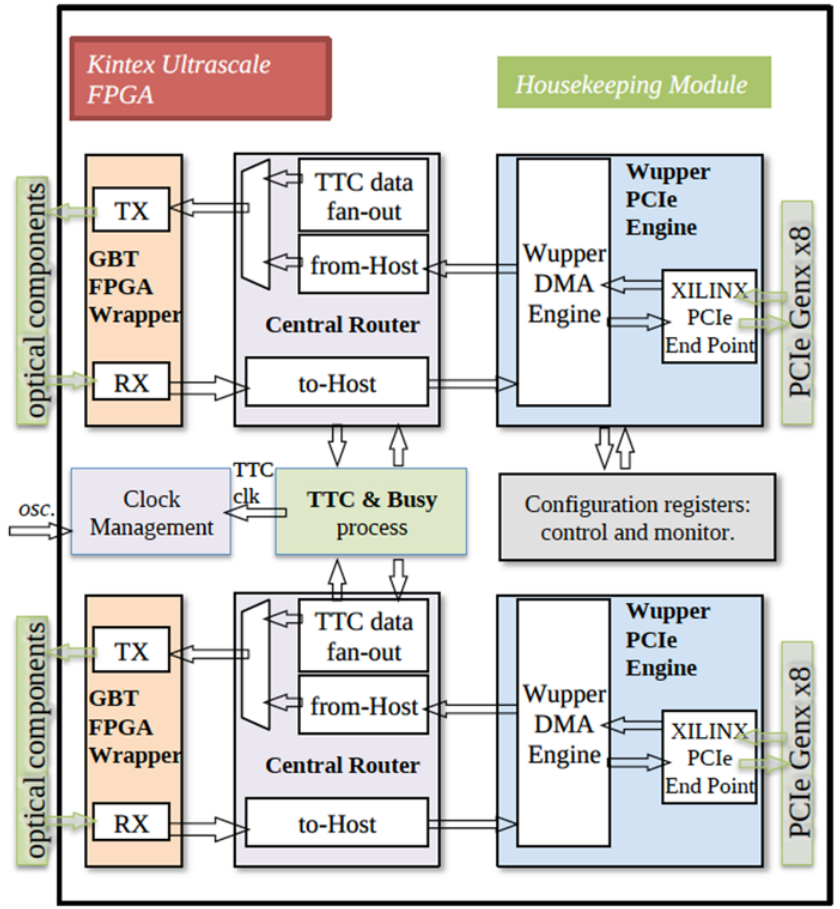


Fig. 5. Block diagram of the FLX-712 firmware

arXiv:1806.10667v1

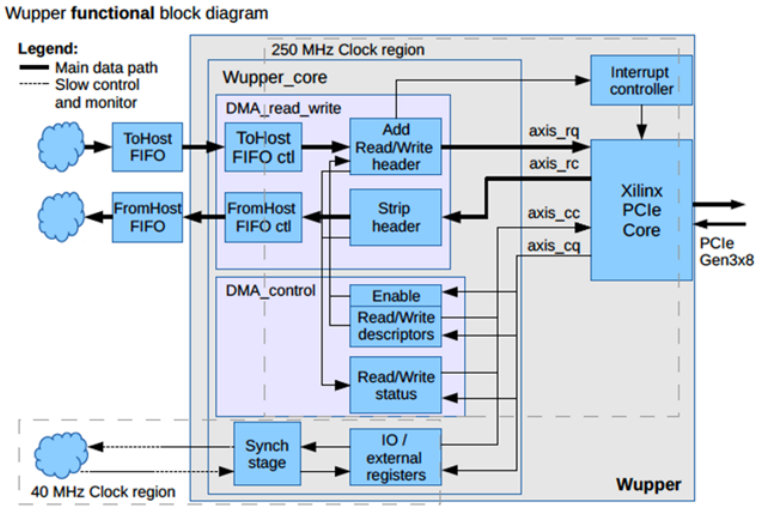
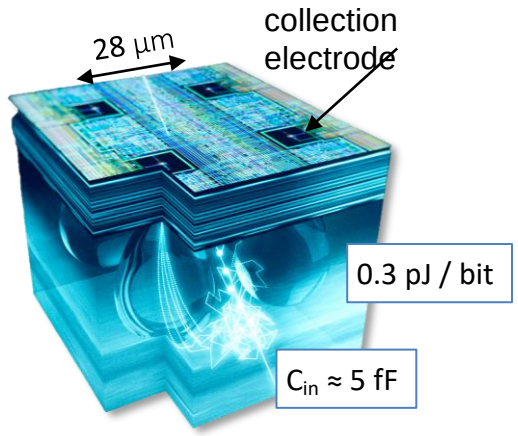


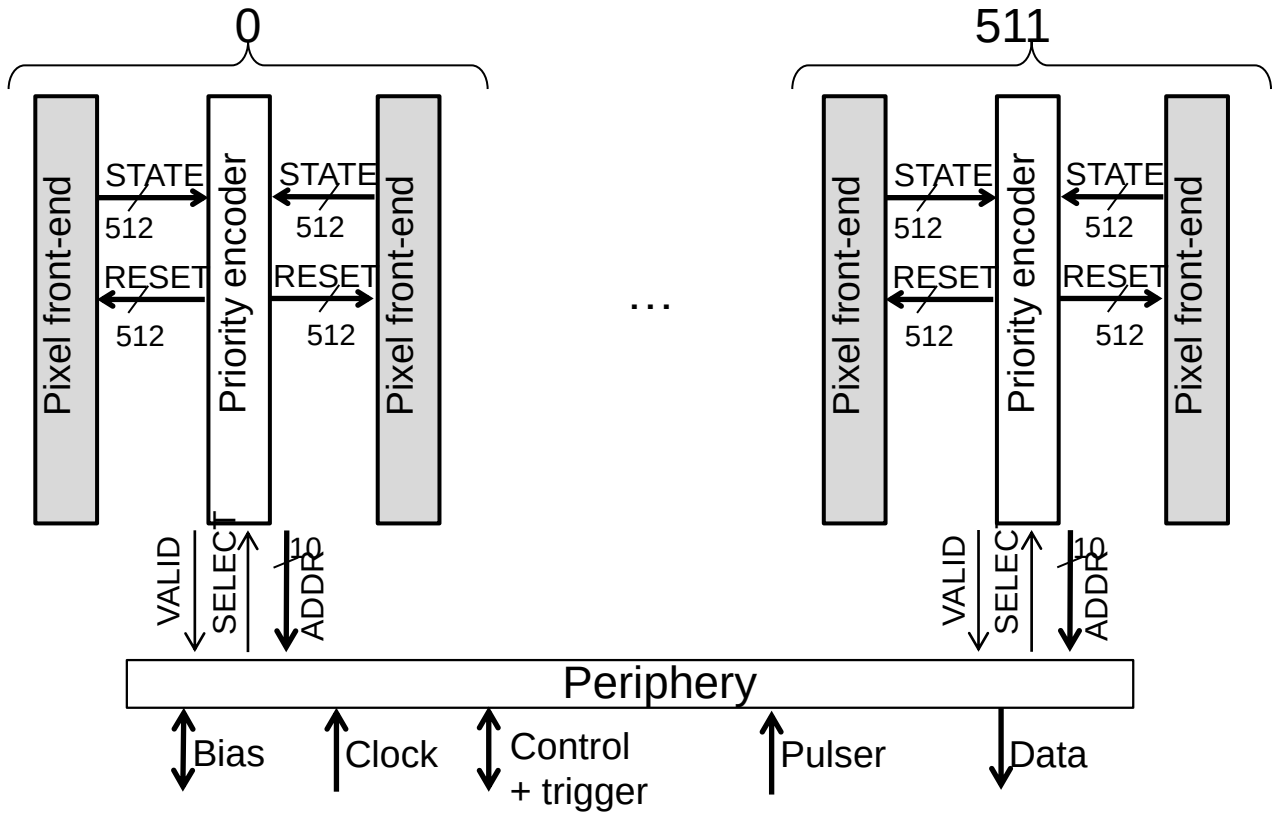
Fig. 6. Structure of the Wupper PCIe engine

Matrix Readout



2 x 2 pixel volume

Q_{in} (MIP) ≈ 1300 e ⇨ V ≈ 40mV



low-power matrix readout ~ 2mW

Pixel Matrix - Hit driven architecture

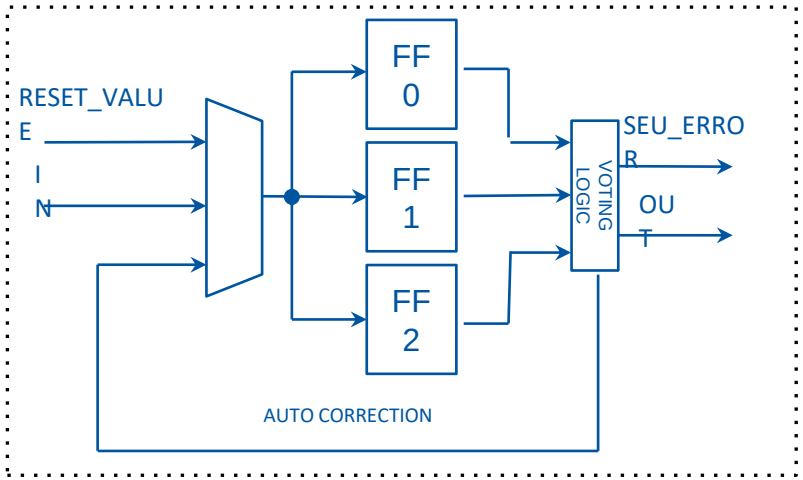
- Priority encoder sequentially provides addresses of all hit pixels present in double column
- No activity if no hit (**no free running clock**) ➔ low power

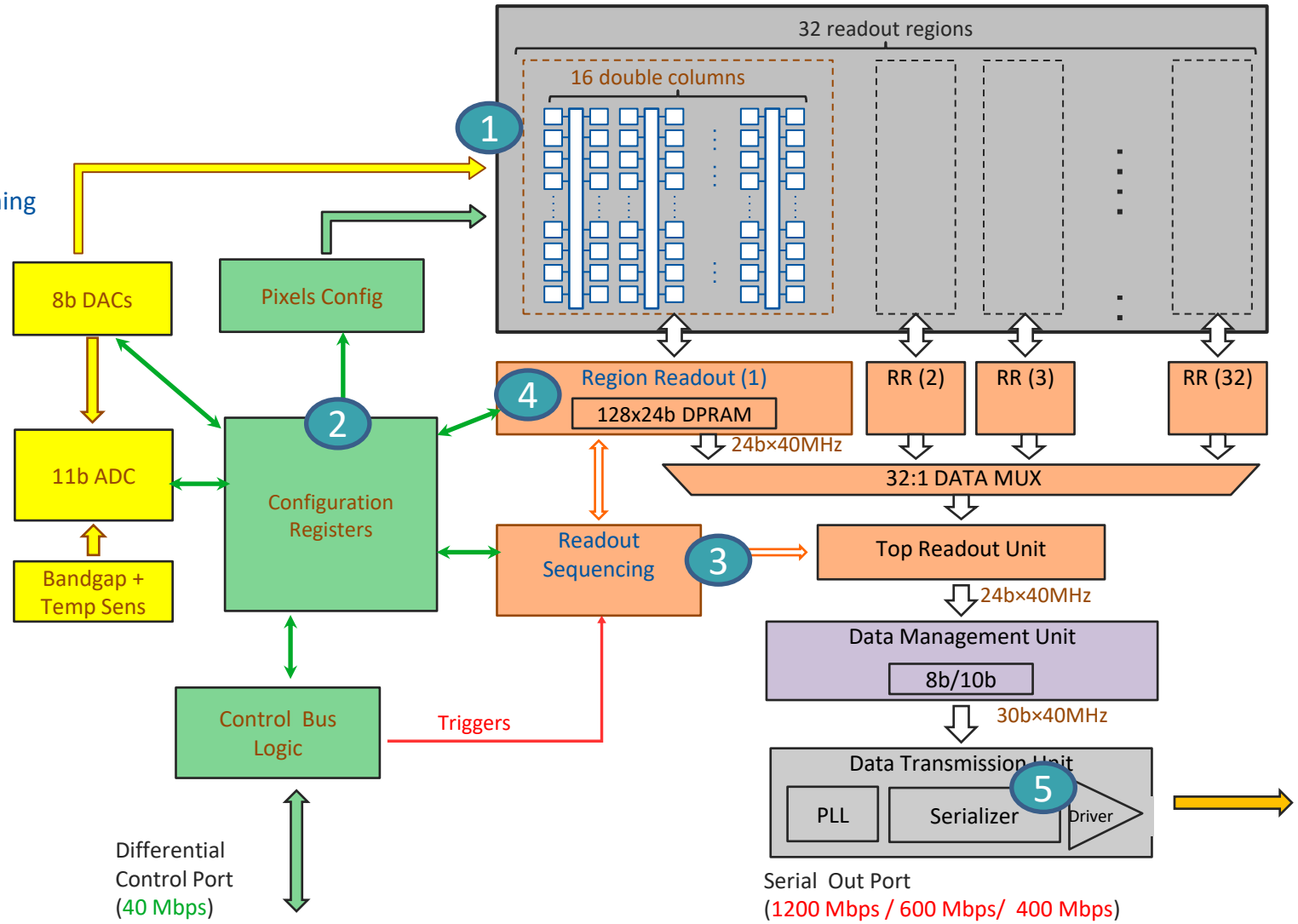
ALPIDE Architecture

ALPIDE elements potentially SEU sensitive

1. Pixel Logic: mask and pulse registers (not protected)
Mitigation : Refresh pixel mask bits in background
2. Periphery logic: state machine, FIFO pointers, counters and configuration registers with TMR
3. Top readout unit and data management unit FIFO with Hamming protection
4. Region Readout DPRAM partially protected
   format protected
   hit data not protected
5. Data Transmission Unit: PLL and Serializer with TMR

Basic **T**riple **M**odular **R**edundancy register cell





ALICE Server/GPU Farms for Data Acquisition and Online Processing

Data Acquisition Servers & Electronics

- 13 “First level Processors” (FLP)
  2 CRUs & 8TB of local storage each
- Storage Farm for commissioning:

  200 TB local disk server + 500 TB cloud storage
- **Event Processing Nodes (GPU Farms)**