eRD109 FY23 Report and FY24 Proposal on EIC AC-LGAD ASIC and Electronics R&D

BNL: Prithwish Tribedy (ptribedy@bnl.gov)
FNAL: Artur Apresyan (apresyan@fnal.gov)
IJCLab: Dominique Marchand (dominique.marchand@ijclab.in2p3.fr)
ORNL: Oskar Hartbrich (hartbricho@ornl.gov)
Rice: Wei Li (wl33@rice.edu)
UCSC/SCIPP: Matthew Gignac (mgignac@ucsc.edu)
UIC: Zhenyu Ye (yezhenyu@uic.edu)

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1 Executive Summary

$192k fund in FY23 has been approved to support the work on frontend ASICs (EICROC, FCFD, ASROC/HPROC/FAST), and low mass kapton printed circuit board (PCB) for AC-LGAD detectors. At the time when this report is submitted (July 7, 2023), the usage of the fund for the kapton PCB has been authorized, while the paperwork for the other funds is still in progress. This has a significant impact on our progresses. Below we summarize what has been done in FY23 and what we propose to do in FY24.

In FY23, IJCLab, Oemga and CEA/Irfu have made progresses in characterizing EICROC0 despite some unexpected delays. While the charge injection circuit, pre-amplifier and TDC all function individually as expected, we observe a cross-talk between TDC clock and preamplifier leading to an

enhanced noise level in the TDC output, and unexpected wider pulse shape and noise structure in the ADC output. We plan to continue our investigation into EICROC0 to understand the noise issue(s), and submit an intermediate version (EICROC0_v1) using the approved FY23 fund with issue fixed. In the meantime, we will work on incorporating a low power consumption ADC design into the next main version EICROC1 that will implement EIC clock frequency and EIC detector specific requirements, as well as possible optimization in the PA, discriminator and TDC based on what we will learn from EICROC0_v1. The submission of EICROC0_v1 is anticipated in the first quarter of FY24, while that of EICROC1 is in the third quarter of FY24. We request \$85k in FY24 to cover the costs of EICROC1 submission and associated PCB fabrication.

In FY23 Fermilab has completed the characterization of the single-channel analog-only FCFDv0 chip with charge injection, laser, radiative source and test beam. The performance of FCFDv0 with a novel design of constant fraction discriminator meets all the expectations. The submission of a multi-channel FCFDv1 is scheduled in August 2023 using the approved FY23 fund. For FY24, we plan to follow the same approach as FCFDv0 to characterize FCFDv1. We also plan to complete the design and submit the next version FCFDv2 in the fourth quarter of FY24 that will incorporate digital TDC/ADC/readout circuits. We request \$40k in FY24 to cover the costs of FCFDv2 submission and associated PCB fabrication.

In FY23 UCSC has developed a readout board for a detailed characterization of the analog front-end of the FAST2 ASIC. We confirm the large dynamic range and slower than optimal risetime. We have designed the characterization board for ASROC and waiting for the arrival of the ASIC. In FY24, we request \$45k to complete the characterization of the first ASROC prototype, FAST3 analog amplifier, the second HPSoC v.2 prototype, and develop the specifications for a third-round HPSoC prototype.

In FY23 ORNL has conducted a technological survey to identify potential vendors and their capabilities to produce flex PCBs. We have also obtained several flex PCB foils and tested their HV, ohmic resistance and line impedance. In FY24, we request \$45k to design and fabricate additional prototypes with the ultimate goal of producing a functional full size demonstrator of the flex PCB that connects at least one readout ASIC and sensor assembly on one end to a RDO prototype on the other end. Moreover different interconnect technologies will be explored to identify the most cost effective approach for sensor-ASIC hybridization.

To read out the ASICs described above, dedicated frontend electronics need to be designed and fabricated to provide the necessary clock and slow control signals to the ASICs as well as receive, aggregate and submit the readout data out of the spatially constrained detector volume. We request \$216k in FY24 to support such efforts to be carried out at BNL, Rice, UIC and ORNL.

Our total budget request in FY24 is \$445k, as summarized in the table below. In the follow sections we give a detailed report on the FY23 work and FY24 proposal.

Inst.	Labor (k\$)	M&S (k\$)	Total (k\$)
IJCLab	-	85	85
FNAL	-	40	40
UCSC	38	7	45
ORNL	10	35	45
BNL	120	17	137
Rice	45	4	49
UIC	30	4	33
Total	243	192	435

Table 1: eRD109 total budget request for AC-LGAD ASIC and electronics R&D in FY24.

2 eRD109 FY23 Report

2.1 eRD109 FY23 Report - EICROC

While specific ASICs have been designed to readout DC-LGADs of ATLAS HGTD and CMS ETL, namely ALTIROC [8, 9, 11] and ETROC [10] respectively, the development of a dedicated ASIC optimized to readout novel fine pixelated AC-LGAD sensors is mandatory to fully exploit their potential in

terms of time and spatial resolutions, taking into account their intrinsic properties: lower capacitance, compare to DC-LGAD, and their charge sharing capability between adjacent pads, which provides an excellent spatial resolution but requires a sensitivity to low charges (2 fC). Besides, in the context of the EIC Far-Forward detectors, such as the Roman Pots, the specifications for the final readout chip (32×32 channels), with a pitch size of 0.5×0.5 mm^2) include a low power consumption (1 mW/channel), as placed in vacuum in a very limited space and an electronic noise smaller than 1 mV/channel to achieve targeted resolutions: a 30 ps time resolution and a 30 μm spatial resolution. Based of these stringent constraints to achieve for the Roman Pots, the designed EICROC chip should fulfill the requirements of most ePIC detector subsystems forseeing the implementation of pixelated AC-LGAD sensors, such as forward TOF, pfRICH, hpDIRC

The EICROC project relies on complementary teams with expertise in micro-electronics, instrumentation and semi-conductor detector characterization from French institutes (IJCLab, OMEGA, CEA-Saclay/Irfu/DEDIP) and from Brookhaven National Laboratory (BNL) also involved in the design and the production of AC-LGAD sensors for EIC. French institutes involved in the EICROC are providing in-kind labor.

In order to fulfill the requirements of most of the detectors subsystems foreseeing the implementation of AC-LGAD sensors, the objective of the EICROC team is to follow a step-by-step process, designing successive ASIC iterations fixing issues faced during testing, and responding to increasing technological challenges.

Within this framework, relying on the feedback from measurements performed in 2022 with an ALTIROC1_v2 chip wire-bonded to an AC-LGAD (3×3) pixelated sensor, provided by BNL, as well as the measurements performed at BNL with an ALTIROC0 chip connected to a stripped AC-LGAD [12], the specifications of the 1st prototype (4×4 channels), EICROC0, have been defined, as well as the associated Printed Circuit Board (PCB), and fabricated relying on a financial support from the P2IO LabEx [13] obtained for the period 2021-2022. The resulting EICROC0 schematics associated to 1 channel/pixel/pad, illustrated on Fig. 1, includes:

- an analogical fast Transimpedance (TZ) pre-amplifier and a discriminator taken from ALTIROC ASIC design (ATLAS),
- a 10 bit Time-to-Digital Converter (TDC) measuring the Time-of-Arrival (ToA). This TDC, designed by CEA/Irfu/DEDIP (France) originally for HGCROC (CMS) [14, 15, 18], has necessitated a challenging spacial adaptation to fit within the reduced surface of a pad (0.5×0.5 mm^2),
- a 8 bit Analogical-to-Digital Converter (ADC), designed and adapted by AGH University of Science and Technology (Krakow, Poland) from the HGCROC 10 bit ADC. Compared to the ALTIROC chip, holding 2 TDCs, one to measure the TOA and the second one associated to the Time-over-Threshold, an ADC has been preferred to measure the signal amplitude to avoid non linear behaviour of a ToT TDC as a function of injected charge.
- an I2C slow control taken from HGCROC,
- digital readout: FIFO depth 8 (200 ns),
- 5 slow control bytes per pixel:
  - 6 bits local threshold,
  - 6 bits ADC pedestal,
  - 16 TDC calibration bits,
  - several on/off and probes

In 2023, in close collaboration with partners within eRD109 and eRD112 consortia (periodic meetings), the activities of the EICROC team has been focused on EICROC0 test bench setting-up and

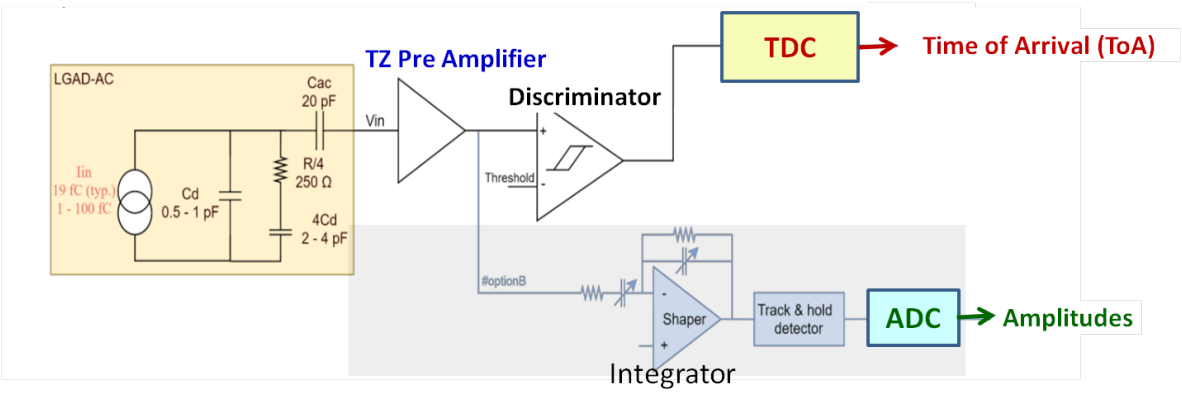

Figure 1: Schematics of one EICROC0 channel. Analogical fast transimpedance (TZ) preamplifier (PA) signals are sent, on the one hand, to a TDC to measure the Time of Arrival (ToA) and, on the other hand, to an integrator (shaper), slowing down PA signals, followed by an 8-bit ADC measuring the distribution amplitude resulting from the deposited charge.

performance characterization of electronics response from boards holding an EICROC0 in view of driving the next EICROC ASIC iteration.

The dedicated printed circuit board (PCB, referred as test board), associated to EICROC0 chips, has been designed by the OMEGA team. Main components are level translators (1.2V and 2.5V), on-board regulators for low voltage, 4 SMA connectors for pre-amplifier signal output. Space have been left near the chip location to accommodate for AC-LGAD sensor wire-bonding. Ten PCBs were delivered and partially cabled at IJCLab. Some EICROC0 chips were then wire-bonded to PCBs by the BNL team. Fig. 2 (left) represents a picture showing an EICROC0 chip wire-bonded on a PCB. The firmware and the software associated to a ZC706 Xilinx board acting as the interface board to control EICROC0 parameters have been developed by the IJCLab team. The picture on the right of Fig. 2 represents the EICROC0 test bench, the test board is connected to the Xilinx interface board through a FMC (FPGA Mezzanine Card) connector. After solving several issues, among which the main one was the non availability to exploit the injection charge system, the first EICROC0 test bench has been operational since March 2023 at IJCLab. Since then, a second one has been set up at OMEGA and we are currently working to have another one at BNL and later on at CEA/Irfu in order to be more efficient in characterizing the EICROC0 chip.

A charge injection system, referred as the command pulse (CMD_Pulse) is used to characterize the electronics response of the EICROC0. The CMD_Pulse signal amplitude is controlled by a 6 bit DAC (Digital to Analog Converter). Given a 100 pF input capacitance, the corresponding injected charge range goes from **0.5** to **25 fC**.

Fig. 3 shows the Probe PA pulse shapes (1 per column). From these signals the amplitude and the rise time have been measured. Figure 4 displays the absolute value of the maximum Probe PA signal amplitude versus channel numbers for different injected charge values, from 0.5 fC to 25 fC. For an injected charge value greater than 3 fC, one can observe a decrease of the absolute value of the maximum amplitude for increasing channel numbers within a column. In addition, the amplitude differs from one column to another. These effects were observed with the ALTIROC1_v2 ASIC (ATLAS/HGTD). The Probe PA output signals are not designed to be uniform for each channel.

Fig. 5 shows the obtained rise (fall) time of Probe PA output signals computed from the time difference corresponding to 10 and 90% of the maximum amplitude and for an injected charge value of 13.8 fC. The average rise time value is about 600 ps. A small variation from column to column, as well as a slight variation within one column is observed. This effect is also attributed to the Probe distribution within the ASIC, as already discussed above.

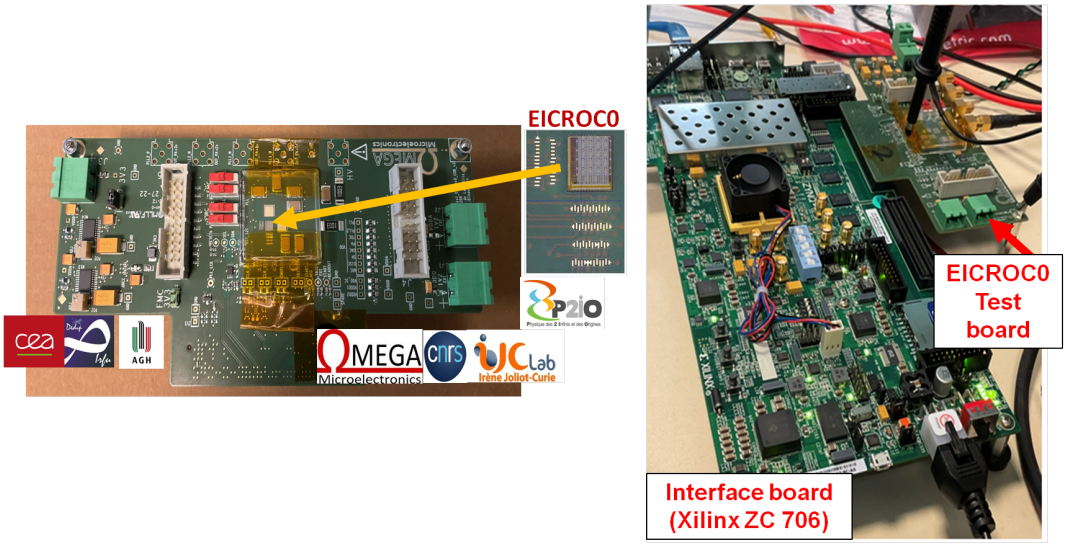

Figure 2: Left: a picture of a PCB with an EICROC0 chip wire-bonded to it. Right: the EICROC0 test bench: EICROC0 PCB is connected to the Xilinx interface board through a FMC connector.

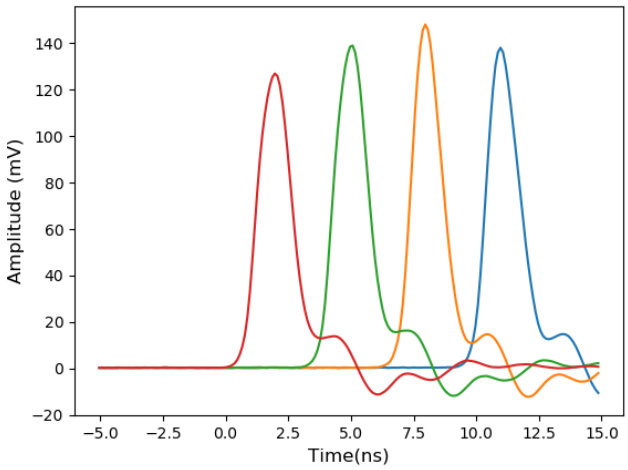

Figure 3: Probe PA output amplitude signals of 1 channel per column, shifted by 3 ns.

The typical Probe PA output noise is about 1.3 mV. The resulting signal to noise ratio is shown on Fig. 6: it ranges from 6 up to 100 for an injected charge from 0.5 to 25 fC.

The Probe PA jitter has been extracted using a CFD method and is displayed on Fig. 7 as a function of the injected charge. The measured Probe PA jitter is below 20 ps for an injected charge $\geq$ 6 fC, and is as low as 8 ps for a 25 fC injected charge, demonstrated the good performance of the pre-amplifier.

All previous results have been obtained with the 160 MHz clock off. This clock drives the TDC and provides the 40 MHz (160 MHz/4) which is used for ADC sampling. When this clock is on, a large noise coupling on the Probe PA output, coherent over all channels, is observed, as shown on Fig. 8, resulting in a noise increase by a factor 10. Such a noise strongly limits a precise time measurement with the TDC. This effect has not been observed with the ASIC simulation and this issue has to be

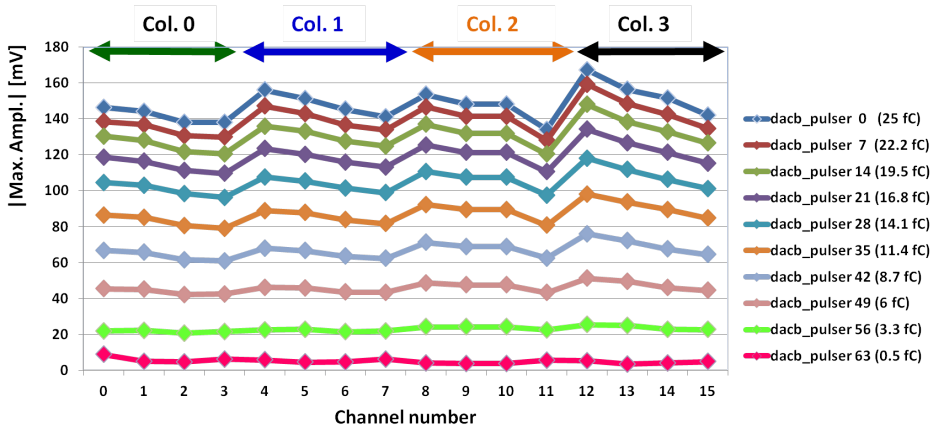

Figure 4: Absolute value of the maximum Probe PA amplitude versus channel numbers for different injected charge values.

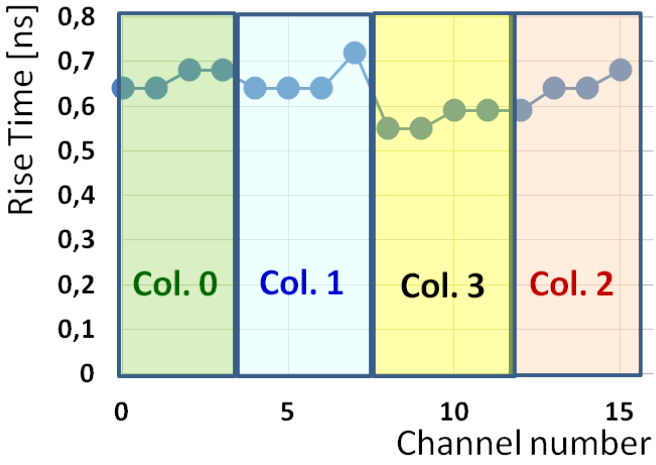

Figure 5: Rise time computed between 10 to 90% of the maximum amplitude for an injected charge of 13.8 fC.

further investigated to identify the origin of the coupling (ground PA, PCB, ...).

Although the noise observed on Probe PA output signals, some of the TDC and ADC intrinsic performances can be studied.

The TDC quantification step has been extracted by shifting the CMD_pulse signal by a precise tunable delay: a value of 24.4 ps has been measured, in fair agreement with the nominal value of 25 ps. Finer tuning of the TDC quantification step can be done using slow control parameters.

With the large noise observed, the time resolution obtained for a signal channel is about 115 ps, much larger than expected. Nevertheless, this noise, being coherent between all channels, can be removed by looking at the time difference between two channels. Fig. 9 shows such a distribution with a RMS of 19.7 ps. Assuming an identical time resolution on each channel, the estimated TOA resolution would be 14 ps (19.7 ps / $\sqrt{2}$) for an injected charge of 25 fC. This result shows that the TDC works as expected.

The performance of the ADC has also been studied. Fig. 10 shows a typical pulse shape for an injected charge of 25 fC. This pulse shape is broader that the expected signal and a 8-fold noise struc-

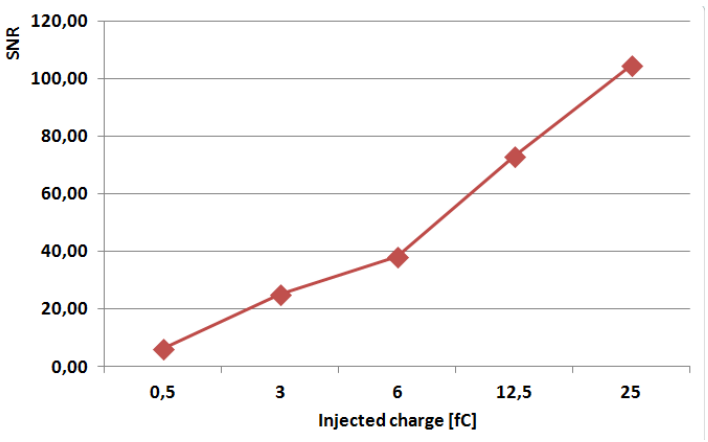

Figure 6: Channel 0 signal to noise ratio as a function of the injected charge.

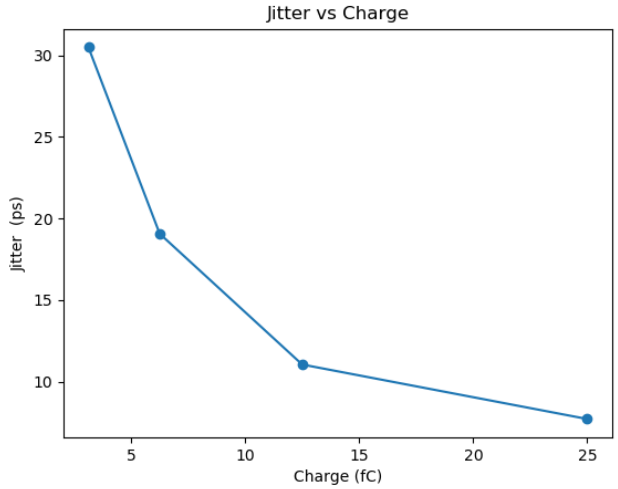

Figure 7: Extracted Probe PA jitter for channel 0 as a function of the injected charge.

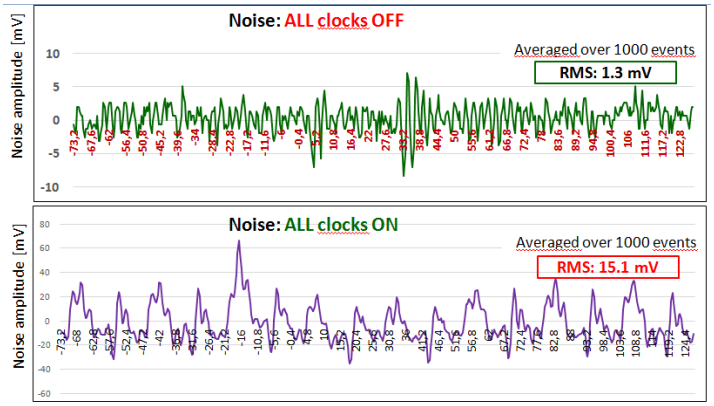

Figure 8: Probe PA output when the 160 MHz clock is OFF/ON. A clear coupling to the clock is observed with a RMS noise increasing from 1.3 to 15.1 mV.

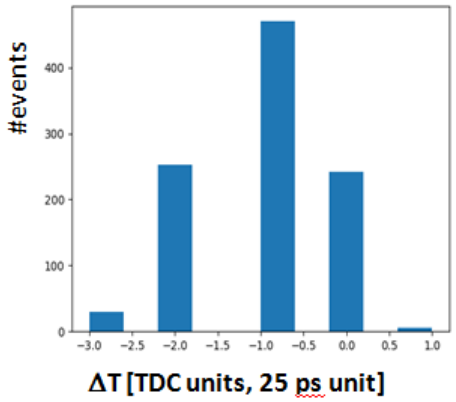

Figure 9: Time difference (ΔT) distribution in TDC units (25 ps). The RMS of this distribution is 0.79 in TDC units, corresponding to 19.7 ps.

ture has been observed. These effects are attributed to the shaping stage at the ADC input and needs to be further investigated.

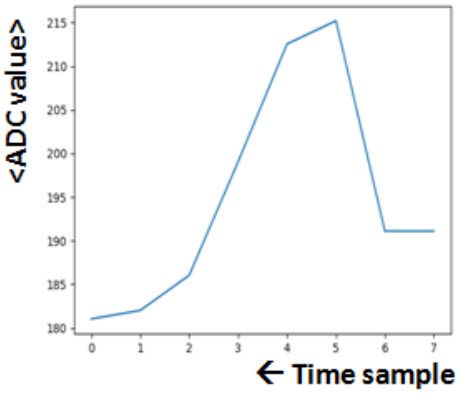

Figure 10: Typical ADC average value versus ADC time sample numbers.

The above results show that the pre-amplifier alone and the TDC alone satisfy the EIC requirements. Measurements with an AC-LGAD connected to an EICROC0 will start soon using the Probe PA output (charge sharing, Beta source, ...).

During FY23, after a non expected slow beginning due to successive issues (delays in delivery, charge injection system not available, decoding, ...), the EICROC0 test bench installed at IJCLab became operational only in March 2023. This led to an approximate delay of 6 months compared to the provisional schedule presented last year before being able to characterize the 1st prototype, EICROC0. Besides, within the framework of this R&D project, the testing of EICROC0 prototype have shown integration effects (160 MHz clock coupling to Pre-Amplifier inputs, preventing TDC time measurements, 8-fold noise structure showing up at the level of the ADC) that require to be further investigated, understood and fixed before ramping up in designing the next ASIC iteration. In that context, within our stepping process, an intermediate iteration (EICROC0_v1) with updated associated PCB will be firstly favored before designing a larger size ASIC, such as EICROC1, including a low power ADC and being compatible to EIC clock.

***The EICROC project has received funding from the LabEx P2IO [13] (Université Paris-Saclay, France) for the period 2021-2022 within the call "Projets Emergents" (AC-LGAD Project).

2.2 eRD109 FY23 Report - FNAL

Design of the front-end electronics capable to extract precision timing information from LGAD sensors presents many challenges but plays a key role in the applications of the LGAD technology. The Fermilab and UIC team has been studying optimal methods for extraction of timing information from LGADs, using either Leading Edge (LE) or Constant Fraction Discriminator (CFD). Timestamping using the LE requires time-of-walk correction for optimal time resolution of the reconstructed signal, due to the dependence of the threshold-crossing on the signal amplitude. The CFD discriminant does not require such a correction and is therefore much simpler to operate and implement in large systems, without a need to derive and monitor signal dependence as the detector ages. Additionally, our studies in [16] showed that CFD outperforms LE for smaller signals, making it a preferred choice for AC-LGAD sensors which have smaller signals in non-primary channels due to signal sharing.

Following the studies presented in [16] the Fermilab team designed and produced the single-channel version an ASIC based on the CFD concept using TSMC 65nm technology (Fermilab CFD version 0, or FCFDv0), summarized in Ref. [17]. The FCFDv0 uses several new techniques to achieve low power, area, jitter, time walk. This enables a simple and robust timing measurement (30 ps) of LGAD signals that vary in amplitude by at least a factor of 10, with no critical threshold setting or corrections required. The FCFDv0 is a single-channel ASIC that only contains analog blocks, i.e. the amplifier and discriminator. Another critical feature in the design and implementation of the ASIC was complete testability with simple bench-top equipment, to properly characterize and adjust the settings on the chip for optimal operation.

During FY23 we performed detailed characterization of the performance of the FCDFv0 chip by measuring time resolution and mean time response under various experimental scenarios including charge injection, laser light injection, beta particle source, and proton beam. These results collectively demonstrate a consistent and high level of performance, and represents a successful demonstration of the utility of the CFD ASIC readout chip concept.

The FCFDv0 chip was designed with a special charge injection mechanism for performance validation. The pulse shape of the injected charge is based on simulated LGAD signal pulses and is representative of minimum ionizing particle signals. Using this charge injection mechanism, we scan the size of the injected signal charge between 4 and 26 fC, and measure the corresponding time resolution and mean time response as shown in Figure 11. We obtain time resolution better than 8 ps at the highest injected charge. Between 6 and 26fC, we observe a stable time response and no evidence of residual time-walk, thus validating the effectiveness of the CFD concept.

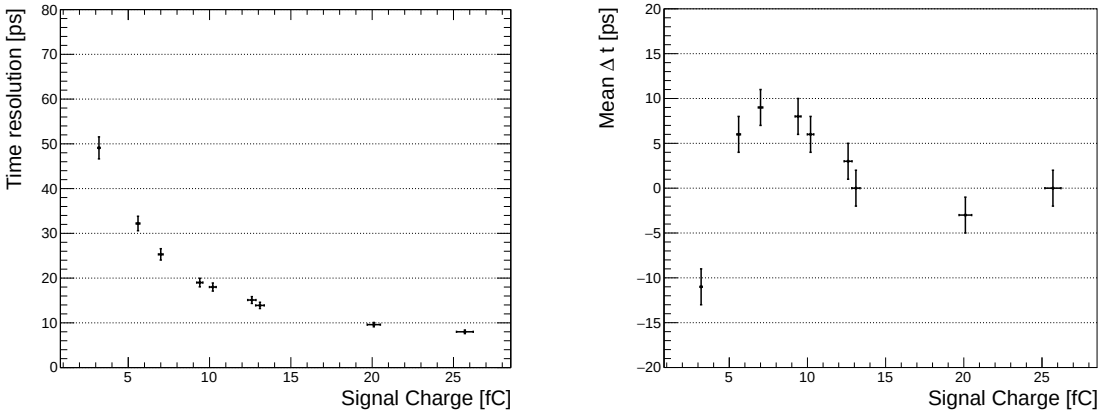

Figure 11: The time resolution (left) and mean time response (right) as a function of the FCFDv0 internal injected signal charge.

With a picosecond pulsed laser, we illuminate the LGAD sensor with photons to mimic the response of a minimum-ionizing particle. The intensity of the laser is varied to scan a range of signal sizes between 3 and 40 fC. The time resolution and mean time response of the FCFDv0 chip is measured as a function of the signal charge, shown in Figure 12. We observe time resolutions similar to the charge

injection measurement. For charge above 30 fC, beyond the design specifications, the FCFDv0 chip begins to saturate and the time resolution becomes increasingly worse for larger signals. The range of signal charge appropriate for the chip will be enlarged in the next version of the chip to accommodate larger signals. The mean time response is also observed to fall within a 10 ps window for charge above 6 fC, consistent with the charge injection measurement.

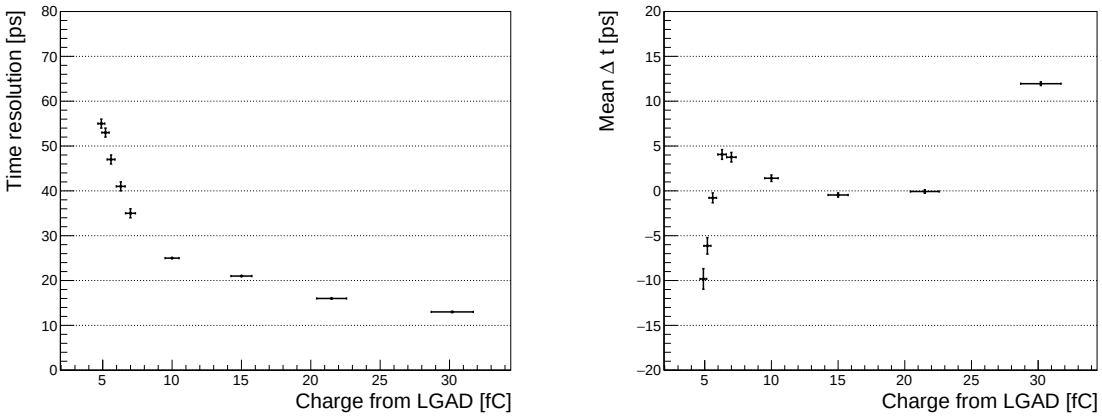

Figure 12: The time resolution (left) and mean time response (right) as a function of the charge of the detected laser signal.

Using the FTBF facilities, we measure the performance of the FCFDv0 chip for 120 GeV protons. On the left of Figure 13, we show measurement of the efficiency for the FCFDv0 chip to produce a valid signal as a function of the proton impact position on the LGAD sensor. We observe an excellent signal efficiency across the surface of the sensors showing the FCFDv0 chip was able readout all signals sent by the LGAD at a trigger rate of about 25 kHz. On the right of Figure 13, we measure the time resolution as a function of the bias voltage applied on the LGAD sensor. At the nominal operating bias voltage of 220 V, we measure a time resolution of about 36 ps, similar to the beta source measurement. Accounting for the impact of the intrinsic time jitter due to Landau fluctuations in the LGAD sensor and the time resolution of the MCP-PMT reference detector, this result again implies a time resolution of the FCFDv0 chip consistent with all previous measurements presented, including the the charge injection, laser signal injection, and beta source measurements.

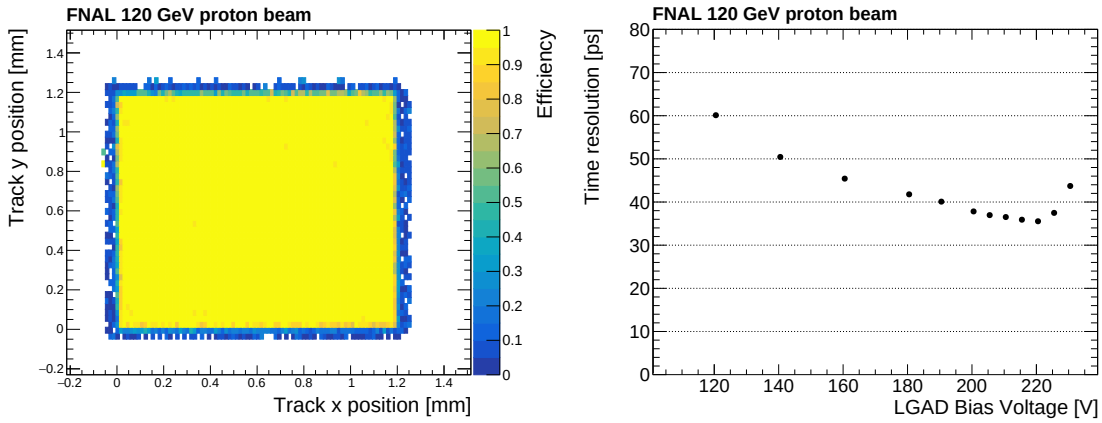

Figure 13: Efficiency as a function of the proton impact position along the horizontal (x) and vertical (y) positions measured using the test beam telescope (left). Time resolution measured as a function of the bias voltage applied to the LGAD sensor for 120 GeV protons (right).

2.3 eRD109 FY23 Report - UCSC

Working along several paths towards an ASIC optimized for EIC detector goals, the SCIPP group has been participating in the development of three separate ASICs with potential applications in an EIC detector. The designs are, variously, focused on improving the timing resolution capability relative to that of systems designed for the LHC timing upgrades, tolerating the larger capacitance associated with strip sensors, and minimizing the per-channel power dissipation. All of these are essential considerations in the design of an EIC LGAD ASIC.

2.3.1 The FAST ASIC Series

The FAST2 ASIC is the latest available prototype in The FAST ASIC series [20]. It is being developed by INFN Torino in a 110 nm CMOS technology as an ASIC optimized for precision timing with LGAD sensors. Along with the EICROC, the FAST development effort is a maturing technology, with both the precision analog front-end and the digital back-end fully under development. The FAST2 ASIC, the latest currently-available member of the family, is a 16-channel device with a three-range, adjustable gain.

During the FY23 period, SCIPP developed a readout board allowing for a detailed characterization of the analog front-end of the FAST2 ASIC, both with calibration inputs as well as in complete detector assemblies Figure 14. A large dynamic range was confirmed, with a signal risetime on the order of 1.5 ns. This risetime is a little slower than optimal for EIC applications. SCIPP awaits the arrival of the FAST3 prototype, the next version in the family, and expects to be able to characterize it with little modification to the existing readout board. As opposed to the other ASIC candidates, FAST are designed to tolerate higher input capacitances, which are faced especially in the strip sensor modules of the barrel-TOF. Reducing the bulk thickness also results in increased AC segment capacitance. To sustain the likelihood of achieving the required timing resolution performance with larger sensors, the FAST3 chip was still included in the evaluation program of SCIPP within eRD109, albeit with lower priority than the other ASICs described here.

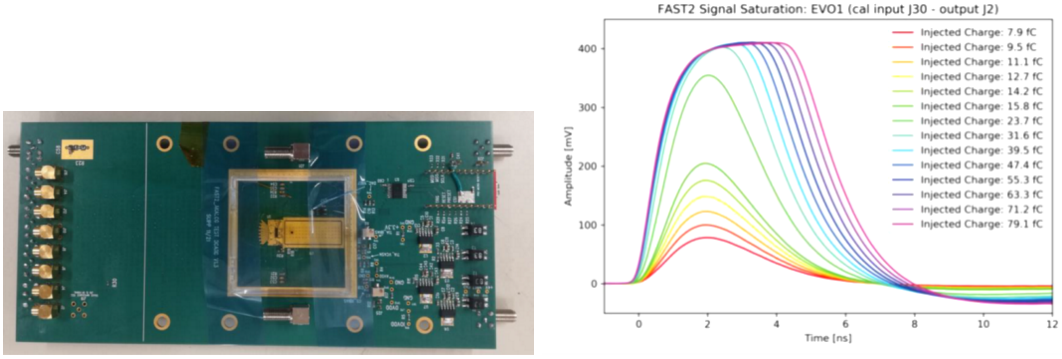

Figure 14: Left: Readout board designed at SCIPP for the characterization of the FATS2 ASIC. Right: Average waveforms observed from the FAST2 analog chain as a function of input calibration pulse amplitude.

2.3.2 The ASROC ASIC

The ASROC, designed in collaboration with SCIPP by Anadyne, Inc., explores the potential advantages of SiGe electronics for use in LGAD readout. During the FY23 period, SCIPP was intimately involved in the development of the design and characterization strategy of the initial ASROC front-end prototype, providing essential input into many aspects of the design and layout of the prototype ASIC. The promise of SiGe seems strong, and working together, the Anadyne/SCIPP team has designed a front-end amplification scheme that promises to provide timing adequate for 20 ps resolution with a per-channel power draw as low as 0.7 mW.

Anadyne has completed the design of the initial 16-channel ASROC prototype, and submitted it for fabrication in a proven SiGe process by TowerJazz. SCIPP has also designed the characterization

board, which is now available in the laboratory and awaits the arrival of the ASROC prototype, expected to be available within the next month. The characterization board, which demands a well-thought-through geometry, high-bandwidth operation, and significant control features, is shown in Figure 15. As of this writing, the board has just been loaded and is awaiting the arrival of the ASROC prototype.

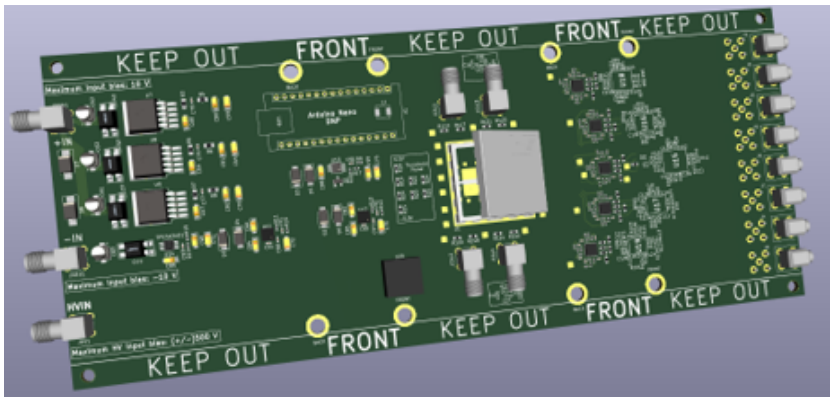

Figure 15: CAD rendering of the ASROC test and characterization board, designed and fabricated in FY23 using eRD109 funding.

2.3.3 The HPSoC ASIC

The HPSoC development project, a joint initiative of SCIPP and Nalu Scientific LLC, is specifically targeted towards maximal timing precision for LGAD readout, with a trans-impedance amplifier (TIA) front-end specifically optimized for AC-LGAD signals for sensors with bulk thickness between 20 and 50 μm. Unique to all other current LGAD readout ASICs, the HPSoC will capture the full signal waveform at a sampling rate of between 10-20 GS/s. Together, these are expected to address the EIC goal of 25 ps timing resolution or better per measured space point. The thin sensor bulk of 50 μm or less is needed to reduce the intrinsic resolution limit caused by charge deposition "Landau" fluctuations in the bulk, but require a co-optimized electronics design to exploit the potential for better resolution.

An initial front-end prototype of the the High-Performance System-on-Chip (HPSoC) ASIC [19] was designed by Nalu Scientific, in close collaboration with SCIPP, and fabricated in 65 nm CMOS by TSMC. In addition to the analog front end, the prototype included test structures to characterize several components of the planned sampling circuitry. A characterization PCB, of similar complexity to that of the ASROC test board, was developed at SCIPP, and used to characterize the front-end amplification system of the four-channel HPSoC prototype ASIC. Figure 16 displays two micrographs of the prototype ASIC, assembled on its characterization board, with its four inputs bonded to pixels in a 3x3 AC LGAD array.

Figure 17 shows the average waveforms accumulated for a 60 μm bulk sensor, as a function of sensor bias (impact ionization gain). The observed risetime of 600 ps is reflective of the intrinsic risetime of the sensor signal, confirming the fast response of the HPSoC TIA amplification system. However, during the characterization of the first chip version during FY23, the overall signal response was roughly a factor of three below design expectations, leading to an overall timing performance somewhat short of expectations. Together with Nalu Scientific LLC, the problem has been identified and the TIA was redesigned. The improved second version of the HPSoC was recently submitted and is being fabricated during the last months of FY23. This second prototype will also contain a significant amount of development of the digital back-end circuitry.

2.3.4 Summary of progress towards EIC goals

Of all the electronics projects currently underway, the HPSoC effort is the CMOS approach that is perhaps the most directly optimized for EIC applications. The front-end amplification scheme, combined with the full waveform digitization, are geared directly towards exceeding the 25 ps timing

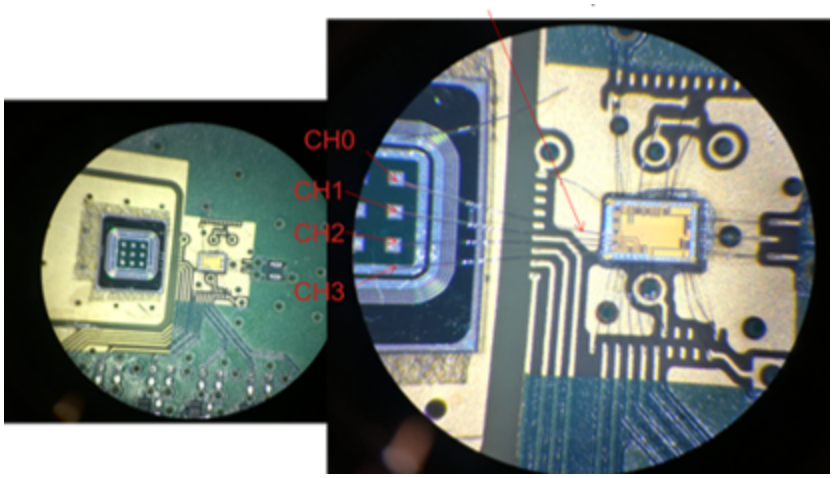

Figure 16: Micrographs of the prototype ASIC, assembled on its characterization board, with its four inputs bonded to pixels in a 3x3 AC-LGAD array.

goal of the EIC. During the FY23 funded period, the evaluation of the first prototype was concluded, an improvement path was identified, and a second prototype chip was submitted for fabrication.

The ASROC development, on the other hand, explores the applicability of SiGe technology to EIC applications. Promising because of ,its intrinsic speed, low noise and potential for low power draw, the funded period saw a completion of the first prototype, and its characterization board; characterization of the chip lies in the near future should funding be available.

Finally, the FAST ASIC, while not as directly optimized for EIC applications, is in a more mature development phase, supported entirely by resources from institutions outside the EIC community. It also has good expected performance for high-capacitance sensor readout, needed for the strip options under consideration by the EIC. During the FY23 funded period, SCIPP developed a readout board for the FAST-2 system and characterized its front-end performance.

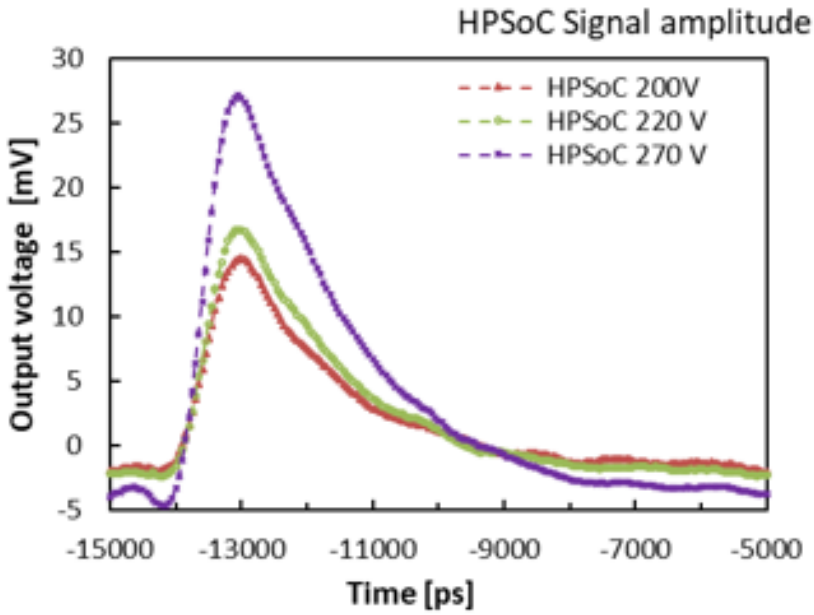

Figure 17: Average waveform delivered by the HPSoC prototype TIA amplifier, for a 60 μm bulk AC-LGAD sensor, as a function of bias voltage (sensor gain).

2.4 eRD109 FY23 Report - ORNL

This provides an overview of the design and production of flexible Kapton circuit boards for evaluating their potential use in providing low voltage, high voltage, high precision clock lines, and high-speed differential data links between the readout board at the end of each TOF stave and the readout chip assemblies. The approved budget of $44k was received in April 2023, with funds allocated until the end of November 2023 to complete the necessary tasks and achieve the project goals.

A technological survey was conducted to identify potential vendors and their capabilities. The survey revealed the availability of various off-the-shelf vendors offering low-cost options with fast turnaround times. However, many of these vendors do not offer customization possibilities. On the other hand, some vendors provided fully custom layups, but at a higher price and longer lead times. Considering the initial goals of the project, it was decided to proceed with inexpensive prototypes from off-the-shelf vendors to ensure a swift start.

Several flex PCB foils were obtained with various conductor geometries, including a 30x5cm^2 foil with three differential signal pairs at 1.3 and 2.5m lengths designed in collaboration with G. Visser from Indiana University. These prototypes were tested for their high voltage capabilities and exhibited no issues at voltages up to 1000V. Additionally, the ohmic resistance of the prototypes fell well within the expected tolerances. However, the measured line impedance was lower than the calculated value, measuring around 30Ω instead of the expected 50Ω. This discrepancy will serve as a reference point for future iterations of the transmission line design. Initial attempts to characterize the prototypes using a vector network analyzer were inconclusive due to the observed impedance mismatch.

Another flex PCB foil based on microstrip transmission lines, provided by Prof. Bean from Kansas University, is currently under testing. In the near future, several more prototypes will be designed, submitted, and characterized with the support of electrical engineering resources at ORNL. A suitable vendor has been identified which is capable of providing flex PCBs up to 2m length for future full-sized prototypes.

The next phase of the project will focus on the comprehensive characterization of the flexible Kapton circuit boards. This will involve testing all future versions for high voltage (HV) and low voltage (LV) compliance. Additionally, the differential data transmission will be evaluated using the CML driver of the ITS3 DPTS prototype available at ORNL. Standalone vector network analyzer (VNA) measurements and FPGA transceiver link speed and bit error rate tests will also be conducted. Furthermore, integration of the flexible circuit boards into the ePIC DAQ precision timing test bench, soon to be available at ORNL, will be pursued to assess the expected clock jitter at various lengths of transmission lines to ultimately inform the requirements on the design of the clock input stage of the readout ASIC.

The design and production of flexible Kapton circuit boards for the purpose of establishing communication between the readout board and the readout chip assemblies are progressing steadily. The initial prototypes have demonstrated satisfactory high voltage capabilities and ohmic resistance. While there have been minor discrepancies in the measured line impedance, they will guide future iterations. The project will now focus on comprehensive characterization and integration into existing test benches to evaluate performance under various conditions.

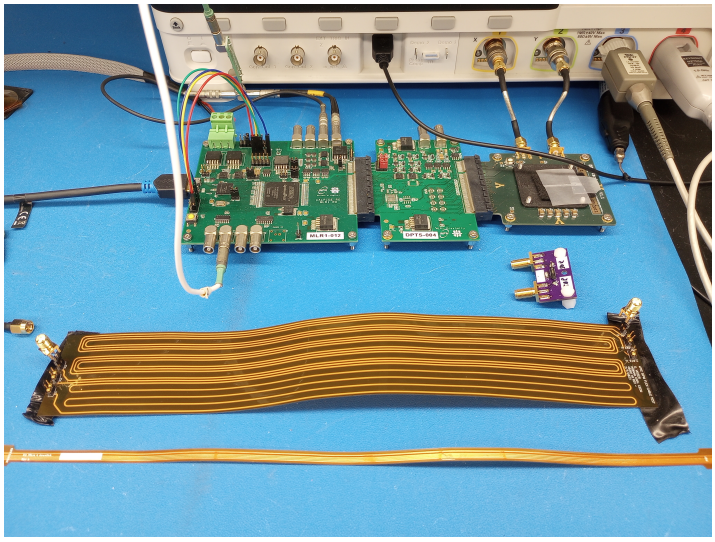

Figure 18: A selection of available flex-PCB prototypes and test setup in the ORNL RNP lab. Front to back: ATLAS ITK flex prototype (courtesy of Prof. Bean, Kansas University), ePIC LFHCAL SiPM flex prototype (courtesy of G. Visser, Indiana University and Brookhaven National Laboratory , ITS3 DPTS test setup and readout board connected to lab oscilloscope.

3 eRD109 FY24 Proposal

3.1 eRD109FY24 Proposal - EICROC

Following 2023 activities, the last quarters of 2023 will be devoted to the investigation of the source of the noise at the level of the TDC and the ADC. Once this is done, a new EICROC0 iterated design (EICROC0_v1) fixing this/these issue(s) will be submitted for fabrication as well as the associated test boards. The submission of EICROC0_v1 is foreseen for the first quarter of FY24. Updated printed circuit boards and EICROC0_v1 chips will be provided to EIC teams willing to collaborate and contribute to EICROC0_v1 characterization measurements.

In parallel, the system [EICROC0 + (4×4) pixelated AC-LGAD sensor] will be thoroughly characterized: electronics response "channel by channel" and exposition to a Beta source at IJCLab (Orsay, France) taking advantage of the Probe Pre-amplifier outputs. Some additional EICROC0 PCBs will be provided to EIC teams in Fall 2023.

Once EICROC0_v1 chips are available, we will set-up an updated dedicated test bench (wire-bonding EICROC0_v1 chips on test boards) and we will characterize EICROC0_v1 in order to assess its intrinsic performances "channel by channel". This will be studied using a calibration charge injection and an internal capacitance mimicking the sensor one. The main steps are the determination of the lowest threshold of the discriminator, the noise measurement and the efficiency as a function of the injevted charge. The TDC quantization steps will be measured by shifting the input calibration signal with a precise delay and the jitter extracted as a function of the charge. By injecting different charge, the ADC quantification step and the ADC non- linearity will be extracted. The signal-over-noise at the output of the ADC is also a key measurement. In a second step, assembled devices including an AC-LGAD sensor (through wire bonding) will be tested to check any further integration issues. The ultimate goal consists in characterizing the module with realistic energy deposits. The module will be tested with particles, first with a radioactive source such as beta (90 Sr) in laboratory and it will be exposed to an IR laser light. Charge sharing and timing resolution can be studied at this step. Eventually the module will be tested with hadron beam particles in a setup equipped with a precise beam telescope to fully assess the position and time resolution performance. Depending on the availability of the infrastructure, the beam test facility at FNAL (Chicago) with 120 GeV protons or at CERN-SPS with charged pions will be used. As teams from IJCLab and BNL are regular users of these beam lines for other projects, there will be no cost for testbeam.

Meanwhile the design of a low power consumption ADC, targetting less than 1 mW per channel, will be finalized. The power budget should in particular include the driving stage (shaper, buffer), which usually consumes several times more than the ADC itself. This low power ADC will be incorporated in the design of the next main step ASIC iteration, referred as EICROC1, which will also implement EIC clock frequency and EIC detector specific requirements. Relying on the feedback from characterization measurements with EICROC0_v1, the front-end electronics (Pre-amplifier and discriminator), as well as the TDC, will be further optimized. EICROC1 which is the main object of the FY24 budget request consists in the design, production and test of a small size prototype 16 (or 8) $\times$ 4 channels, to study floorplanning. The submission of EICROC1 design is scheduled for 3rd quarter of 2024. An EICROC1 dedicated printed circuit will be designed and fabricated. The characterization of EICROC1 will start as soon as the dedicated test bench is set-up.

Progress reports will be made at periodic meetings within the team and within the EIC R&D consortia. The EICROC0_v1 performances will be the object of presentations and publications.

The FY24 EICROC project timeline is displayed in Fig. 19.

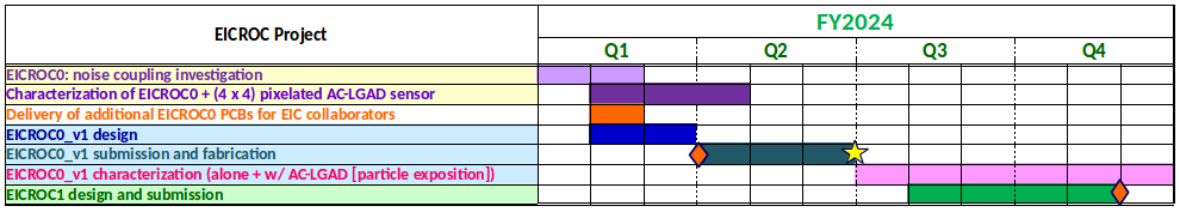

Figure 19: FY24 EICROC project timeline.

The FY24 budget request is presented in Table 2 which also lists FY24 human resource involvement from French institutions (IJCLab, OMEGA and CEA/Irfu).

The technical issues (noise coupling at the level of the TDC and the ADC) discovered during the testing of the first ASIC prototype (EICROC0) require the submission of an intermediate iteration (EICROC0ǐ) including associated PCB for which the FY23 budget is used.

The FY24 EICROC budget request amounts for 85 k$ and relates mainly to the submission of EICROC1 within a Multi-Project Wafer (MPW) and to the purchase of associated components such as the fabrication of printed circuit boards (PCBs) and cabling. The number of PCBs and associated components will accommodate for the number of EIC teams willing to contribute to EICROC1 characterization.

Institution	Resource	FTE (%)	Budget (k$)
IJCLab	Senior associate scientist	70	0 (in-kind)
	Senior scientist	35	0 (in-kind)
	Senior scientist	20	0 (in-kind)
	Research engineer	25	0 (in-kind)
	Post-Doc	100	0 (in-kind)
	EICROC1 [8 (or 16) $\times$ 4 channels] submission (MPW)	-	60
	Fabrication of testboards and associated components	-	25
OMEGA	Senior research engineer	25	0 (in-kind)
	Senior research engineer	20	0 (in-kind)
	Research engineer	15	0 (in-kind)
	Research engineer	50	0 (in-kind)
	Assistant engineer	20	0 (in-kind)
CEA/Irfu	Senior research engineer	30	0 (in-kind)
Total	-	-	**85**

Table 2: eRD109 budget request for FY24 for EICROC project. All entries in thousands of dollars.

The labor of French institutions collaborators will be in-kind. A grant was obtained to hire at IJCLab for 1 year (fall '23 - fall '24) a post-doc who will be fully involved in the EICROC project, in particular in the characterization of the system [EICROC0 wire-bonded + AC-LGAD] and EICROC0_v1.

3.2 eRD109 FY24 Proposal - FNAL

The Fermilab team has continued the development of the FCFD ASIC prototype, and in FY23 has designed the first multi-channel prototype with this approach, labelled as FCFDv1. This specialized 6-channel ASIC is designed to read out signals from LGADs, and provide precision timing and amplitude readout. The main developments since FCFDv0 prototype are the introduction of amplitude readout, extended dynamic range, and scaling up to multi-channels. Numerous other technical improvements were implemented based on the experience with FCFDv0, aimed at addressing the stability and performance of the system. The FCFDv1 ASIC is scheduled for submission in the end of Summer 2023, and once received it will allow one to build a large-area demonstrator of the technology that would be able to perform simultaneous measurements of position and timing of the passage of charged particles.

After the successful demonstration of the system readout with a FCFDv1 system during FY24, the next step, FCFDv2 would aim to build a full chip, including the digital readout, during the second half of FY24 and first half of FY25 (FCFDv2). The final, mixed-signal ASIC will be produced and tested during FY25 (FCFDv3), and its performance will be characterized using a single-layer AC-LGAD demonstrator system.

In FY24 we will focus on detailed characterization of the FCFDv1 performance, similar to studies presented in Section. 2.2. The FCFDv1 ASIC is expected to be delivered near end of 2023, and we will promptly proceed to testing it on the test bench in the lab, followed by testing with laser and test beams. A specialized readout board will be designed to accommodate the new ASIC connected to the EIC-module size AC-LGAD sensors, which will be designed after the FCFDv1 ASIC is finalized and submitted for production. Following the initial testing of the FCFDv1, the ASIC design engineers will pass on the subsequent testing to the members of the Fermilab and UIC teams to perform detailed studies in the beam test and laboratory environment, and the ASIC designers will proceed to design the next version, FCFDv2. This version will integrate the TDC and digigal components into the ASIC. These components will use previosly developed components from other timing detector projects developed at Fermilb, such as the ETROC family of chips.

The goal of FCFDv2 will be to deliver a full functionality ASIC with low power ADC and TDC adapted to the EIC 100 MHz clock, and expected particle occupancies. The ASIC will be optimized for EIC-LGADs, defined by the EIC detector groups and currently assumed to be AC-LGADs with 500 μm pitch and 1.0 cm length of strips. The ADC will be used to digitize the signal amplitude measurement, which is required for position reconstruction that uses the charge sharing property of the AC-LGAD sensors. Low power ADC and TDC have been implemented in the ETROC chip developed by the Fermilab group, and will be reused in this chip.

The ASIC design will be carried out by FNAL ASIC design engineers (Tom Zimmerman and others), who have decades of experience in designing ASICs for particle physics experiments, such as the QIE used in CMS experiment at the LHC, ETROC for CMS timing detector, and FLORA for X-ray experiments at LCLS-II. The UIC and FNAL postdocs and students will develop the ASIC specifications based on detailed studies of test-beam data from AC-LGAD sensors, develop the DAQ, and perform the characterization of FCFDv1 in test-beams. The group will work with FNAL scientists S. Xie and C. Peña on the design and characterization of the FCFDv1 chip. The team also includes postdocs and graduate students from collaborating institutes (Caltech, BNL, UCSC, University of Santa Maria Chile).

- **Deliverable #1 in Q1FY24**: Development of specifications for the FCFDv2.
- **Deliverable #2 in Q2-Q3 FY24**: Detailed characterization of the FCFDv1 performance
- **Deliverable #3 in Q2-Q4 FY24**: Design of the mixed-signal multi-channel FCFDv2 ASIC
- **Deliverable #4 in Q4 FY24**: Submission of the multi-channel FCFDv2

The FY24 budget request of the FNAL team is to support the production cost of the ASIC submission, and production cost of the readout boards ($40k).

Resource	Task	FTE	Budget (k$)
Staff Scientists	oversight and coordination	5	0 (in-kind)
Postdoc	Sensor testing	15	0 (in-kind)
Engineers	FCFDv2 design	25	0 (in-kind)
Postdoc	FCFD+Sensor testing	25	0 (in-kind)
FCFDv2 Multi-Project Wafer (MPW)	-	-	30
FCFDv2 test boards and components	-	-	10
Total	-	-	**40**

Table 3: eRD109 FNAL Budget request for FY24 on FCFD. All entries in thousands of dollars.

3.3 eRD109 FY24 Proposal - UCSC

No ASIC currently under development has yet demonstrated the capability of meeting EIC design goals of 20-25 ps resolution for sensors with capacitance as large as several pF, with minimal per-channel power consumption. Continued R&D is required to achieve this goals.

In collaboration with two small electronics firms, SCIPP continues to be a driving force in the development of two complementary approaches to LGAD readout. These include the CMOS-based HPSoC precision-timing "system on chip" development (Nalu Scientific) and the SiGe-based low-power ASROC front-end development (Anadyne, Inc.), both described above. We plan to continue our collaborative work with these two companies. For the case of HPSoC, characterization data accumulated for the initial four-channel prototype has allowed Nalu to refine the front-end to a design expected to meet the goals of the EIC Detector effort. Support from eRD109, coupled with that expected from other sources, should allow the HPSoC/SCIPP collaboration characterize this second, more optimized prototype, which includes an on-board 10 Gs/s back-end digitizer for waveform analysis and storage. For ASROC initiative, the FY24 effort will allow the first prototype, currently in fabrication, to be fully characterized and evaluated as a prospective front-end solution for an EIC LGAD readout ASIC. Finally, we propose to continue our characterization of the FAST family of chips, for which a new version (FAST3) is expected soon.

3.3.1 HPSoC ASIC Development

The focus of the FY24 HPSoC effort will be the characterization of the second, EIC-optimized prototype ASIC, including front-end performance, performance of the 10 GS/s digitizer, and an analysis of the overall performance benefits that come from replacing a simple discrimination with a full waveform analysis.

Characteristic	50 μm bulk	20 μm bulk
Assumed input charge (fC)	10	4
R_{in} (Ω)	63	30
Bandwidth (MHz)	129	129
Rise time (ps)	690	370
Noise to 5 GHz (mV)	0.14	0.14
V_{peak} (mV)	169	74
Jitter at 1 mV total noise (ps)	5.1	6.2

Table 4: Expected analog performance characteristics of the second HPSoC prototype. Layout parasitics have not been considered.

Table 4 lists expected performance parameters for the four-channel second-round HPSoC prototype, currently in fabrication in the 65 nm CMOS process offered by TSMC, critical to achievement of EIC specifications. Results are presented without the inclusion of layout-related parasitics, and actual performance will likely be somewhat worse. However, the moderate bandwidth, representing an optimum between the competing principles of increase slew rate vs. decreased noise, will likely limit the contribution from parasitic effects. In addition, timing resolution ("jitter") contributions from electronic noise are calculated under an assumption of 1 mV of noise, significantly above that suggested by the simulations. Simulation also suggest that this performance will be achieved at a power

draw of approximately 3 mA per channel, including triggering, amplification, and comparator/timing functionality.

The optimization of amplifier parameters was performed with two limiting cases of sensor geometry in mind: the standard 50 μm bulk, and the 20 μm bulk that simulations suggest will be needed to limit intrinsic charge-deposition fluctuation ("Landau") contributions to the timing resolution to the level needed to achieve 20 ps resolution, which has yet to be demonstrated for any EIC prototype system. We believe it is essential to retain this possibility in EIC electronics development, and the HPSoC has been explicitly engineered to do so, achieving an estimated timing jitter in the 5 ps range for both 50 and 20 μm bulk thickness. In addition, the new TIA amplifier has been designed to be significantly more tolerant of external loading, making it a candidate both for the pixel and strip LGAD systems envisioned for the endcap and barrel regions, respectively, of the EIC detector.

When evaluating the electronic contribution to the timing resolution of LGAD-based detection systems, it is conventional to only consider the jitter contribution that arises from the fluctuation of the electronic noise around an optimized discrimination scheme. However, as the performance of fast timing systems is pushed farther, additional electronic contributions to the timing resolution arise, including those from digitization noise, pulse amplitude fluctuations, threshold-value fluctuation, timing reference jitter, and TDC time-scale fluctuations. When all these are taken into account, the overall electronic contribution to the timing resolution can be significantly worse than that of the isolated jitter contribution.

These contributions have been estimated in the context of the HPSoC system, for which all of these elements appear within the architecture of the ASIC, which, unlike other ASIC development efforts, includes an on-board 10 GS/s waveform digitizer. Figure 20 shows a histogram of time-of-arrival estimates available to a system employing a standard discrimination-based timing scheme, including all the potential sources of time-resolution degradation attributable to the readout. A resolution of approximately 14 ps is observed, far worse than the expected jitter contribution of 5 ps, and not compatible with a goal of 20 ps overall timing resolution once sensor contributions are added in. Also shown in Figure 20, however, are results obtained when a simple waveform analysis is performed, showing that an electronic contribution in the 5 ps range is recovered. Thus, the ability to measure and capture LGAD waveforms could be essential to achieving EIC goals for TOF timing resolution. Waveform digitization could also prove important in making use of information in neighboring channels to improve both timing and spatial resolution.

3.3.2 ASROC ASIC Development

The ASROC is unique among ASICs under development for the EIC in its use of a SiGe BiCMOS technology to produce a fast, low-noise analog amplifier with superior power-consumption properties. Figure 21 shows the expected jitter contribution as a function of input charge for two separate values of per-channel power consumption: 1.1 mW and 0.72 mW. A jitter contribution of less than 10 ps is observed for input charge of 4 fC or greater for a power draw as small as 0.71 mW, making this a potentially promising front-end solution for the EIC.

A first prototype, through a collaboration between SCIPP and Anadyne, Inc. funded by a Phase-I SBIR, will be available for characterization by the beginning of the FY24 funded period. A characterization board (Figure 22), designed at SCIPP and currently being loaded and qualified, will enable the characterization.

3.3.3 FAST ASIC Testing

During FY23 funded activity, a characterization board (Figure 23) was developed for the characterization of the front end amplifier system of the FAST2 ASIC. While the time resolution performance of the ASIC was not found to be as good as that expected for other EIC-oriented ASICs, its behavior is expected to be relatively unaffected by high capacitive loads. We would like to keep this option open for now for large-capacitance applications, for which strips of dimension 500 μm x 1cm are proposed.

A new version (FAST3), featuring a pulse-width regulator to improve timing jitter and a dedicated analog output buffer, is expected to become available during the FY24 funded period. With only minor modifications, the existing characterization board can be used to study the analog performance of the FAST3 ASIC, and its prospects for application at the EIC. We see this work as requiring relatively

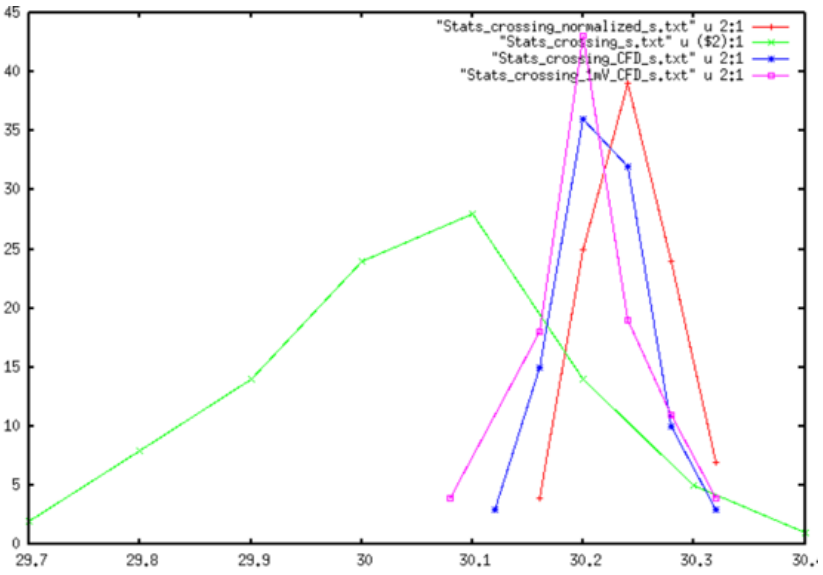

Figure 20: Comparison of readout-associated timing resolution between constant-level discrimination and more sophisticated forms of time-of-arrival determination permitted by waveform analysis. The green histogram represents the spread of time-of-arrival results under the assumption of constant-level discrimination, when all sources of electronics-induced uncertainty are included, yielding a timing resolution of 14 ps. The red and blue histograms show the improvement when the waveform is made use of to correct for varying pulse height, or perform full constant-fraction discrimination, respectively. For the pink histogram, a realistic digitization step of 1 mV is also included. The use of even this simple sort of waveform analysis can restore the electronic contribution to the timing resolution to the desired 5 ps range.

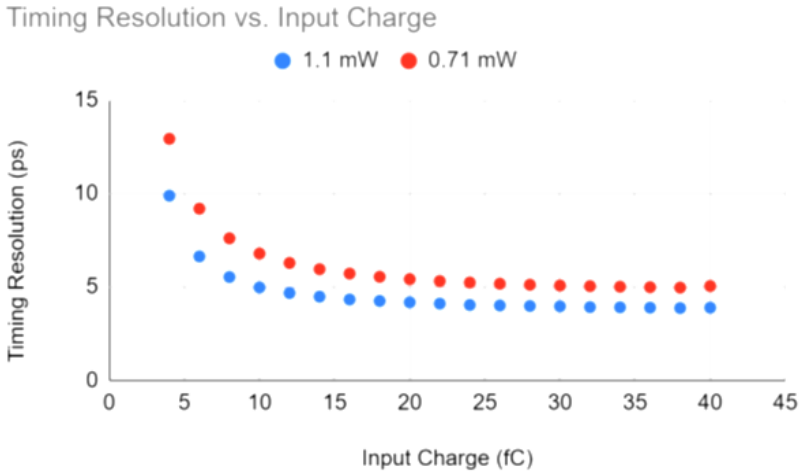

Figure 21: Expected timing performance of the SiGe ASROC front-end amplifier, for two values of per-channel power consumption (1.1 mW and 0.71 mW)

little effort, and only minimal support from EIC funds, but include it as an option to be kept in play for now, and also as a good point of comparison for ASICs directly geared towards the EIC.

3.3.4 Summary and Milestones

As a collaboration, the EIC detector groups are pursuing timing resolution for minimum-ionizing particles that is significantly better than has been achieved for large HL-LHC applications. We have yet to demonstrate a detection system, or a clear path towards one, that can meet stated EIC goals.

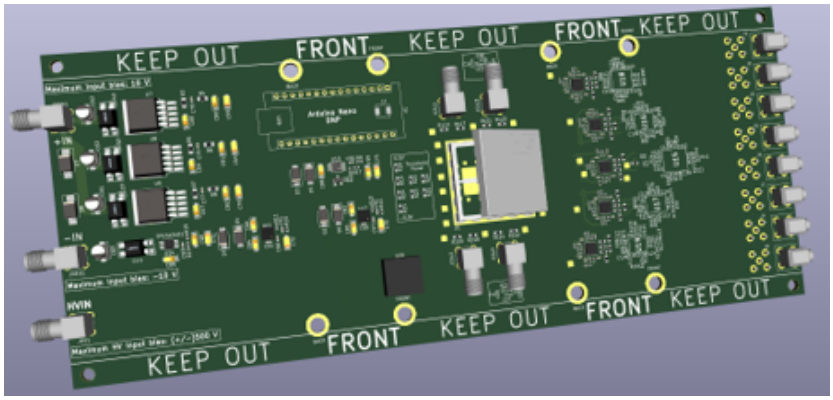

Figure 22: PC board developed at SCIPP for the characterization of the ASROC prototype.

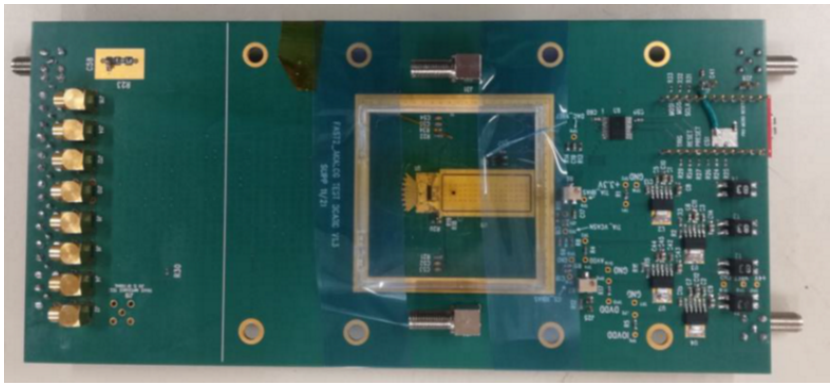

Figure 23: PC board developed at SCIPP for the characterization of the FAST ASIC chip.

Thus, integrated R&D must continue on both sensor technologies and readout schemes. Here, we proposed a program that can leverage a body of ongoing effort to keep several important options for an EIC ASIC or ASIC sub-component that could prove essential to meeting EIC goals. If funded, we foresee the achievement of the following milestones by the end of the FY24 period:

- Characterization of the ASROC first prototype with calibration and sensor inputs, in time to begin discussion for mode of adoption into EIC TOF systems if performance found attractive (January 2024)
- Characterization of the FAST3 analog amplifier with calibration and sensor inputs (March 2024)
- Characterization of 4-channel HPSoC v.2, with calibration inputs as well as inputs from complete pixel and strip assemblies (March 2024)
- Development of specifications for a third-round HPSoC prototype (May 2024)
- Comparative study of HPSoC performance between simple constant-level discrimination and basic waveform analysis (July 2024)

3.3.5 UCSC eRD109 Budget

The FY24 budget proposal for UCSC/SCIPP is tabulated in Table 5.

3.4 eRD109 FY24 Proposal - ORNL

The ongoing R&D into Kapton flex technologies and vendors for long distance differential link and power distribution will yield a flex PCB prototype and a characterizations of its performance in terms of RF insertion loss, achieved clock jitters and transmission bit rates. The continuation of this R&D

Inst.	Personnel	Months	Percent	Budget (k$)
SCIPP	Faculty	12	$1 \times 8\%$	0 (in-kind)
SCIPP	Senior Staff	12	$1 \times 8\%$	0 (in-kind)
SCIPP	Postdoctoral Fellow	12	$1 \times 10\%$	0 (in-kind)
SCIPP	Electrical Engineer	12	8%	14.0
SCIPP	Electro-Mechanical engineer	12	5%	12.0
SCIPP	Laboratory Specialist	12	10%	12.0
SCIPP	Material and Supplies			7.0
Total				**45.0**

Table 5: UCSC/SCIPP budget request for eRD109 readout electronics development in FY24. All entries in thousands of dollars.

program towards the required 90% design maturity for the CD2 review in 2024 will produce a functional full size demonstrator of the flex PCB that connects at least one readout ASIC and sensor assembly on one end to a RDO prototype to be developed by the BNL and Rice groups.

This demonstrator will require the bonding of a diced readout ASIC onto the flex PCB by wire bonds or bump bonds, depending on the interfaces of the readout ASIC revision available at that time. The connectivity between readout ASIC and sensor is yet to be determined, but can be performed via direct wire bonds, or via a bump-to-wire interposer structure designed into the flex PCB.

The design of this full size prototype will also require a survey and selection of a suitable connector type on the end that connects to the RDO and the primary power sources.

The technical realisation of this prototype will rely significantly on external vendors and/or ORNL technicians and engineering support for the production and ENIG coating of the flex PCB, various bonding services, assembly of sensor-ASIC modules as well as additional material costs to acquire these ASICs and readout ASICs.

The evaluation of the full prototype will consist of demonstrating its capability to read out the available readout ASIC prototype over the required distance of 1.3m, as well as more detailed characterization of the jitter characteristics incurred from the signal propagation on the clock transmission line using the ePIC DAQ precision timing test benches that are currently under construction and evaluation.

We propose to continue the funding of the ongoing project at the cost profile given in Table 6 starting from December 1st, 2023.

Inst.	Resource	FTE (%)	Budget (k$)
	Barrel Low-Mass Service Hybrid R&D		
ORNL	Electrical Engineering + Technician	10	10
ORNL	Staff Scientist	10	0 (in-kind)
ORNL	Materials and Supplies	-	10
ORNL	Production and Bonding	-	10
ORNL	Low cost interconnect	-	15
Total			**45**

Table 6: eRD109 Budget request for the continuation of the ORNL flexible Kapton PCB R&D in FY24, starting from December 1st 2023. All entries in thousands of dollars.

3.4.1 Low cost interconnect for sensor-ASIC hybridization

ASIC and sensor interconnection in hybrid pixel detectors is typically done by bump bonding techniques involving the lithographic deposition of solder material on the pixels of the ASIC and the precision flip-chipping of this ASIC on the sensor, previously itself coated with under bump metallization (UBM). This costly process is required to achieve the high yield and high-density interconnect required for pixel detectors with a pixel pitch of 50-200 μm.

The pixel/strip pitch required for EIC AC-LGAD is more relaxed than for hybrid pixel sensors in LHC experiments and interconnection could be achieved with a less costly technology. We propose to start the investigation of alternative bonding techniques for possible application in sensor-ASIC

interconnection at EIC. In FY24, the first phase of this study will focus on surveying the available technologies and services and available, procuring materials for trials, and making first contact with possible vendors. The second phase, at the beginning of FY25 will be the first trials with the sensor and ASIC at ORNL, using the SET FC150 High Precision Flip-Chip Bonder to be installed in our cleanroom in Summer 2024.

The study will target multiple types of technologies that could provide the desired interconnect at a reduced cost :

- Anisotropic Conductive Adhesive/Films bonding (ACA/ACF)
- Printing methods for solder deposition and balling
- Laser jetting solder sphere deposition
- solder ball transfer via stencil

ACA and ACF are films of adhesive containing conductive micro-particles that can be purchased from various vendors. Electro-less Nickel-Gold pad deposition can be carried on ASIC and sensors to create protruding mushroom-like pads on both dies that are used when proceeding to flip-chipping with the ACA/ACF deposited in between, to capture micro-particles in a sandwich between the pads. This phase of the project will aim at procuring the ACA/ACF that can be dispensed/applied in our flip-chip bonder and purchasing the materials to proceed to ENIG deposition on the sensor and ASIC samples.

Solder printing/Stencil deposition can be used to deposit solder on electrodes to create solder pads for flip-chip soldering. Modern printing techniques can achieve the desired pitch and could provide a cheap method to interconnect sensors and ASICs. In this phase of the project, we will get in communication with possible vendors providing these services or machinery capable of this method for a reasonable cost.

Laser jetting and solder ball transfer are wafer-level solder ball deposition methods used to lower the cost of packaging wafers with modest requirements in pitch, with regard to costly lithography and sputtering involved in standard bump-bonding. In both cases, the solder ball of pitch down to 200 μm can be mechanically placed, one by one or all at once, on a wafer with UBM and reflowed in situ. The resulting dies can be used to bond the ASIC to the sensors that should also have UBM deposited. In this phase of the project, we will establish contact with solder ball transfer vendors, request quotes for production-level processing and set up the process for trials with the techniques.

We request $15k for the procurement of materials for bonding trials, chemicals and products for ENIG deposition trials and dummy silicon for mechanical and chemical trials of ENIG deposition.

3.5 eRD109 FY24 Proposal - frontend electronics at BNL, Rice, UIC and ORNL

To accompany the AC-LGAD frontend readout ASICs described above, dedicated readout electronics need to be developed and designed to provide the necessary clocks and slow control signals to the readout ASICs as well as receive, aggregate and submit the readout data out of the spatially constrained detector volume. To this end, we propose to form a collaborative AC-LGAD readout electronics working group between BNL, Rice, UIC, and ORNL to address these challenging questions.

This work will include fundamental R&D on an integrated clock conditioning and distribution system that meets the low jitter requirements of a sub-30 ps MIP timing system and implementation studies on streaming data acquisition architectures with the EICROC family of readout ASICs, based on “commercial off the shelf” FPGAs and components. At the same time, specific implementations of such systems, including power distribution and slow control links, will be studied and developed for the barrel and endcap regions of the TOF system. While we envision both barrel and endcap readout system to be based on the same general architecture, the differences in readout channel density, sensor module geometry and spatial constraints warrant independent (yet closely collaborative) developments for each region. The resulting readout board concepts will be applicable as an immediate basis for developments towards the readout system of the far-forward AC-LGAD detector systems.

During FY 23, we are in the process of establishing a strong foundation for the project. The EICROC0 ASIC PCB has been procured, and we have bonded the AC-LGAD and EICROC0 onto the

PCB with the assistance of BNL's instrumentation division. Corrections to the PCB have been made as needed. We have also acquired a Xilinx development kit and have set up a test stand at BNL and UIC. The required software and firmware have been installed, and we are currently modifying the software to establish connections between the test stand and the EICROC0. Our aim is to create the first fully operational test stand that combines the sensor, ASIC, and candidate prototype board, allowing us to perform primary characterizations and replicate results achieved by the EICROCx developer. Stage 0 marks the starting point of the project, laying the groundwork for the subsequent stages and ensuring the successful development of the ePIC TOF readout electronics. We are also doing workforce development by involving two graduate students who are learning about the sensor, ASIC, and board technologies and their applications in the ePIC TOF project.

As one of main milestones planned for FY23, the Rice and UIC team will contribute to the development of a general layout of frontend readout electronics, with a focus on the forward and barrel TOF, respectively, to be used as baseline for the CD2 review. We propose to build a complete prototype frontend "service hybrid" to provide full functionalities of TOF readout, based on a compact design of a readout board and power board to minimize material budget and space constraint. A prototype readout PCB board that provides a series of frontend services will be developed: (1) connectors that are compatible with EICROCs via flex cables; (2) data aggregation, transmission, slow controls via electronic links and transceiver FPGA chips; (3) connectors to low and bias voltage power supply. A power board will provide low voltage power supplies to EICROCs and other on-detector chips for data transmission and slow control. We propose to build a power board based on CERN bPOL12V DC-DC converters with one layer planar spiral coil and a small connector that is pin compatible with the CERN bPOL12V_CLP module. The power board will also have a connector to low voltage power supply cables. With the anticipated delivery of first version of EICROC, our goal is to demonstrate a prototype full chain readout from the frontend to backend.

The ePIC TOF Readout Board (RDO) is a crucial component of the readout chain of the AC-LGAD based TOF. It serves as an interface PCB between the electrical ASICs and the fiber-based DAQ system. The RDO interfaces with the readout ASIC (e.g., EICROCx) and facilitates data paths for configuration, control, and data/status transmission. It provides low-jitter clocks (5 ps) for maintaining a 30 ps timing resolution. The RDO interfaces with the ePIC DAQ via high-speed fiber links for ASIC configuration data, clock recovery, and streaming mode data transmission. The design goal is to make it small, cost-effective, and low-power, with an FPGA, SFP+ (Small Form-factor Pluggable) fiber interface, PLLs, clock cleaners, and ASIC connectors. The design stages of the RDO involve prototyping with a Xilinx Development Kit, custom crafting using FPGA and other components, and TOF-specific customization with final connector choices. The board has different form factors for the ETOF and BTOF detectors. The BTOF Readout Board has 64 ASICs per board, while the ETOF Readout Board has 24 to 48 ASICs per board. The expected data rates are $<$0.6 Gbs/fiber for BTOF and $\sim$3 Gbs/fiber for ETOF. The ePIC TOF RDO project will maintain close integration with the ePIC DAQ Group for both prototyping and final versions. This includes collaboration on FPGA selection, fiber link protocols, clock recovery schemes, and use of FPGA development kits/boards. The design blocks of the FPGA are shared or developed within the ePIC DAQ framework, covering infrastructure, fiber interfacing, clock recovery, and I2C blocks. Only the ASIC-specific readout blocks are provided by TOF, ensuring cost savings and risk reduction through commonalities across subsystems in ePIC DAQ. The following stages mark crucial milestones in the development of the RDO and will bring us closer to achieving our objectives for the ePIC TOF project.

Stage 0 (FY 23): In FY23, we focused on workforce development, component assembly and groundwork preparation for stage 1 and 2 in FY24. We procured the sensor, the first iteration of the ASIC (EICROC0) mounted on a separate PCB (FEB) and a Xilinx development Kit. We assembled the parts, set up a test stand, and installed the software to reproduce some of the primary developer's results.

Stage 1 (First half of FY24): Our goal in this stage will be to demonstrate the TOF readout chain for the first time, going beyond the basic tests performed by the EICROC developers who only use ethernet that is expected to be reproduced in stage 0. To achieve this, we will start to prototype the RDO using a Xilinx Development Kit, such as the Xilinx ZCU106 with an ethernet interface for the backend DAQ. We will also interface and develop the ePIC DAQ protocols using fiber, which include

clock recovery, ASIC configuration, ASIC status, streaming readout, etc. This will allow us to test the full functionality of the TOF readout chain. We will also assemble EICROC0-V1, the updated EICROC0 with fixed issues and lower power consumption that will be available at the end of FY23. We will test the performance of the FEEs with specific focus on noise studies, time walk and jitter and compatibility with the TOF requirements. We will provide necessary feedback before subsequent submission of the ASIC. We will also prototype the flex cables connecting the FEB and the RDO.

Stage 2 (Second half of FY24): In this stage, we will focus on customization specific to the ePIC DAQ environment. We will collaborate with the ePIC DAQ team to develop a first complete RDO prototype that includes the FPGA and other components for providing all necessary functionalities in the final version. We will align with them on various aspects of prototyping and design, such as FPGA choice and configuration, fiber link type, speed and protocols, clock recovery scheme, design stages and FPGA development kits/boards. Our current choice for the FPGA is the Xilinx Artix Ultrascale+. We will also explore various timing chips ("clock cleaners and jitter removal"). We will continue to prototype Flex connector. On completion of Stage 2, we will achieve a full demonstration of the TOF readout chain, and prepare to move onto developing the prototype specifics for the barrel and forward end cap TOFs.

We seek a grant for electrical engineer efforts for 12 months (6 months each for stage 1 and stage 2) to develop readout electronics for the ePIC TOF detector. The engineer will collaborate with the EICROCx developer and conduct R&D activities for the ePIC TOF requirements. The engineer's support will also help give feedback for the next EICROCx submissions on the compatibility of EICROCx for the TOF requirement. This project will address the challenges of providing clocks, slow control signals, and data acquisition for the AC-LGAD frontend readout ASICs. Moreover, specific implementations of such systems, including power distribution and slow control links will be included in the first and second stages of the project. This is a collaborative venture on the AC-LGAD readout electronics working group between BNL, Rice, UIC and ORNL to design and improve the readout electronics using the EICROC family of readout ASICs. The workload will be distributed among the three institutions according to their expertise and resources. We are confident that we will find the engineer support we need for this project, with the required skills and experience to succeed and also allocate the FTE of the personnel between the groups. The deliverable of this project will be sub-30 ps MIP timing systems that will boost the performance of the ePIC TOF detector. The readout board concepts will be applicable for the far-forward AC-LGAD detector systems as well.

Activities at BNL: A 0.4 FTE electrical engineer will serve as the main interface with the EICROCx designer, demonstrate the initial readout chain and contribute to the development of the full RDO prototype (5 months).

Activities at Rice: A 0.3 FTE electrical engineer will contribute to the development of the full RDO prototype, with a particular focus on the end cap-specific designs (3.5 months) based on the CMS endcap timing layer experience.

Activities at UIC: A 0.3 FTE electrical engineer will contribute to the development of the full RDO prototype, with a focus on the barrel TOF-specific designs (3.5 months).

Activities at ORNL: Communicate with BNL, Rice and UIC and make and test a flex PCB prototype that connects a readout ASIC and sensor assembly to a RDO prototype from BNL/Rice/UIC, using external or ORNL services.

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Inst.	Resource	FTE (%)	Budget (k$)
	TOF readout electronics R&D		
BNL	Electrical Engineering	40	120
BNL	Development Kit	-	10
BNL	Travel	-	4
BNL	Other component	-	3
Rice	Electrical Engineering	30	45
Rice	Travel	-	2
Rice	Other component	-	2
UIC	Electrical Engineering	30	30
UIC	Travel	-	2
UIC	Other component	-	2
Total			**220**

Table 7: eRD109 budget request for R&D of readout electronics in FY24. All entries in thousands of dollars.

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