AstroPix Status Update

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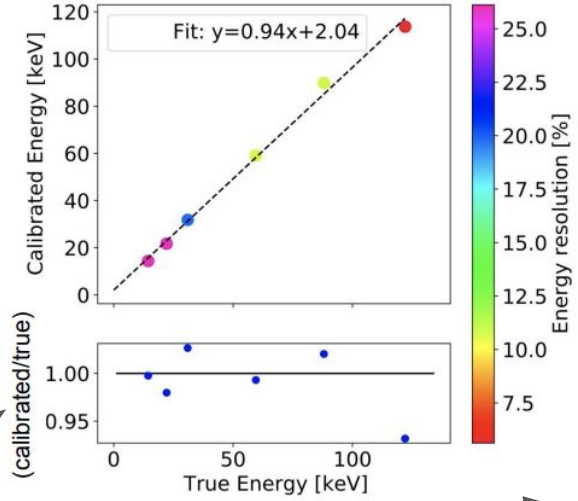
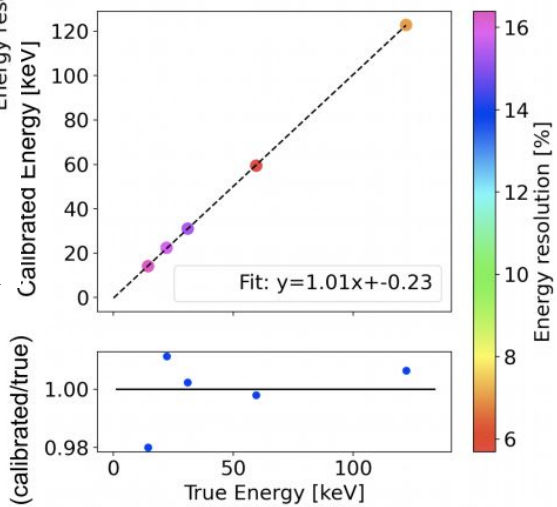
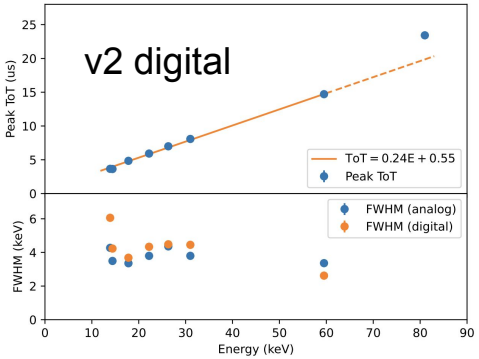
ePIC Imaging Barrel Calorimeter Meeting

Publication history

- ATLASPix
  - https://arxiv.org/abs/2101.02665
  - https://arxiv.org/abs/2109.13409
- AstroPix_v1 (analog data)
  - https://arxiv.org/abs/2209.02631
- AstroPix_v2 (analog data)
  - https://arxiv.org/abs/2302.00101
- AstroPix_v2 (digital data), initial AstroPix_v3
  - https://pos.sissa.it/444/644/pdf
- A-STEP, utilizing AstroPix_v3
  - https://pos.sissa.it/444/579/pdf

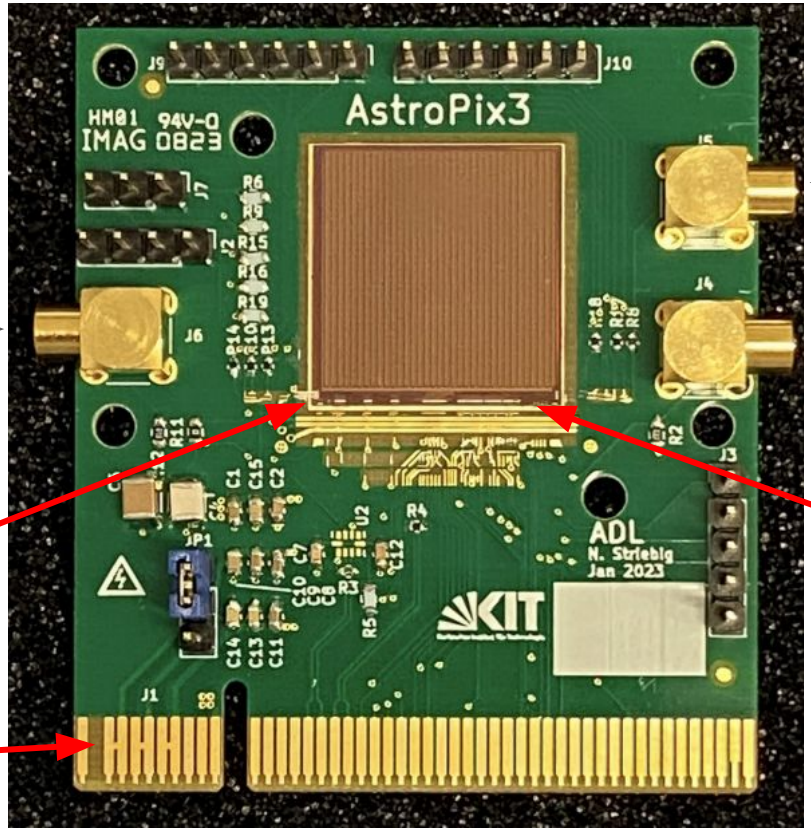






Incremental changes stepping from ATLASPix to benchmarked AstroPix

Chip PCB



200 MHz sample clock

High-voltage bias
(-160V)

Output analog signal

Digital periphery,
“digital top”

Wire bonds for power
and IO

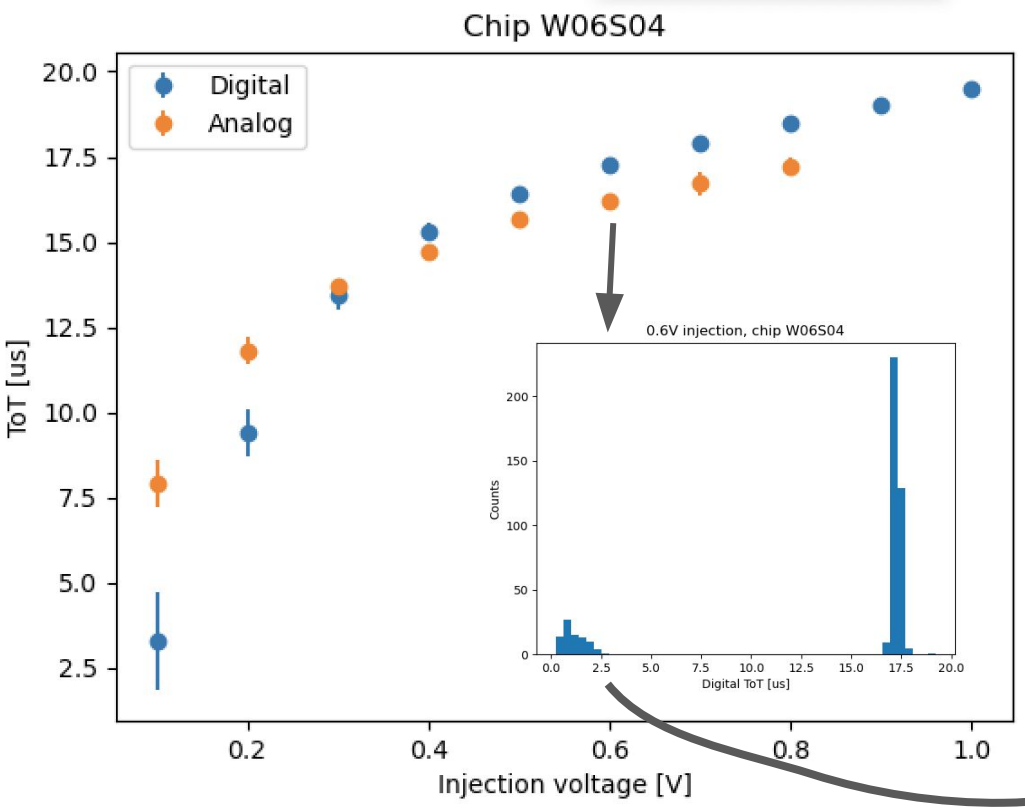
Connection to testing
readout board

Updates since last meeting (16 June)

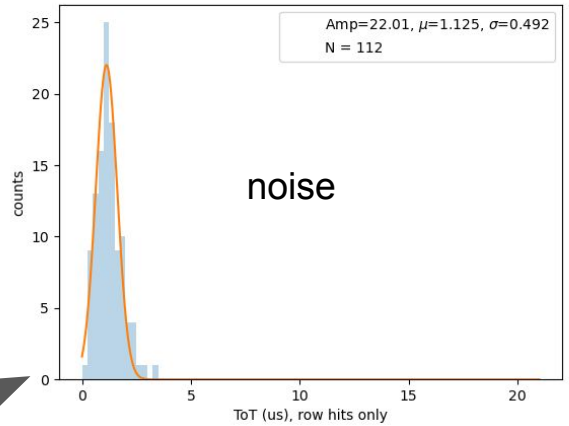
Emphasis on testing chips on 300 Ohm*cm substrate

- Originally fabricated on 3 substrates:
  - 1 kOhm*cm = flight chip
  - 300 Ohm*cm = backup chip
  - 50 Ohm*cm = test chip
- Poorly understood nature of 1 kOhm*cm pixels
  - Chips drew very high leakage current off bias line (breakdown with any supplied voltage)
  - High leakage -> possible surface currents / edge effects -> very poor data quality

Preliminary testing - injection scan into single pixel (r0c10)

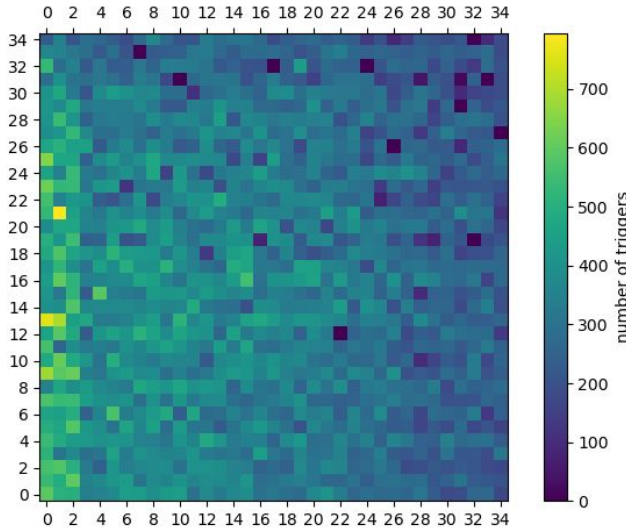


- Analog and digital data (from row0 / bottom row only)
- Nearly optimized configuration / pulse shaping settings (still WIP)
- Expected behavior
- Not very good agreement between digital and analog - different shapes
  - WIP to understand



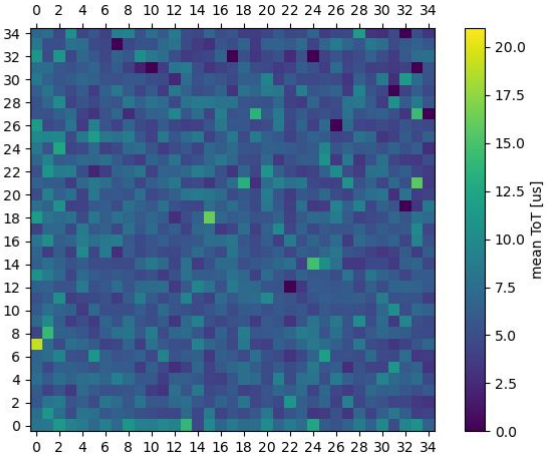
Ba133 pixel scan - 30s/pixel, 200mV threshold

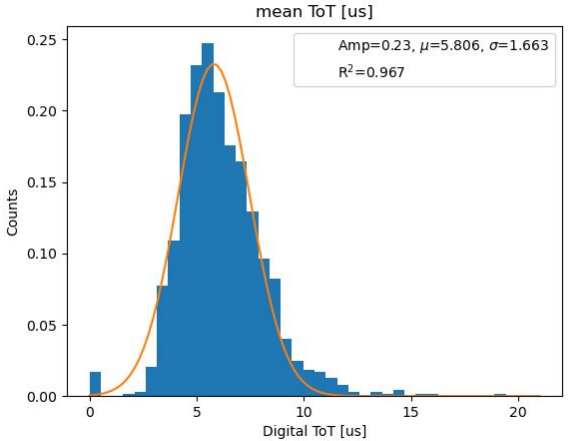
Number of triggers



Off-center source seen in hot spot!

Mean ToT of distribution from each pixel



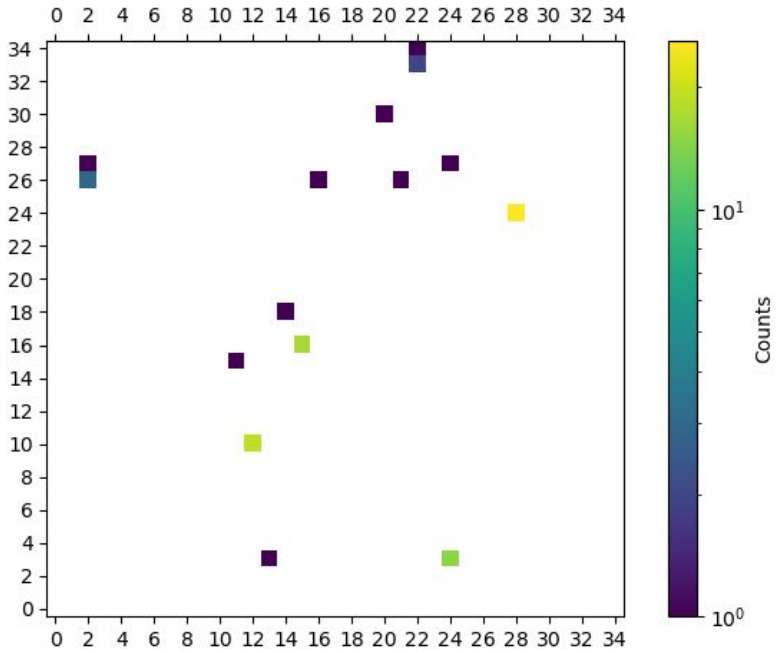


- Variability V = σ/μ *100% = 28.6%
  - Still have a bit of config optimization
- Compare to v2 (Backup slide), V = 21.5%
- We have known since v2 that individual pixel calibration will be required
  - WILL NOT BE NECESSARY FOR v4+ with pixel tuneDACs

Current testing = full-array running

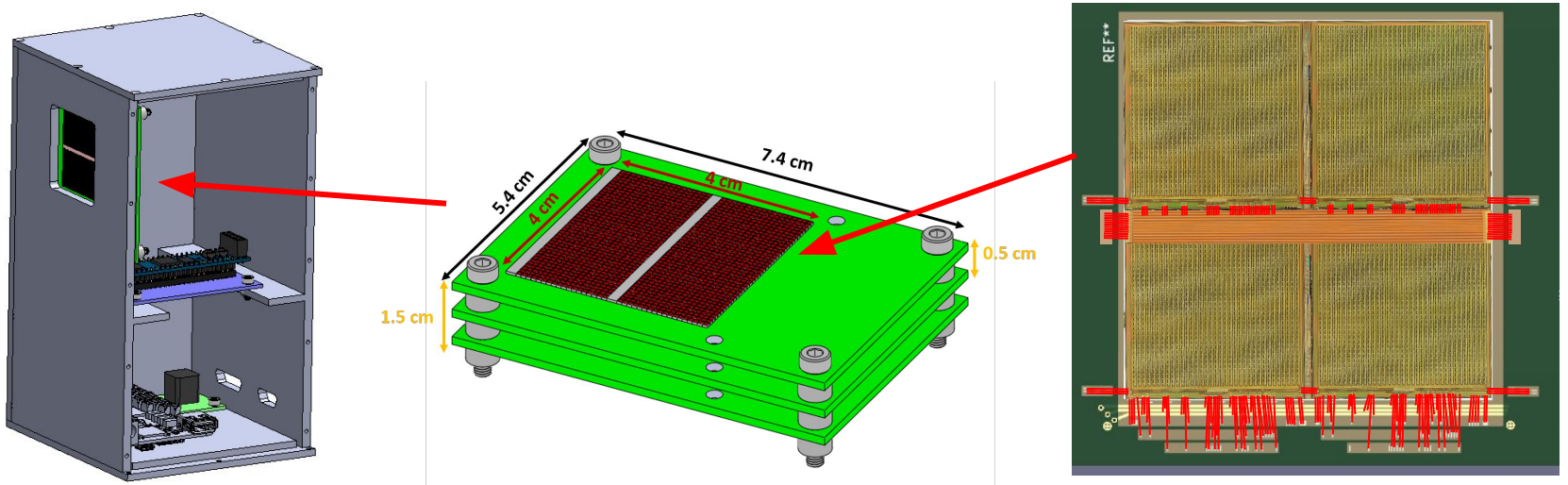
- Noisy pixels masked (<1% of array)
- 200 mV comparator threshold (relatively high, just for testing. ~40-50 keV)
- Next (obvious) steps = test full array with radioactive sources

1 min noise run, ~0.5 Hz



A-STEP and v3 quad-chip

- A-STEP mission objective = Raise technical readiness level (TRL) of AstroPix quad-chip for future use in AMEGO-X
  - Validate operation of v3 quad-chip in space environment on sounding rocket
- AstroPix_v3 is a flight chip to be used on A-STEP
  - Use tools developed while playing around with v3 to create a structured v3 test program

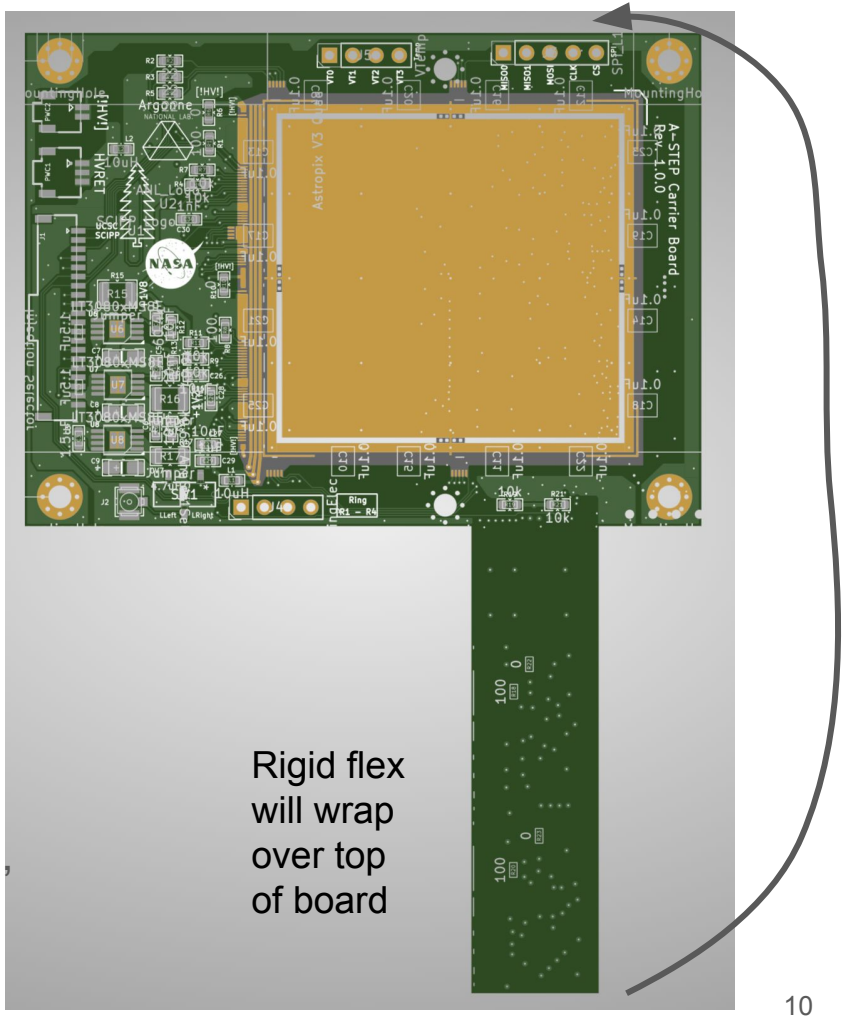


v3 quad-chip testing

- Custom-designed chip carrier board (and rigid flex bar to allow for wire bonds to the top two chips) submitted for fabrication this week
- First bench testing of quad-chip in late September

v4 status

- Submitted to foundry in June 2023
- Expect delivery ~end of 2023
- tuneDACs (for individual pixel threshold setting), asynchronous ToT strategy, no row/col ORing and overall smaller data packets



Firmware Development

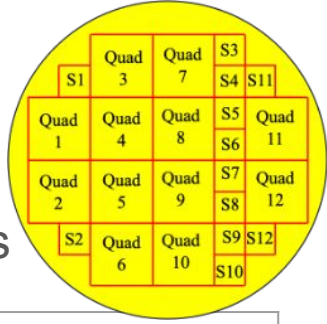
Led by Richard Leys at KIT

- FW-driven SPI readout
  - Previously, SW-driven readout strategy introduced additional deadtime
  - Now chip itself triggers readout when there is data in buffers
- Scale-ability
  - Read through the daisy-chain in FW rather than SW
  - Each daisy-chained SPI input has own interface which feed into global buffer (one chip reads out a time)
    - Supports up to 20 SPI inputs
- Different comms protocols
  - Interface with computer via USB or UART
- Simulated test structures
  - Simulate hit data at “SPI interface to global buffer” level, can also be integrated with SW dev for testing
- Housekeeping
  - Include packets of housekeeping data in data stream, as defined by user (voltages on FPGA, FPGA temp, etc)

Backup

v3

V3 substrates

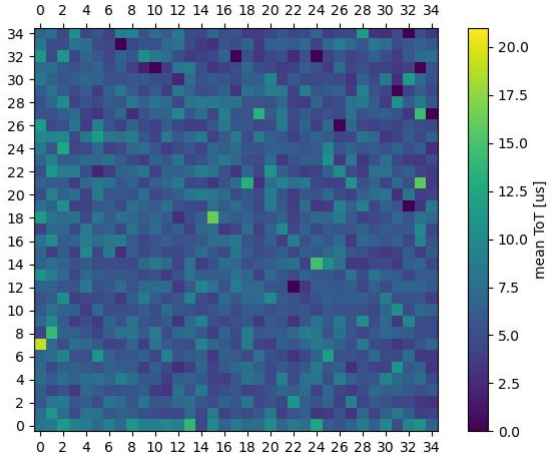


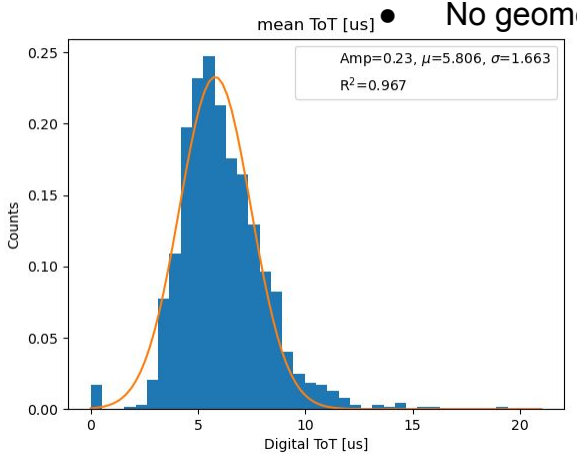
Fabricated chips (single chips and quad-chips) using 3 different substrates

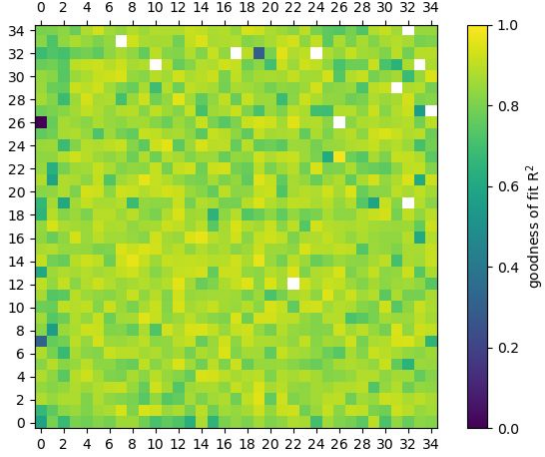
	TSI Substrate	Okmetic Substrate	Topsil Substrate
Purpose	Testing	Backup	Flight
Resistivity [Ω*cm]	50	300-400	10,000
Number of wafers	2	2	3
Diced and mounted on test board?	Yes	No (in progress)	Yes
Breakdown voltage [-V]	250	290	High leakage current (uA) with any applied voltage
Leakage current, -150V [-nA]	40	40	High (80mA at -30V)
Testing notes	Low-quality substrate, high pixel variability	Tested on wafer, sent for dicing	Challenging - will explore in a bit

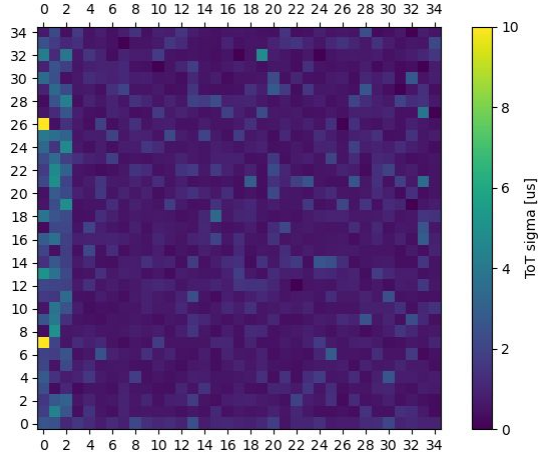
Ba133 pixel scan - 30s/pixel

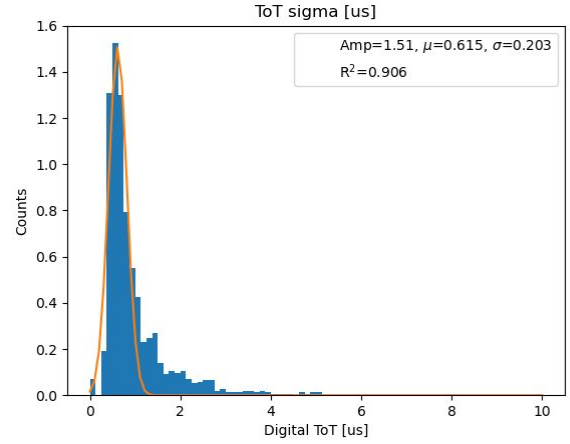
- Lower variation than TSI chips
- Poorer DQ in PMOS columns
- Generally good fits
- No geometric dependence

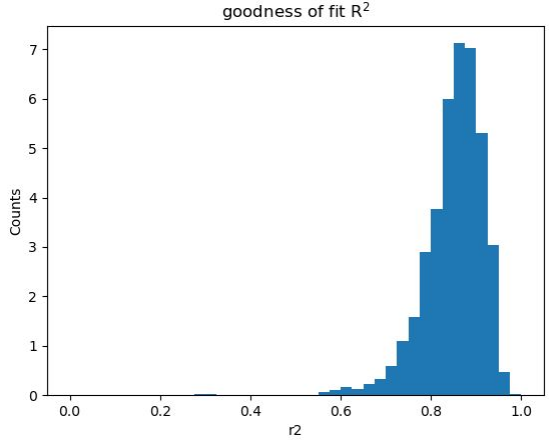






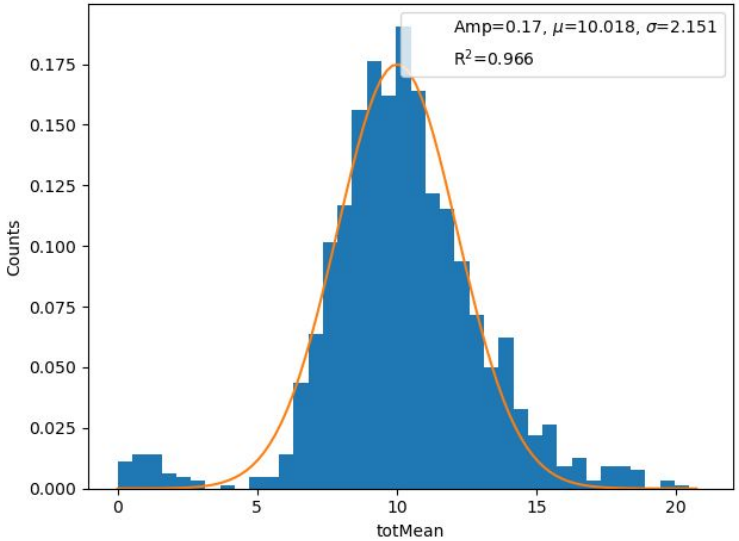




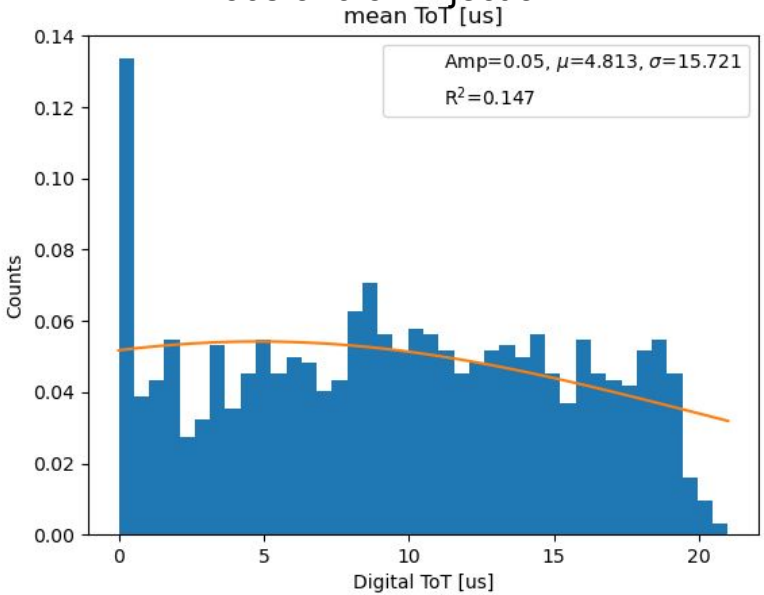


Compare pixel scan to older chips

V2 standard wafer (300 Ohm*cm)
30s of 0.3V injection



V3 TSI wafer (50 Ohm*cm)
30s of 0.3V injection



No clear mean ToT peak -> ultra high pixel variation

*Caveat - unoptimized settings so known very long pulses

Work to be done for A-STEP

- First flex bus bar designed to connect upper 2 chips in quad chip ✅
- First test of chip daisy-chains
- Scaling of firmware to handle multiple chips / multiple layers ✅
- Mechanical testing of wire bonds, support structure (windowpane-like supports, not solid PCB)
- Flight software for data packetization and telemetry (new sophistication to DAQ)
- Eventual environmental testing of full system
    - Vibration, temperature/vacuum, etc