EIC Calorimeter Readout proposal - eRD109

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with collaboration: LFHCal team, Barrel HCal team, backward HCal team, Barrel ECal team, backward ECal team, forward ECal team

1 Introduction

At the electron-ion collider, the calorimeters cover a large phase space of the collision region. Different calorimeter technologies are considered for different regions of the phase space to maximize the resolution while minimizing the cost of the detectors. The requirement on the readout electronics is to be able to handle all the different detector types provided adequate dynamic range for the lowest to highest energy measurements. In this proposal we are focusing of using the existing H2GCROCv3 as the main readout ASIC for all the calorimeters at the ePIC detector.

2 Progress report from FY23

The work has started on the H2GCROC3 readout scheme. We received a testboard from the Paris-Omega group and ordered a small mezzanine PCB with the H2GCROC3 attached. There are 3 of these mezzanines available now, we still currently have 4 extra H2GCROC3 chips for the prototype production. We used our own existing KCU105 evaluation kit to develop the initial firmware for the readout. The ORNL testing setup can be seen in Figure 1.

The firmware and software were developed for the testing. The combination is enabling to read and write the I2C registers in for the H2GCROC3. Furthermore, it has some debugging features to synchronize the data stream in the FPGA, monitor the idles sent by the chip and I2C PLL lines, for example. There are three readout modes enabled:

- Trigger mode: The trigger threshold can be set and the data is read out only if this threshold is reached by monitoring the trigger lines.

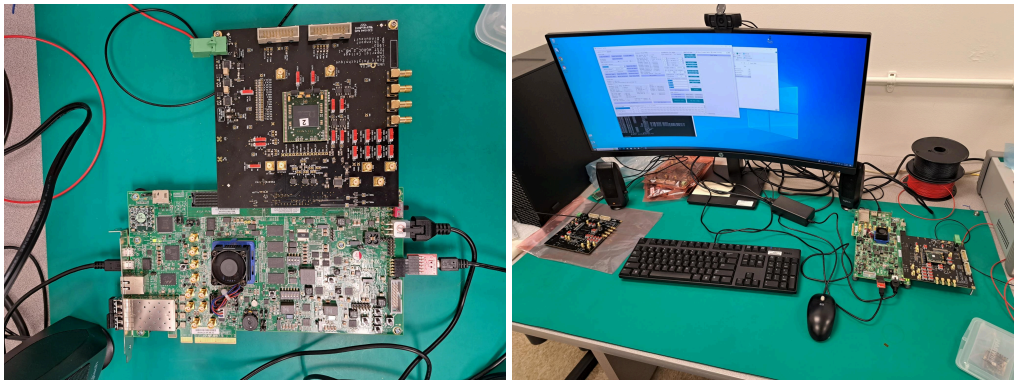

Figure 1: Left figure shows the KCU105 evalutation kit connected to the carrier board (black) and the attached mezzanine with the H2GCROC (green mezzanine with number 2 on the H2GCROC3 chip). The right figure shows the full readout setup with the PC in ORNL EIC test lab.

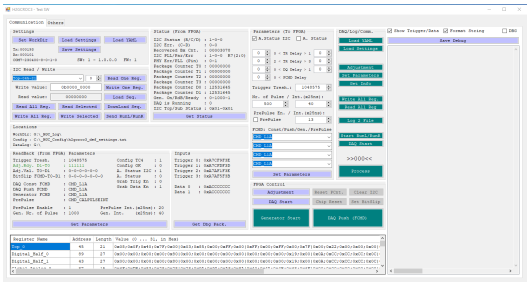

Figure 2: The screenshot for the H2GCROCv3 testing software.

- DAQ push: sends a singular FCMD to read out the data.
- Generator mode: generates FCMD to read out the data in certain intervals

All of these modes can individually set which FCMD is sent for the readout. For this we would refer to the H2GCROC3 data sheet for further reference. There is also an implementation of the Prepulse which is meant to test the internal calibration circuit. It enables us to send a FCMDcalib command and then we can send another FCMDL1A to force the readout after certain interval of 25 ns is passed.

The FPGA firmware also includes a internal logic analyzer to test the data and FCMD packages and delays sent to the ASIC. This is implemented for debugging purposes.

We tested some of the injection signals with the fixed gain setting and scanned the entire shaper using the phase and delay parameters from the I2C setup. There are three injection setting seen in Figure Figure 6. We can confirm that the rise time is 10 ns long and the entire length of the signal is within 100 ns in length. This coincides with the data obtained previously from the CMS collaboration.

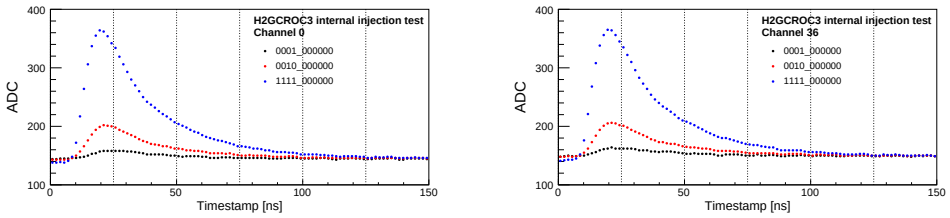

Figure 3: Two internally injected channels (0 and 36) of the H2GCROC3 and scanned over 150ns length. Three different injection pulses in the low injection circuit are shown.

2.1 Remaining studies for FY23

We are developing the first prototype testboard using the H2GCROC3 chip. The PCB is currently under development and should be produced by September 2023. The PCB will contain 2 H2GCROC3 chips and will be compatible with the A5657 CAEN readout board. We implement a switch on the PCB in order to chain the H2GCROC3 on the same I2C line or it can be configured individually if needed. We can then use this prototype to test the different prototype detector and asses the risk involved in using the ASIC for the generic readout scheme.

At the same time, we will further test the H2GCROC3 capabilities using the test setup. In current mode we can scan all the internal calibration signals as presented in the previous section. The current plan is:

- Internal injection test of ADC only (disable TOA/TOT)
- Scan different gain setups and reconstruc the signal shape
- Develop ADC and dynamic range calibration for the ROC
- Develop TOA calibration scheme for all channels
- Develop TOT calibration scheme for all channels

After the systematic checks of the H2GCROC3, we will have command of the entire capability of the chip and will be able to provide feedback to the developers of the chip in order to accomodate the shaper and other parameters of the chip towards the ePIC detector.

3 Development for the FY24

We plan to continue further with the testing of the H2GCROC3 in the next year. The first step will be to combine our current setup with and external injection. This can already be achieved in FY23, however, it will be continued also in FY24. Here, we will focus on the risk involved in using the H2GCROCv3 in the different calorimeter technologies.

By September 2023, we will have our first prototype readout PCB for the calorimeter readout. We plan to test it in September and October at test beam facilities at CERN. These tests will mostly include connecting SiPM on a tile with the H2GCROC3 readout board. Those will show if the H2GCROC3 is a suitable readout ASIC for the ePIC detector.

Furthermore, in FY23 we also changed the design of how the LFHCAL is read out. Instead of wavelength shifting fibers, each scintillator is equipped with a SiPM and the analog signal is led out through a $1.4m$ cable to the back of the detector. We need to investigate the signal propagation over this long line and include it in the R&D for the H2CROC3 readout and any risk involving longer signal propagation and signal degradation as a function of the distance.

In current scheme, each channel will be summing either 5 or 10 SiPM signals from the LFHCal detector. Therefore, we need to develop a summing circuit in front of the H2GCROC3 input. This will be an analog summing, but we have to consider the capacitance of the 5 (or 10) SiPM's in one channel of the ASIC. This summing scheme involves an initial risk when using the H2GCROC3 which was designed for single SiPM readout. We also consider further development for the firmware and software of the readout, which is now implemented in the FY24 budget proposal, see Tab. 2.

The often raised question about the H2GCROCv3 is the temperature stability of the gains and linearity. We plan to test the full capability of the ASIC in an environmental chamber with internal and external injections. Especially, the concern is the transition of the ADC-TOT region. Currently, it has a known non-linearity around the threshold region and we plan to investigate it at different temperature and humidity conditions.

We also plan to investigate the H2GCROC3 use in different calorimeter technologies. The main purpose is to investigate the feasibility of using this ASIC in other calorimeter readout explained in Section 13. The collaboration with the other detectors would require to visit the corresponding laboratory spaces and testbeam facilities in order to test the readout architecture with their prototype. The Tab. 2 also includes the travel budget requested for this purpose for FY24/25.

The main goal of the FY24 is to asses the current capability of the H2GCROCv3 and then identify in applying the ASIC for all six of the ePIC calorimeters. At the end of the study we also need to create a comprehensive list of improvements which can be made to tailor the current ASIC for the ePIC detector and avoid further risk in its usage.

4 Overview of the readout electronics

All calorimetry in ePIC will use Silicon Photomultipliers (SiPM) for their readout. However, the number of channels and input signals and capacitance varies greatly from detector to detector. One has to take into account also the radiation damage the SiPM will suffer throughout the years of running.

The basic block diagram of the readout system requirements is shown in Figure 4. The first part of the readout electronics is the voltage regulators for the individual SiPM's and the corresponding dark current monitoring system. The next part would consist of the pre-amplifiers and shapers, which then would be digitized by the ADC. We consider a minimum need of 12 bit ADC readout to reach the desired resolution for all the calorimeter performances.

Another part of the readout consists of the time counters and hit detection which will be stored in a FIFO for the final readout. We would further require a zero suppression which will be sending the final signal out via LVDS cables towards the ePIC DAQ. The ePIC data acquisition requires streaming readout from all of its detectors via their planned FELIX boards; hence, all readout electronics has to be compatible with this scheme. Furthermore, the DAQ runs with the 100 MHz beam clock.

The minimum requirement for each calorimeter is to be able to identify the single MIP

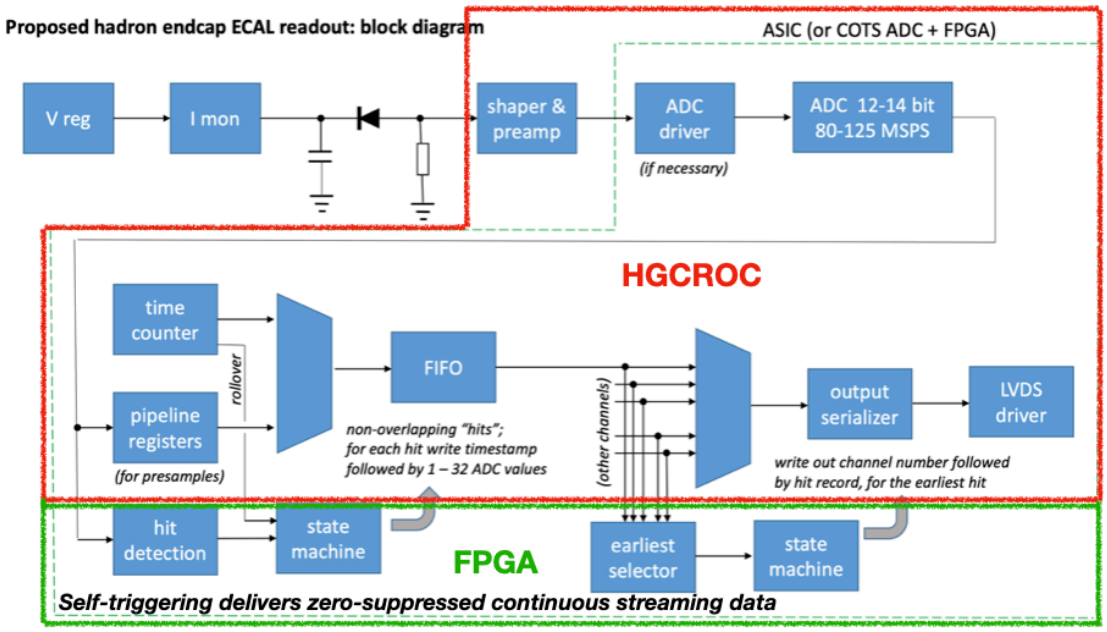

Figure 4: The block diagram of the required readout electronics for the calorimeters at ePIC. The highlighted region in green box could be included in an ASIC with an FPGA controlling the hit detector and the zero suppression.

particle from noise, as well as extend its upper limit towards 120 GeV particle showers. Considering the readout electronics, we expect at 500kHz interaction frequency about 1/10th of the rate per channel in the forward electromagnetic and hadronic calorimeters, which would receive the highest particle flow per channel. The input capacitance for each channel would range from 60 pF to 5 nF.

The forward calorimetry itself combining the electromagnetic, hadronic and insert calorimeters would add up to almost 90k channels, while the rest of the calorimeters with SiPM readout (not including the imaging calorimeter) would result in 43k channels. The forward calorimeter group is unique as it requires most of the electronics on the detector, while keeping it very compact due to the limited space. Therefore, we plan to implement a very power efficient scheme for the readout electronics using ASICs which would avoid using additional cooling (cost and space).

5 ASIC consideration: H2GCROCv3

Using an ASIC in the readout of the calorimeter is a very cost effective, more radiation tolerant and cooler (i.e. consuming less power) solution. From the ASICs available on the market today, we choose the H2GCROCv3 chip. The H2GCROCv3 chip was developed by the Omega group for the primary use for the High Granularity Calorimeter (HGCAL) for the CMS detector at LHC, making it a great fit for any calorimeter readout. The ASIC requirements for this detector are very low noise level, low power consumption (20 mW /channel), and very good ($< 1\%$) linearity throughout a very large dynamic range. The basic block diagram is shown in Figure 5. The chip has two versions, one for the silicon sensor one for the SiPM; we concentrate on the latter only, which includes also a current conveyor where each channel's bias voltage can be fine tuned from the ASIC itself.

The H2GCROCv3 has 72 input channels (and additional common noise and calibration channels). The ASIC provides measurements of the 10-bit ADC, 10-bit TOA and 12-bit TOT. When the ADC saturates, the TOT would extend the dynamic range resulting in a 22-bit total dynamic range; in the SiPM version the input signal range is from 160 fC to 320 pC. It runs nominally on the 40 MHz LHC clock and implements two buffers of 512-deep RAM1 and the 32-deep RAM2. There is also an internal trigger path which sums up 4 or 9 channels and streams out with 40 MHz cycles. The ASIC outputs are 2x data links and 4x trigger links at 1.28 Gbit/sec. The ASIC itself requires a trigger input to shift the data out from its buffers. The slow control is handled by the I2C protocol via the so called "slow control" communication port, the clock and trigger information is sent via the so called "fast commands" communication port.

The ASIC is rated for LHC-HL runs for $10^{14}\mathrm{n/cm^2}$ neutron flux, which is 2-3 orders of magnitude larger than expected at mid- and forward-rapidity at the EIC. Therefore, we can consider the H2GCROCv3 to be radiation tolerant for the full run of the EIC. The feasibility of the H2GCROCv3 should be tested to determine if the shaping time of the signal is enough to reconstruct the signals correctly. Therefore, a small study was conducted, using the realistic shaping time shown in Figure 6. The signal will be sampled by the H2GCROCv3 with a 40 MHz clock, while the collisions at EIC will happen at 100 MHz clock cycle. The consequence of this will be a natural phase shift of the signals, resulting in 5 distinguished shapes of the distribution. However, if we sample 3-4 samples around the maximum of the signal, we can apply a template fit and realistically reconstruct the maximum of the signal in each phase. In addition, the TOA measurement provides very good approximation in which phase we will be of the five possible cases.

The TOA would provide us further information about the timing information, not only usable for the determination of the phase. The timing is in 25 ps increments and should have beneficial physics-analysis implications as well, which could be further studied with simulations.

6 Adaptation of the ASIC to ePIC

The H2GCROCv3 evaluation board and sample chip is provided to us by the Omega group for the basic studies of the chip. The carrier board (Figure 7) interfaces to a KCU105 Xilinx evaluation board, for which we obtained the necessary firmware.

The first step is to study the characteristics of the ASIC parameters. The main goal is to

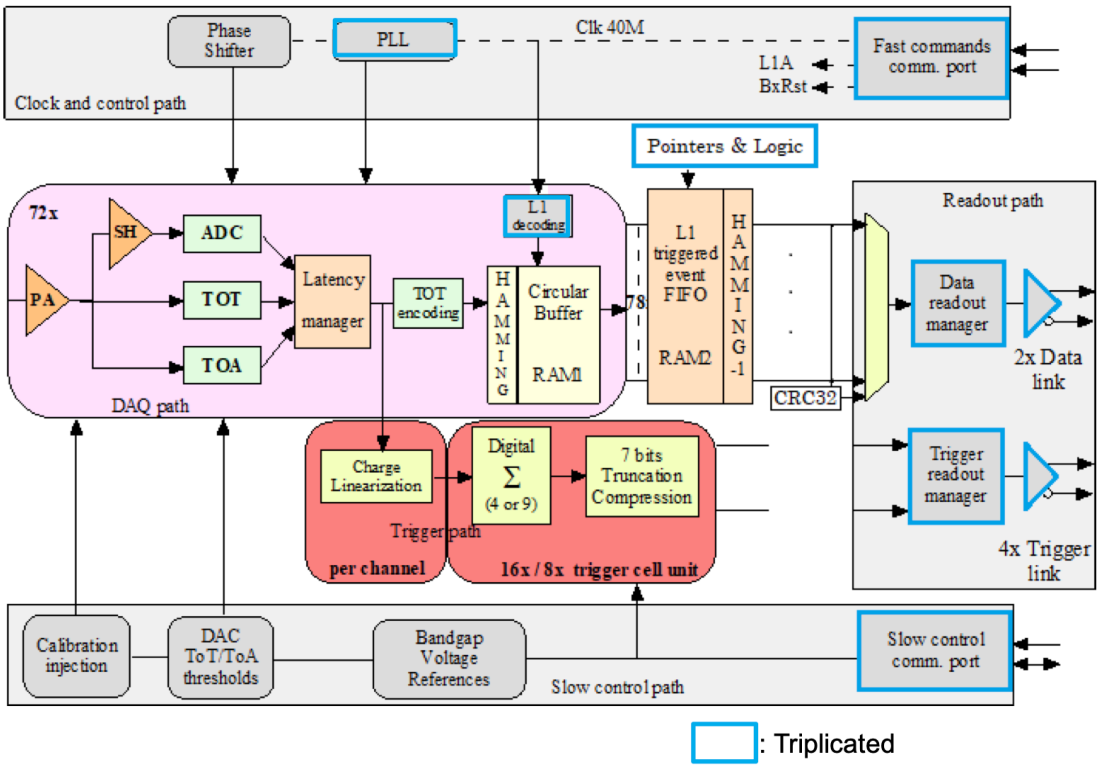

Figure 5: The block diagram of the H2GCROCv3. The pink box is the ASIC measurements, the red boxes are the trigger paths. The RAM1 buffer is 512 deep, always includes all the channels measurements (ADC, TOA and TOT), the RAM2 is 32 deep. All the blue boxes are triplicated for radiation tolerance.

study the feasibility of adopting this ASIC to the EIC calorimeters. The test would include a full characterization of the chip itself, including the linearity and threshold setups for the TOA/TOT's. Another test will be the readout of the 3-4 samples and stress testing the maximum readout speed achievable in realistic conditions from the chip.

The carrier board allows us to access the input pins of the different channels. While the ASIC provides an internal injection test, we also need to test with an external injection where we can easily control the amount of charge injected to each channel. This will also allows us to study the cross-talk between the channels.

Further tests can be done by connecting a planned SiPM directly to the input pins and test the full response of the ASIC with different light sources. We could test different quality and sizes of SiPM's, including also irradiated SiPM's. These tests will further expand if this ASIC

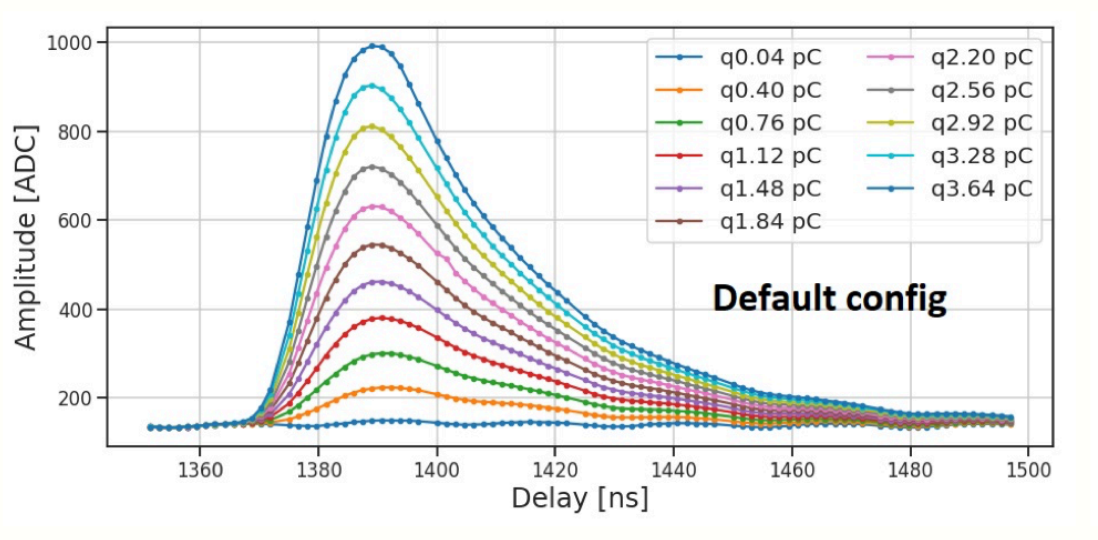

Figure 6: The signal from the shaper of the H2GCROCv3 with the default configuration

Figure 7: The carrier board (left) and the mezzanine board with the H2GCROCv3 (right)

is feasible as a readout chip for realistic EIC conditions.

Proposed milestones:

- Phase 1: Full test of the H2GCROCv3 capability using internal injection capability of the ASIC and compare with a well calibrated external injection results. Study of the linearity, dynamic range and current conveyers of the ASIC
- Phase 2: Connect the testboard to a SiPM sensor and test the readout and voltage compensation of the ASIC
- Phase 3: Test all possible input signal shapes and SiPM technologies planned in the ePIC

detector. Additional irradiated sensor should be tested

7 Development of voltage and dark current monitoring

The experience from previous experiments operating large numbers of SiPMs in radiation environments shows that it is crucially important to keep close track of the SiPM bias voltages and dark currents over the course of the operating lifetime of a detector. To this end, the designed system must not be susceptible to adverse effects from irradiation itself.

The H2GCROCv3 ASIC offers integrated bias voltage trimming in the range of up to 2.5 V, which still requires a base bias voltage supply that the individual channel trimming applies to. This base bias voltage requires high precision monitoring to ensure that operation of each SiPM at a defined working point in gain and photon detection efficiency. This requires a circuit design which either incorporates a radiation hardened band-gap reference or an externally supplied reference voltage.

In addition, the implemented design should enable current monitoring of individual SiPM channels to track radiation damage, quickly diagnose broken and noisy SiPM and potentially even provide an estimate of beam backgrounds.

A SiPM biasing and monitoring system has been previously implemented as part of the STAR FCS readout system by Gerard Visser, as shown in Figure 8. It provides regulated, temperature compensated bias voltages to individual SiPMs with integrated current monitoring and over-current protection. The original design has been proven to be robust over several years of operation. Some R&D for minor modifications to the circuit are required to adapt this concept to serve the 56 SiPMs per LFHCAL module and to properly integrate with the H2GCROCv3 bias adjustments.

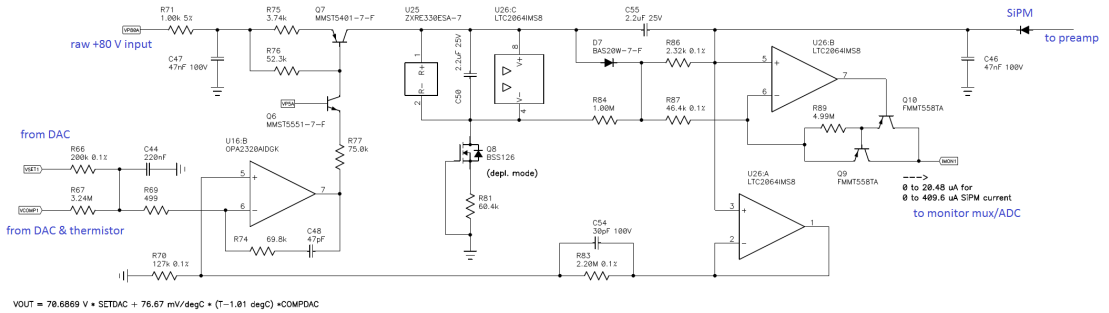

Figure 8: The bias voltage control and monitoring system diagram as developed for the STAR FCS system

8 Prototype development for ASIC board

The next step is to develop a readout board with the H2GCROCv3 to be used as a part of the readout electronics for the calorimeter readout. There are several methods of the final readout board which has to be investigated: - on-board electronics, the ASIC is directly placed on the

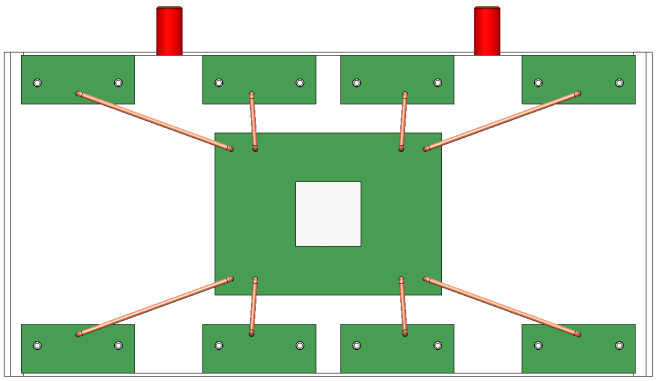

Figure 9: The illustration of the on-detector readout electronics for the LFHCal detector. The 8 small boards each contain 7 SiPMs and are connected to the main readout backplane containing the HGCROC in the middle.

detector - off-detector electronics, the signal cable from the active sensor is connected via long (few meters) cable to the input of the ASIC electronics.

The first plan is to develop a readout electronics PCB for the LFHCal and subsequently for the forward ECal detector. The LFHCal has an available area of 10x20cm in the back of the detector, which would easily fit the ASIC board with 8 individual SiPM boards containing 7 SiPM's each for the readout. The planned illustration of the back-plane on the LFHCal is shown in Figure 9.

However, during the FY23 of the R&D phase, we discovered probable weakness in the design using the wavelength shifting fibers. The design was changed to mount each scintillator with a SiPM and lead out the analog signals electrically. This method would be more safe, but it brings also other questions about the length to get the analog signal out. Another question is the grouping of the channels. The H2GCROCv3 was designed to read out a single SiPM, and we plan to sum up 5 or 10 analog signals from the SiPM's and read it out in a single channel.

The physical connection of the 4×2 Scintillator tile with the 8 SiPM's will sit on a flex PCB and it has to be connected to a long PCB which will lead out the signals to the back of the detector, see Figure **??**. This connection is non-trivial to make and not deform the analog signal. We plan to pursue several options in order to deliver the signal towards the back of the detector. This technique might be used also by other detectors where the SiPM and H2GCROCv3 should be 1-2 meters apart.

We also plan to develop a summing board on the H2GCROCv3 input. It would sum up the analog signal from different SiPM's and provide it towards the ASIC input as one channel. Here we have to test the capacitance of this input channel and feasibility to use it with the ROC itself. In LFHCal we plan to sum 5 or 10 SiPM signals, but the solution of such circuit would be applicable also in other calorimeter projects also, see Section 13.

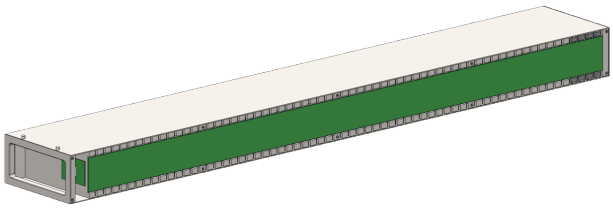

Figure 10: The new design of the LFHCAL module as seen from the back of the detector. Each layer would consist of 2×4 Scintillator on SiPM tiles and the long green PCB would bring out the signal to the back. Here would sit the FEB with the summing board and the H2GCROCv3 .

After a successful test beam of the LFHCAL detector, we would like to study how to adopt to the other calorimeters. We would like to set up some milestones for the development of the prototype boards:

- Phase 1: Prototype board for the LFHCAL detector. One H2GCROCv3 reading out 56 channels.
- Phase 2: On-detector prototype board for different calorimeter design - forward ECal, forward insert detectors
- Phase 3: Off-detector electronics for barrel calorimetry and backward calorimetry

9 FPGA and firmware development

The Omega group together with the CMS groups developed firmware based on the Xilinx KCU105 evaluation board which is ready to use. It has all the basic functionality to be able to read out and test the H2GCROCv3 . Further firmware development for our needs can be done at ORNL.

We need to implement multi-buffer entry readout, reading out at least 3-4 consequential buffer entries to reconstruct the full signal shape. This was already demonstrated with the CMS development, proving the feasibility of this feature of the ASIC. The next phase is to optimize the calibration for the ASIC, and this could be done also by a rapid firmware code between the FPGA and the ASIC itself.

We then define the following milestones:

- Phase 0: Basic capability to readout the ASIC
- Phase 1: Optimize the ASIC parameters for the SiPM readout at EIC and readout multiple consecutive bunch crossings
- Phase 2: Improve the communication between the FPGA and ASIC in order to complete rapid calibration and optimization. Determine the thresholds and apply zero suppression

10 Integration to FELIX streaming readout

One of the main requirements of the ePIC detector readout is to be compatible with streaming readout. While the H2GCROCv3 ASIC itself requires a L1 trigger signal to be read out (see in

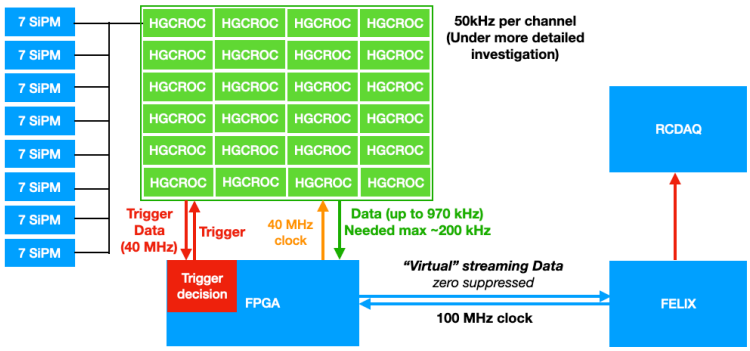

Figure 11: Schematic view of the proposed readout electronics for the LFHCAL. Each tower will be readout out by 7 SiPMs. The H2GCROCv3 will handle 56 channel (out of 72), while the FPGA will be handling up to 24 ASICs each. The FPGA and H2GCROCv3 will contain the local trigger information (in red line), providing fast decision timing and zero suppression. The FPGA will derive the 40 MHz clock (orange) from the provided beam clock of 100 MHz (blue line). The data will be 'virtually streaming' towards the FELIX board and the DAQ system.

Figure 5), the maximum readout speed of of 72 channels (32-bit each) with 2x1.28Gbps lines is 970 kHz. The expected interaction rate at the EIC is 500 kHz, which would translate to the probability pre-channel hit to 50kHz in the forward region. The proposed readout of 3-4 bunch crossing samples of the signal shape would then require 150-200 kHz readout speed, way within the reach of this ASIC.

Therefore, we propose a readout scheme where the FPGA would receive and process the trigger lines from the H2GCROCv3's and making a very quick decision to move the event into the ASIC buffers. The RAM1 buffer size is continuously filled for each clock cycle with the depth of 512 registers, creating a limitation to receive the L1 decision within 12.5 μs. The required information is then stored in the RAM2 buffer of depth 32 registers while waiting for a readout signal from the FPGA. The trigger decision would be localized between the FPGA and the ASIC only.

The FPGA will then aggregate and stream out the zero suppressed data towards the FELIX board and the DAQ system. We can also stream out some of the trigger data in order to optimize it to each detector design. This will ensure the maximum efficiency of the virtually streaming readout while also sending out zero suppressed data.

We require further detailed simulation studies not only of the expected hit/channel simulation, but a full simulation of the detector including very good description of the expected beam backgrounds. However, the readout capability could be increased by almost by factor of 4 without changing anything in the ASIC design, further if we only require 3-sample

streaming.

11 Service reduction for the readout boards

An additional study we include in this proposal is the R&D on the service reduction towards the detector. The priority is the reduction of the number and thickness of the cables, making the readout electronics on the detector as compact as possible. Due to the limited space, the gigabit trigger and data cables could occupy more space and increase the cost of the readout electronics.

This reduction is in very good synergy with the eRD104 proposal, and we plan to implement it in similar way. The ASIC requires one low voltage and one bias voltage line and the gigabit lines could be reduced to optical fibers. It would include the survey of what is available on the market and find a good solution for implementation. Optical fibers would provide a cheap and compact design for the electronics, not producing additional heat in the limited space of the readout.

In current plan we include a Samtec cable test from their HQDP series. The principle of this test is to see if all the services for a single FEB could be provided by this single cable. This would include the data transmission of 2×1.28 Gbps, LV and bias voltage lines, slow control (I2C) and FCMD lines, including the 320 MHz clock needed for the ASIC. This test would significantly reduce the services required between FEB and RDO's. In FY23 we already ordered the cables at different lengths, 1 meter, 3 meter, 5 meter and 10 meter lengths. The cable itself is rated up to 14 Gbps up to 1 meter length. We plan to test the data transmission for the different lengths also in FY24.

12 Cost and timeline estimations

We summarize the advantages of using the proposed solution of the readout electronics:

- 20mW per channel, total power consumption 2.56 kW for the whole EIC calorimetry (128.2k channels)
- Compact readout electronics
- Cost effective, one ASIC is about 0.3$/channel
- Compatible with the required streaming readout

As mentioned above, the carrier board and the H2GCROCv3 chips were provided to us already by the Omega group. We have available KCU105 boards to connect with the test setup and start the calorimeter development. The table in Figure 12 shows the tentative plan of the development of the readout electronics and also the plan to adopt it to different calorimeter groups. From the first initial number, the HGCROC should be able to work with all of the different calorimeter technologies. The tests with the different calorimeter groups is planned to be performed in FY2024-2025.

The H2GCROCv3 chip already exists, and it is already tested by the CMS collaboration for their upcoming upgrade HGCal detector which comes online in 2028. Several testbeam efforts were already performed with the previous and current generation of the chip, mostly led by

Table 1: Total funding request by institution for each R&D activity.

cost in k$	FY 2023	FY 2024	FY 2025	total
material	7	10	10	27
licenses	-	10	10	20
el. engineering	32	24	16	72
el. engineering (in-kind)	4 week	3 week	2 week	9 weeks
physicist (in-kind)	0.5 FTE	0.5 FTE	0.5 FTE	1.5 FTE
travel budget (domestic)	-	10	10	20
travel budget (international)	-	10	10	20
total	39	64	56	159

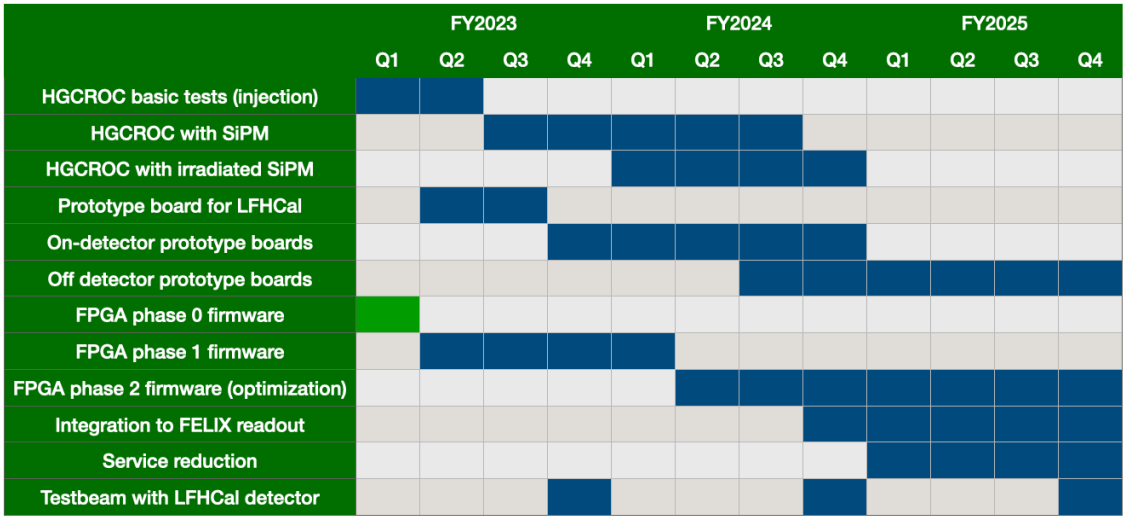

Figure 12: Time line of the development of the calorimeter readout with the HGCROC ASIC.

the CERN and DESY groups at CMS. We plan to benefit greatly from their progress and we focus on adopting the chip for the EIC use in the different calorimeter technologies.

The cost estimation driven by material cost and engineering time is summarized in Tab. **??**. The cost of the material include the PCB's and the components to produce the prototype boards for the H2GCROCv3 and also the FPGA prototype board. Furthermore, the off-detector

prototype board requires combining the ASIC and FPGA boards together. The el. engineering cost covers both the design of the PCB as well as the firmware development needed.

13 Additional studies for applying to different calorimeter readouts

13.1 Dedicated studies for the backward ECal at IJCLab

The backward endcap electromagnetic calorimeter has the most stringent demands in terms of stability, channel-by-channel variations, linearity and power dissipation. Its requirements makes it an excellent subsystem for testing and validating H2GCROCv3 as a common ASIC for calorimetry at EIC.

The choice of SiPM for the backward endcap calorimeter is almost finalized and would most likely be either Hamamatsu's S14160-6010PS (10 μm pixels) or S14160-6015PS (15 μm pixels). Their terminal capacitance at operating voltage is 2.5 nF. We plan to use 4 SiPM per crystal, with either a serial or parallel readout in each crystal.

The group at IJCLab, together with LLR and OMEGA, plan to focus during FY24 in validating the readout of the backward endcap calorimeter with H2GCROCv3. The LLR (Laboratory Leprince Ringuet) in Palaiseau has extensive experience with the HGCROC chip as they have been heavily involved in its characterization for the HGCAL calorimeter of CMS. Their group, together with their engineering support, would like to get involved in ePIC and in particular in the electronics of the backward ECAL. The OMEGA group, also in Palaiseau, is planning to significantly support this effort. The interface with the calorimeter cooling system and other services under design at IJCLab will make this collaboration particularly effective.

We will setup a test-bench with Hamamatsu's S14160-6010PS and S14160-6015PS SiPMs using a Xilinx149 KCU105 evaluation board. We will first characterize the chip using internal injection and then with laser optical bench (already available from previous developments for CMS). All basic functionalities will be measured, with particular attention to linearity, resolution and gain stability. Some measurements with irradiated SiPM would be also possible, in order to check the minimum detectable signal due to pedestal broadening.

Table 2 shows our funding request for FY24 with an estimate for FY25. Material costs include the Xilinx, PCB boards and components. Labor request is for student support, physicist and engineering labor are provided in-kind. A small amount of travel funds are also included.

Table 2: Funding request by IJCLab

cost in k$	FY 2024	FY 2025	total
Material	8	10	20
Student support	7.5	10	17.5
Travel	1.5	2	3.5
Indirect cost	3.4	4.4	7.8
el. engineering (in-kind)	1 FTE	1 FTE	2 FTE
physicist (in-kind)	0.5 FTE	0.5 FTE	1 FTE
total	20.4	26.4	46.8

13.2 Dedicated studies for the Barrel ECal calorimeter

The Barrel ECal detector will be based on a design similar to the existing GlueX Barrel ECal at JLab. The scintillating fibers will be read out on the side of the absorber-scintillator sandwiches. Each module will be 4.35 meters long and consist of 60 cells, to which a lightguide and a SiPM array will be attached. It's important to note that these towers are oriented in the transverse direction, and the SiPMs are placed on the side of the detector to register signals from showers developing radially. The plan is to connect each of these transverse cells to an individual channel in the H2GCROCv3 .

There is already an existing small-scale GlueX Barrel ECal prototype called Baby BCal, which utilizes SiPM wedges with S12045(X) arrays from the GlueX detector. In FY24, there is a plan to integrate the system with thinner Scintillating Fiber Imaging Layers (SFILs). The SFILs will be instrumented with new SiPMs, most probably S14161-3050-04 Hamamatsu arrays. The goal of this R&D program is to implement our prototype PCB with the H2GCROCv3 and test it in the FNAL test beam facility using the small-scale ePIC Barrel ECal prototype. One of the crucial tests for this detector is to evaluate the timing resolution, as it directly translates to the position resolution along the detector. Unlike GlueX, the ePIC Barrel ECal also includes AstroPix Si sensor layers, which provide more precise position resolution compared to conventional calorimeters. However, it's important to note that the AstroPix layer readout is not included in this RD phase, only the scintillating fiber SiPM readout.

13.3 Dedicated studies for Barrel HCal detector

The barrel hadronic calorimeter for ePIC is a re-use of the existing sPHENIX Barrel HCal. The scintillating tiles and steel absorber structure will be used as-is, but the electronics and readout will be upgraded to read out the individual scintillating tiles using the HGCRCOCv3. The existing SiPM's will be replaced with the Hamamatsu S14160-3015PS, which maintains the high pixel count ($\sim$40k) and form factor (3x3 mm^2) of the existing SiPMs used in sPHENIX.

In the ePIC configuration, the HGCROCs will be located on-detector (on the ends and/or center of the sectors) and connected to the tile SiPM's by μ-coax cables of a length $<$ 3m. To test the ePIC barrel HCAL electronics chain it will be highly advantageous to plan a test beam with pre-production electronics to verify conformance with the detector requirements. To this end, the outer HCAL prototype fixture that was used for the sPHENIX test beams is available and can be populated in either a mid-rapidity or high-rapidity configuration using spare tiles from the sPHENIX production (see Figure 13). The goals of the beam test would be to verify the detector performance using the full ePIC reaodut chain, including the long runs of μ-coax and HGCROCv3 digitization. This testing could be done coincident with other beam tests of ePIC calorimetry and readout.

Figure 13: The fully assembled outer HCals sPHENIX test beam sector prototype. Each section has 20 steel absorber plates stacked together and 80 scintillating tiles are inserted between them. SiPMs read out from five tiles are ganged together like a tower in sPHENIX, but in the ePIC configuration each tile will be read out independently. This configuration is sufficient to contain a few GeV hadronic shower initiated in the center of the detector.