Status of EIC-Incom PED contract & related activity

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eRD110 Consortium Meeting, July 20, 2023

Overall status and expectations

- Contract was signed by JLAB and Incom end of June
- The respective “major” HRPPD component orders were placed shortly afterwards
  - Our custom anode base plates
  - 3.8mm thick sapphire windows
  - Samtec interposers are not ordered yet, but are not a long lead item either

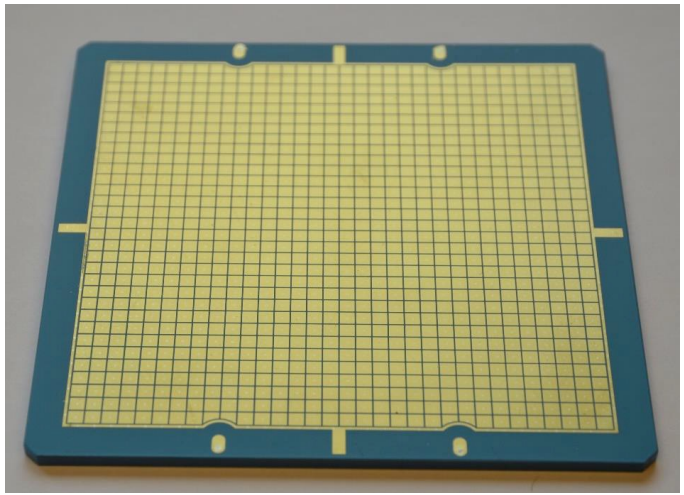
- Base plates are expected from Kyocera end of November
  - However, a usable first article will hopefully become available much earlier
- This essentially means:
  - We should be able to see a first EIC HRPPD end of Fall 2023
  - Our original plan to have five tiles by March 2024 *does not look unrealistic*
  - One can think of a short beam test in January-February 2024 as listed in the eRD110 FY24 proposal …
  - … with a caveat that FY24 funding may not become available by early 2024

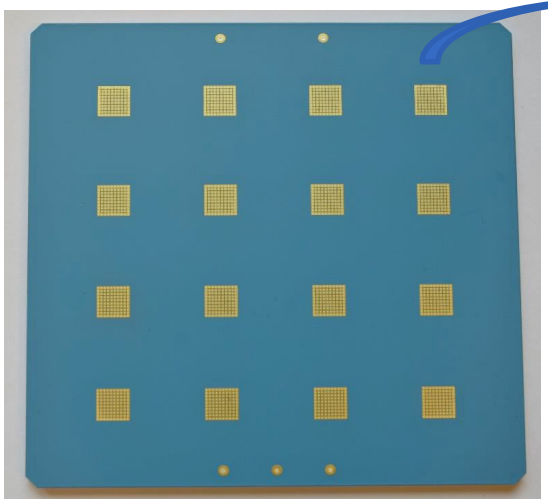
Overall status and expectations, cont'd

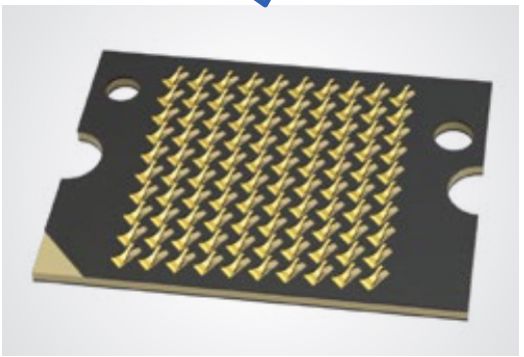
- A dummy backplane with Samtec ERF8 connectors is already ~designed (BNL)
  - Technically can be ordered any time
  - (M)MCX interface adapters yet needs to be discussed (and we have no FY23 funds to order them)

- Work on the ASIC backplane started already
  - OMEGA group will come up with an ASIC board design by the end of September
  - ~100 required HGCROC3 ASICs can be provided ahead of FY24 funding availability
  - We should make an effort to order a pilot version in October, either this or that way
  - Debrecen University group will start with the FPGA board design in the second half of September
  - KCU105 FPGA kit, Oak Ridge carrier board and a mezzanine board with a single HGCROC3 ASIC will all become available at BNL for a DAQ driver development by the end of July (hopefully)
- If funding is available in early Fall 2023, be that R&D or PED, making two iterations of an ASIC board and an FPGA board by ~March 2024 *does not look unrealistic*
  - And we only need this interface by the time of the pfRICH beam test in May-June 2024

First iteration: anode base plate Y03e (Techtra)







Stock interposer with 800 μm pitch

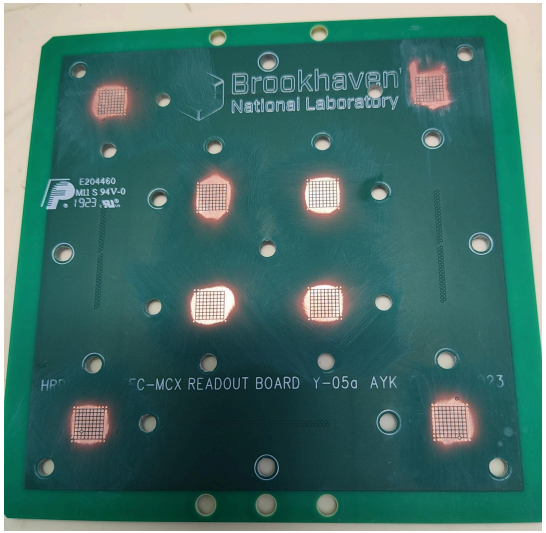
Full size (120mm) HRPPD anode plate by Techtra

Ceramic plate Y03e, matching 800 μm pitch Samtec (stock) interposers: trace specs appeared to be too tight for implementation (~10% shorts)

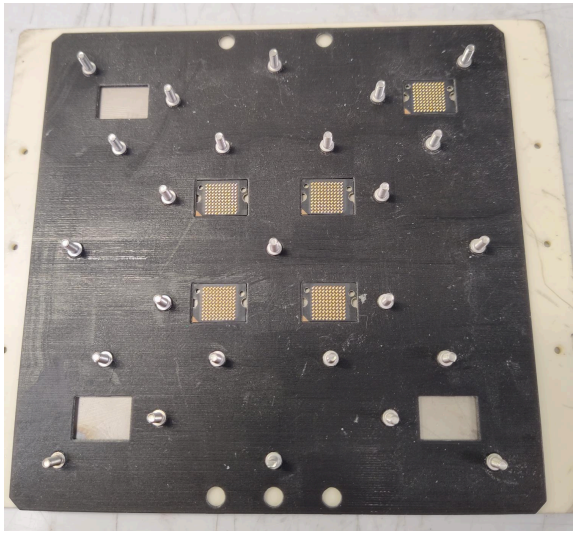
-> Incom is planning to build a functional prototype out of this base plate anyway

First iteration: a matching Y05a connector board

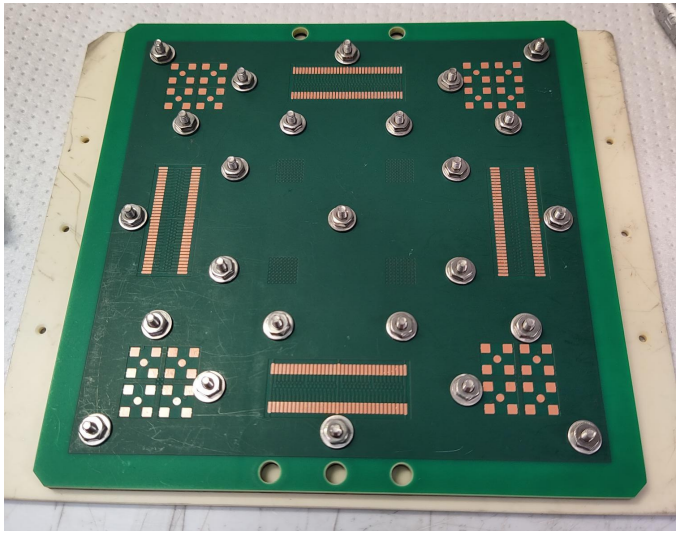
Case #1: double-sided (floating) 800 μm pitch Samtec interposers



Bottom (interposer) side



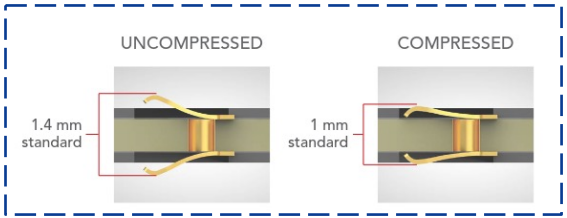
3D printed spacer, screws, interposers



Full assembly; top (connector) side

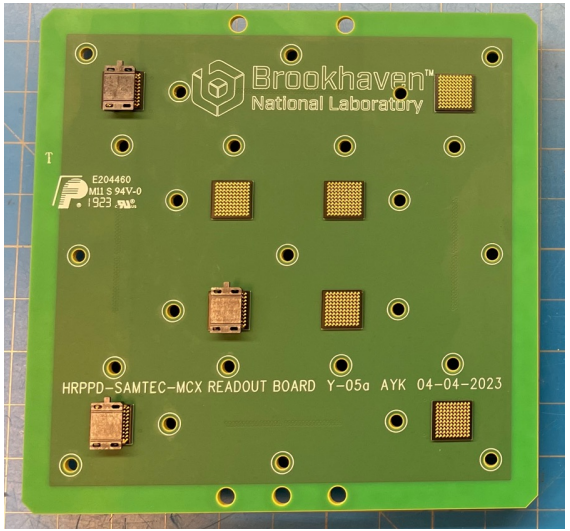
-> Electrical connectivity is confirmed,
as well as mechanical integration overall

Next step: signal quality check

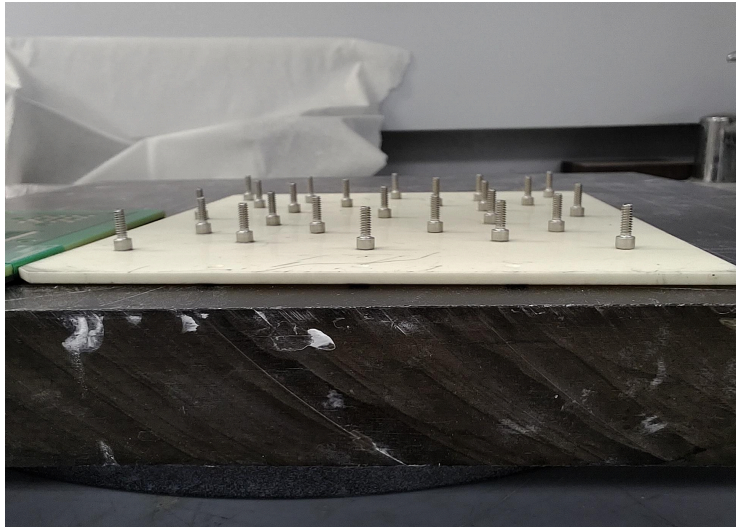


First iteration: a matching Y05a connector board

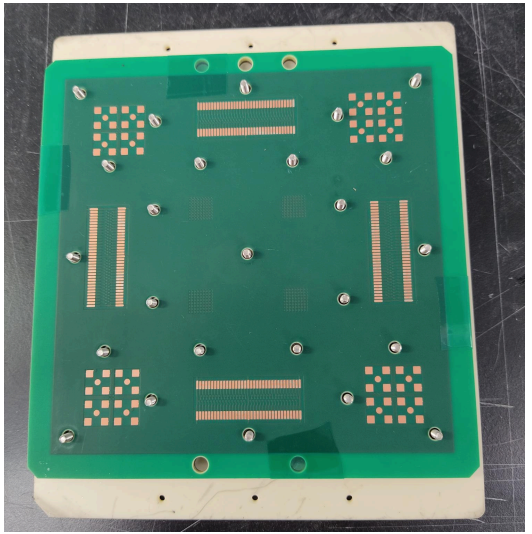
Case #2: single-sided (soldered) 800 μm pitch Samtec interposers



Bottom (interposer) side

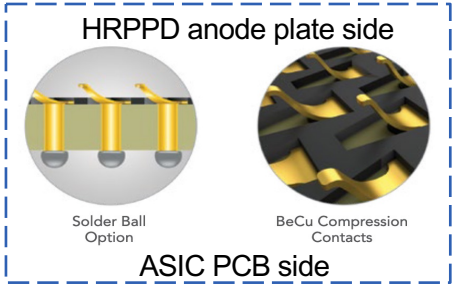


Screws epoxy glued onto a dummy ceramic plate

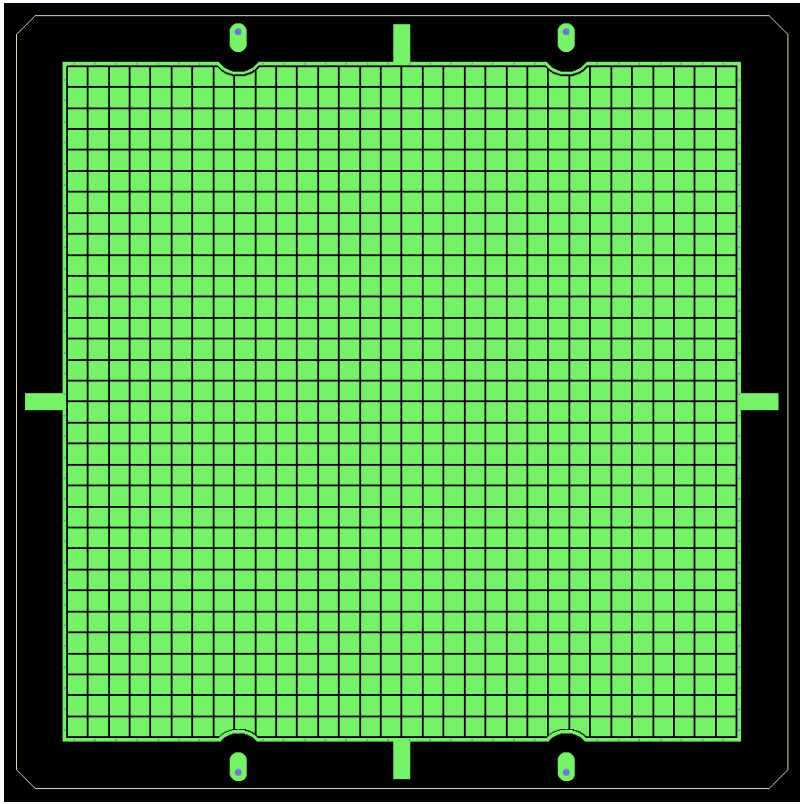


Top (connector) side

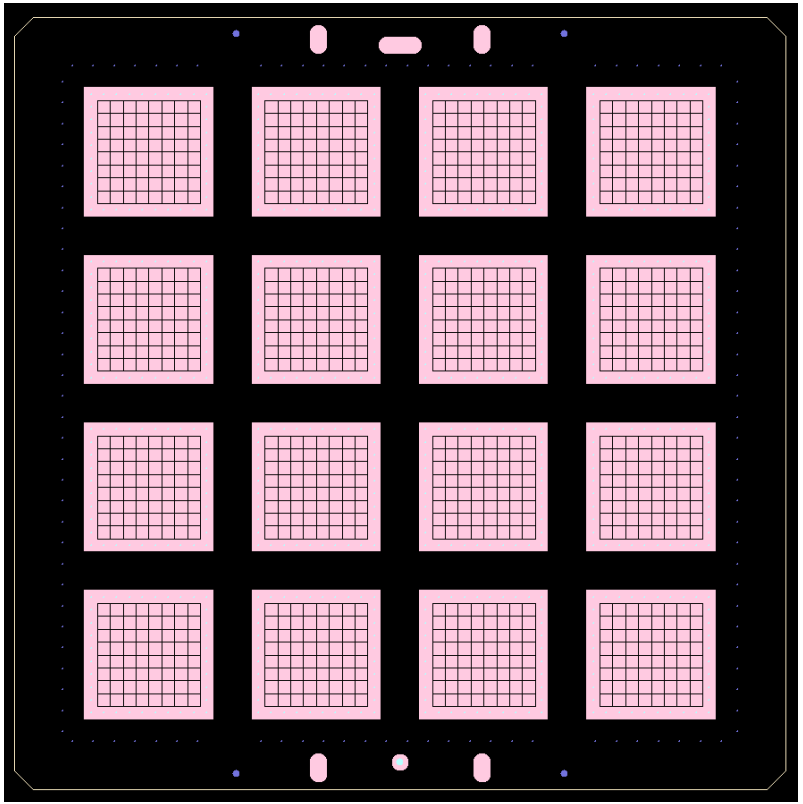
-> Have not been tried out yet
(but is not a leading option either)



“EIC HRPPDs”: base plate Y03h (Kyocera)

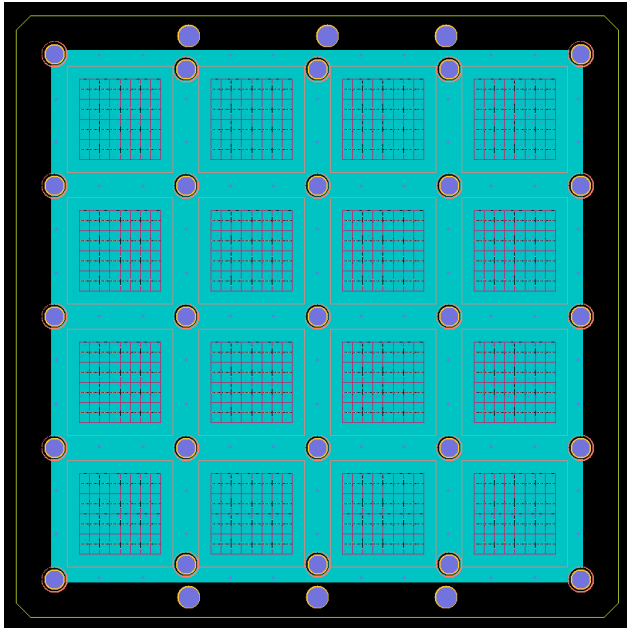


Inner side with a 32x32 pad uniform layout (3.25mm pitch)

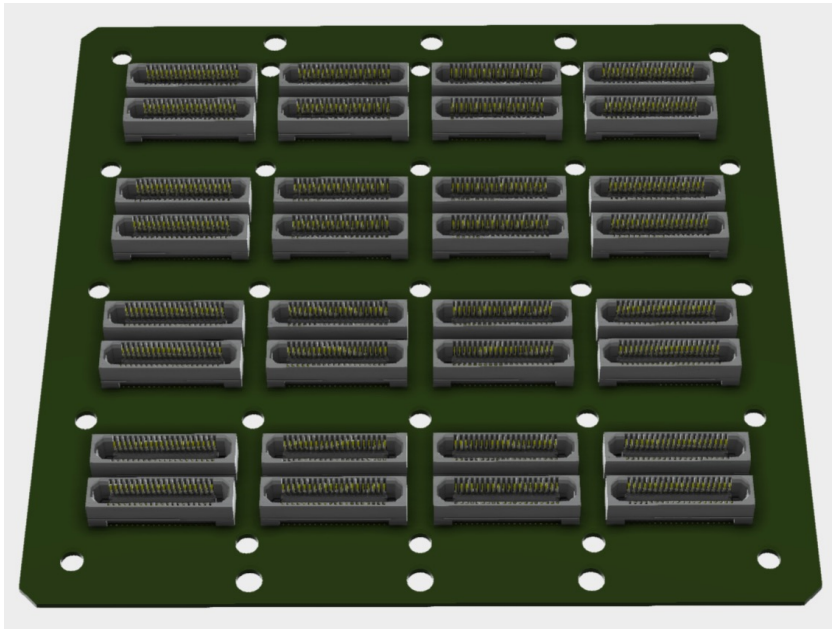


Outer side with 4x4 8x8 pad fields (2.0mm pitch)

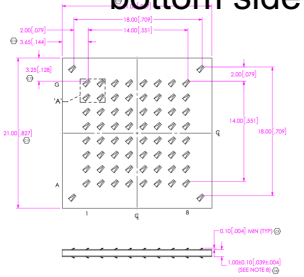
EIC HRPPDs: a dummy readout board Y05d



bottom side (matches HRPPD rear side)

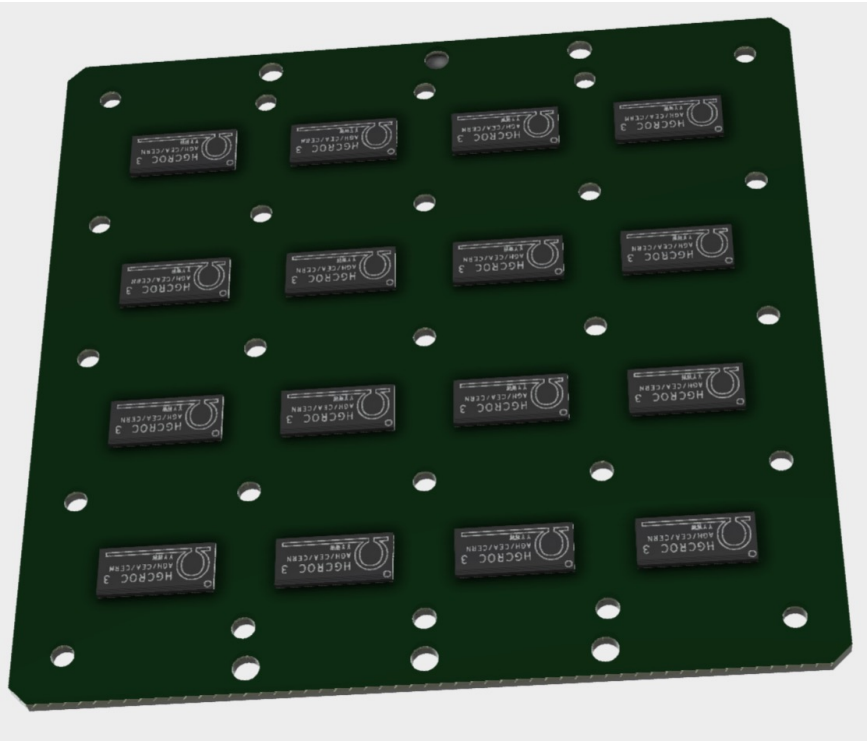


top side (32 ERF8 connectors)

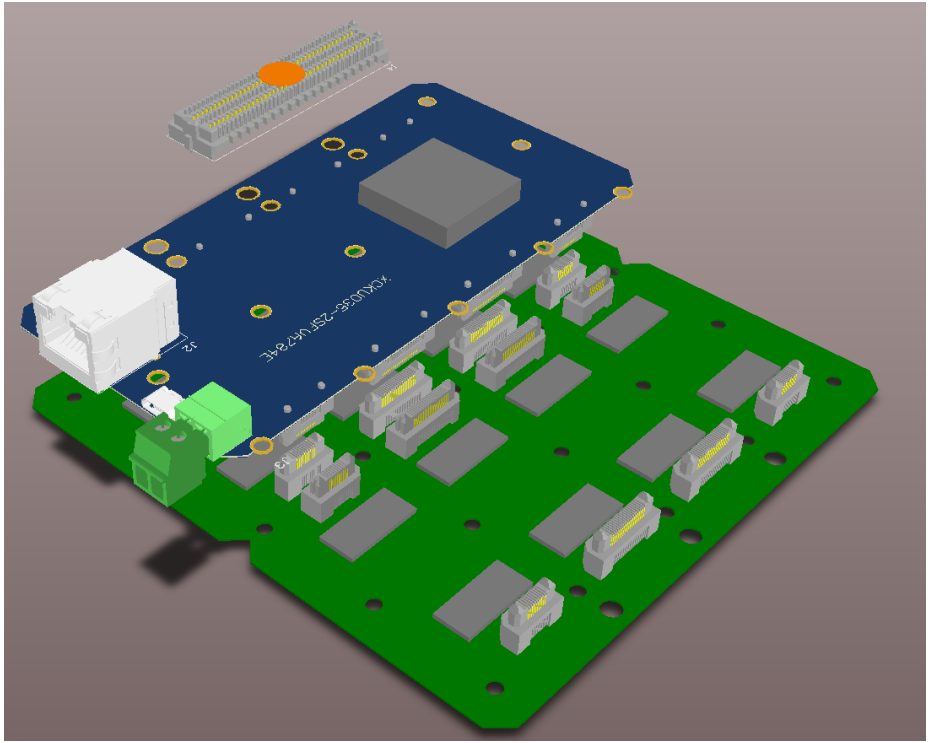


- Connectivity proposal for any of the sixteen 8x8 pad fields:
  - A set of [2x ERM8 -> MMCX] adapters, either 16ch (4x4) or 32ch (4x8; 6x6-4) at a time
  - A set of grounding caps for all other 8x8 fields

EIC HRPPDs: HGCROC3 ASIC backplane



EIC HRPPD ASIC backplane layout (OMEGA group)



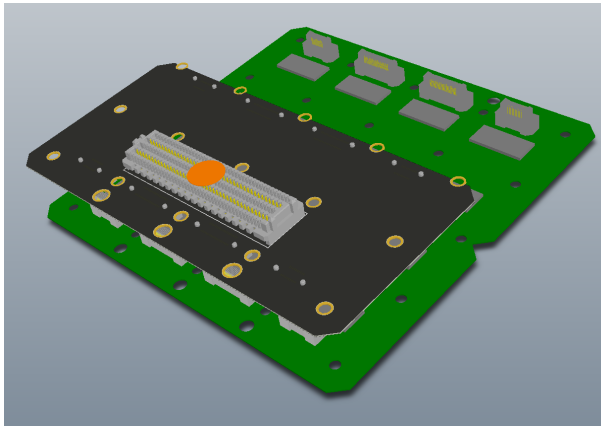
EIC HRPPD Xilinx UltraScale FPGA board proposal (Uni Debrecen)

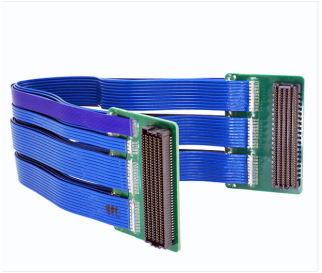
-> flex interface with an FMC connector

-> Samtec ERF5 connectors + a mezzanine

pfRICH beam test: require either five (or ten?) KCU105 boards or gigabit ethernet connectivity

HGCROC3 backplane: KCUs for debugging only?





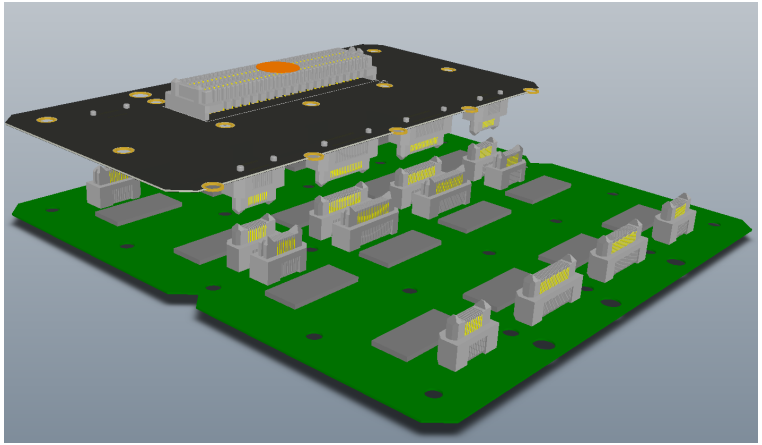
HDR-169468-xx VITA 57.1 FMC Samtec HDR Cable Assembly (HPC) Female to (HPC) Male (HDR02)

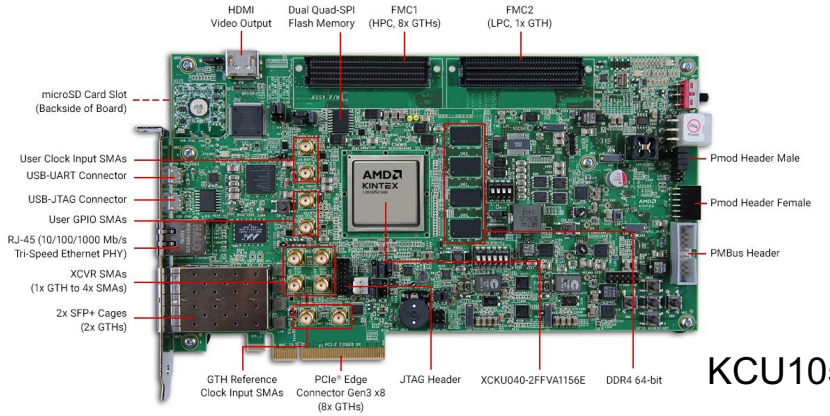
From: £82.17

- VITA 57.1 FMC standard
- Mezzanine to carrier side assembly
- High data rate HPC to HPC cable
- Connectors opposite sides

Data sheet | Technical Specification | Related Products | Product Configurator

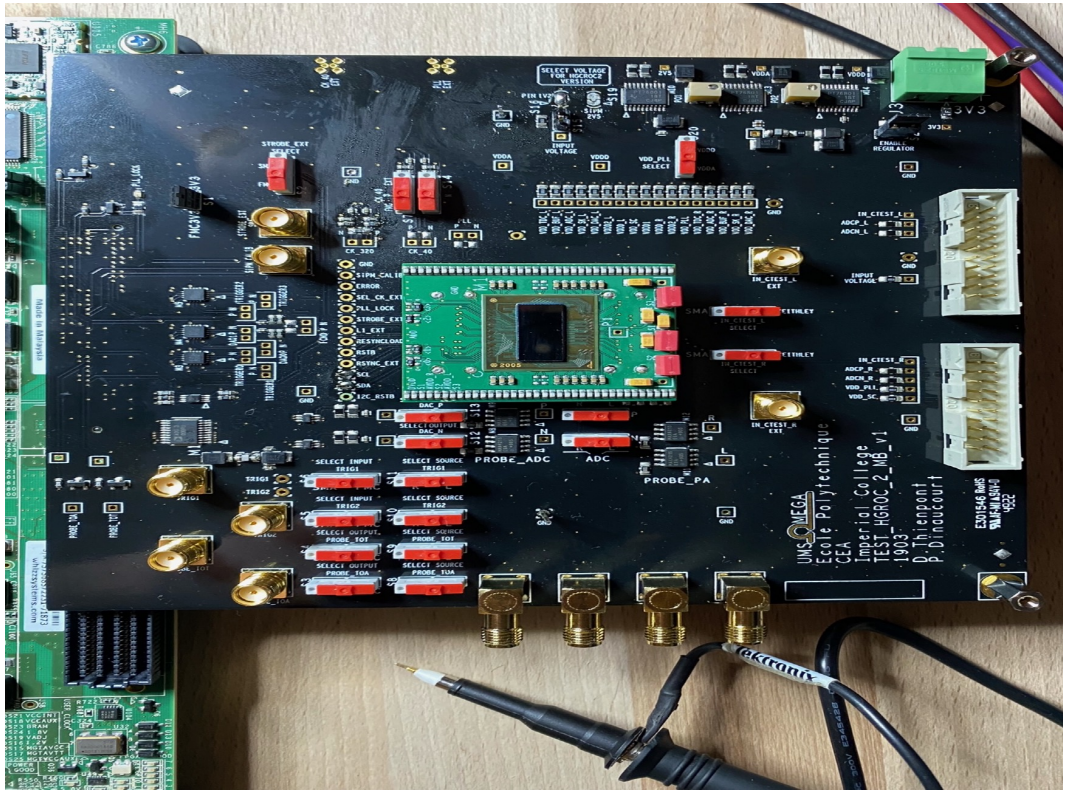
Part No.	Stock Qty	Price Breaks				Qty	
HDR-169468-01 3D CAD 300mm HPC Fem to Male Opp Side	3 in stock	1+: £133.43	10+: £129.72	25+: £122.89	View all prices	1	Buy
HDR-169468-02 3D CAD 550mm HPC Fem-Male Opp Side	Standard delivery 15 - 17 working days *	1+: £176.50	10+: £171.60	25+: £162.57	View all prices	1	Buy





KCU105

HGCROC3 “development kit”



FPGA board, carrier board, mezzanine board with ASIC @ Oak Ridge

- Going to reproduce this setup at BNL by August 2023
  - KCU105 kit provided by John Kuczewski (BNL)
  - Carrier board by Norbert Novitzky (Oak Ridge)
  - Mezzanine board with an ASIC by Damien Thienpont (OMEGA)
- Should suffice to develop a DAQ driver for RCDAQ (in a configuration with KCU105’s)
- (Driver development in a gigabit ethernet configuration is a different story)

Discussion

-> So, what is our planning strategy for 2023/2024 and what are the fallback options?