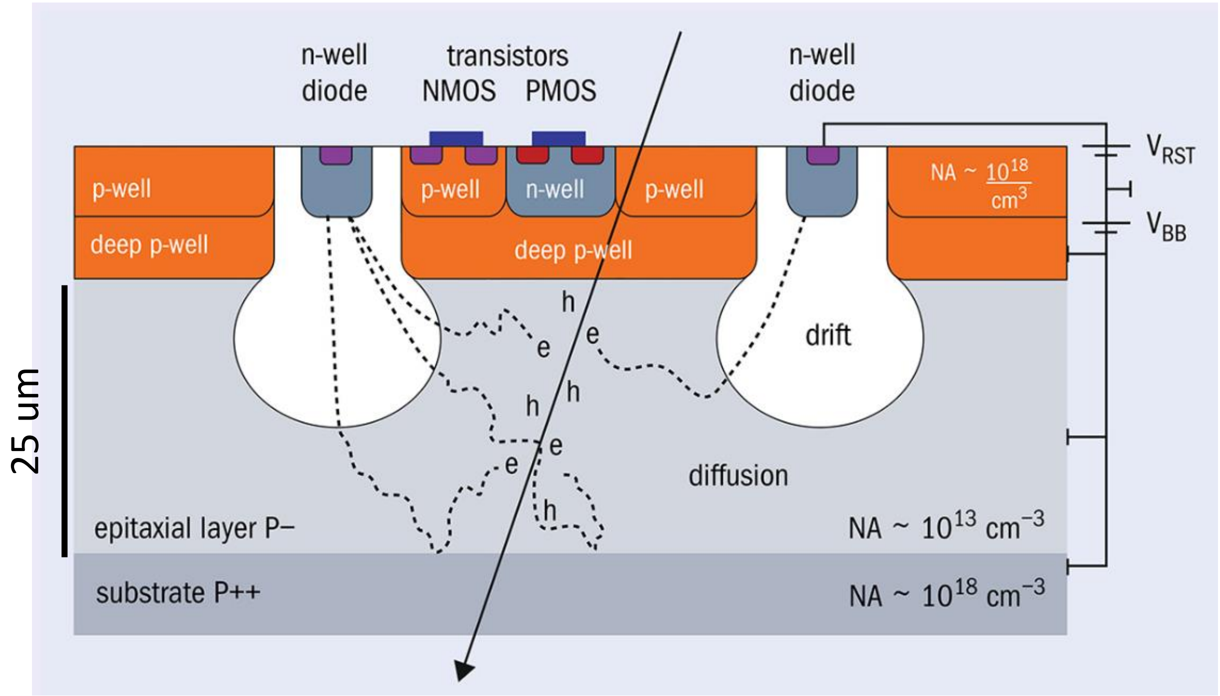
Overview of Digital Pixel Test Structure (DPTS) studies at LBNL

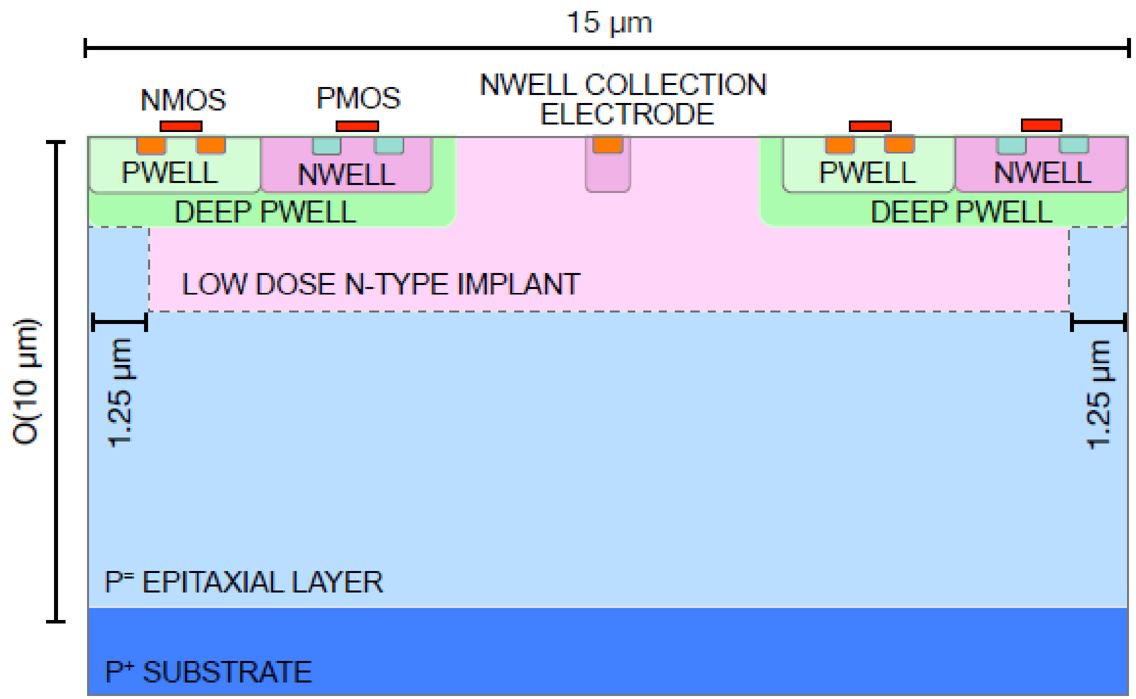
Barak Schmookler

DPTS chip

ALPIDE Chip



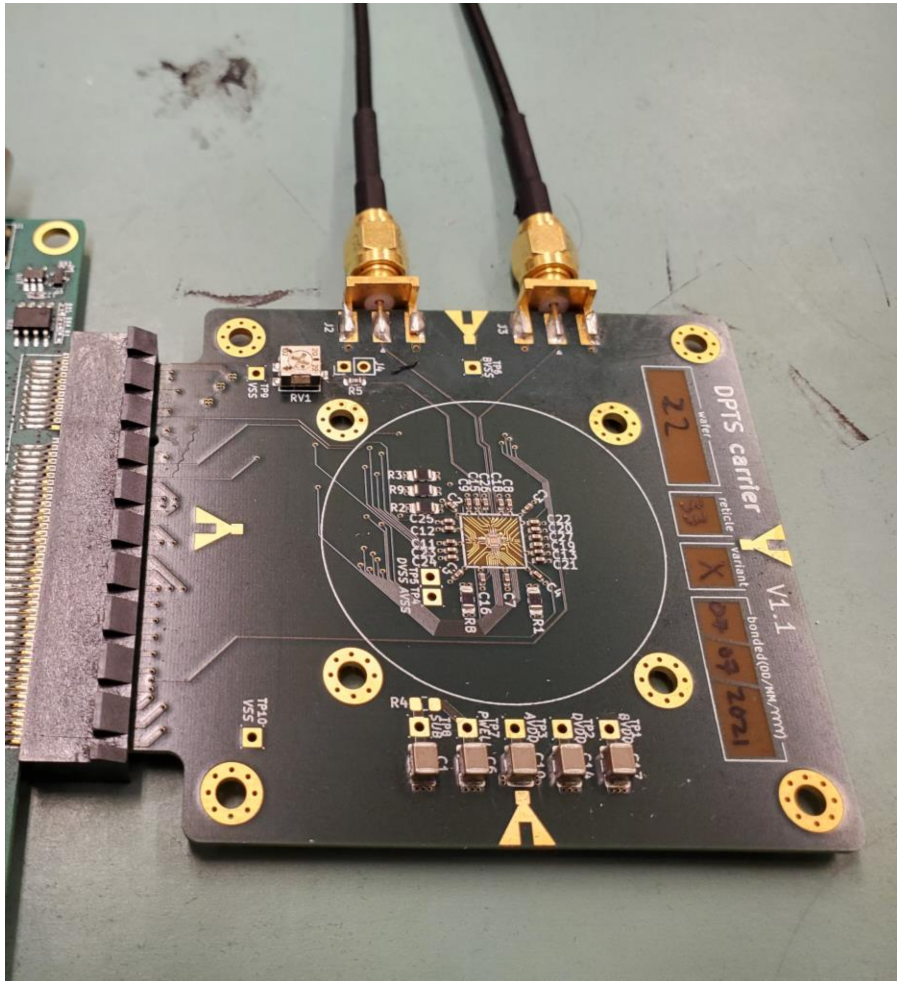
DPTS Chip



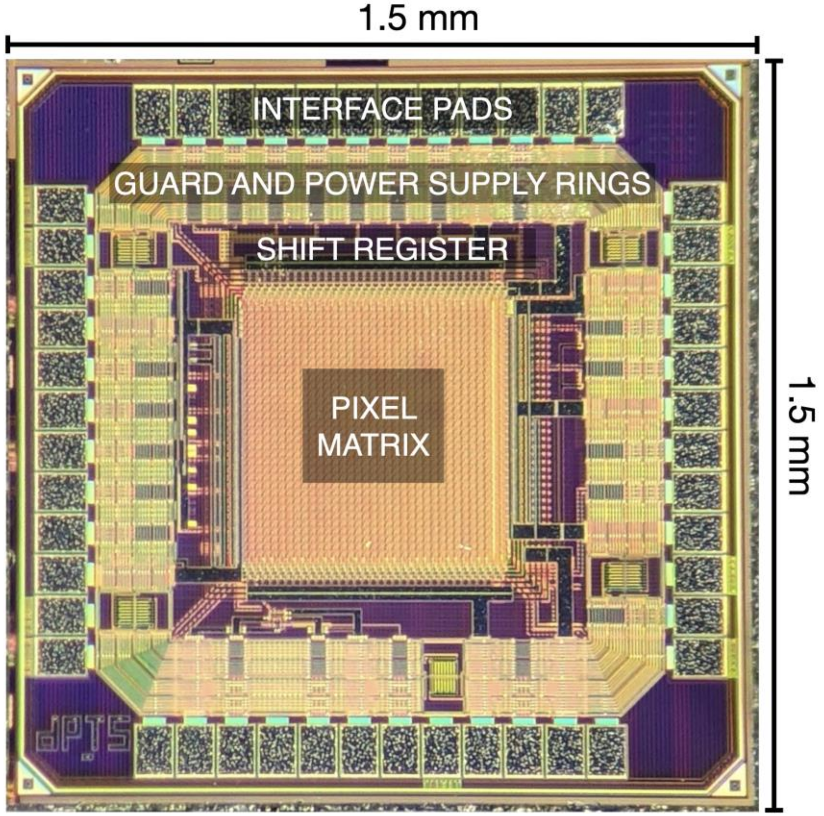
- The most complex prototype MAPS produced in the first submission of the Tower Partners Semiconduction Company 65nm technology process.
- Junction displaced into the epitaxial layer to deplete layer over the full pixel width.

DPTS chip

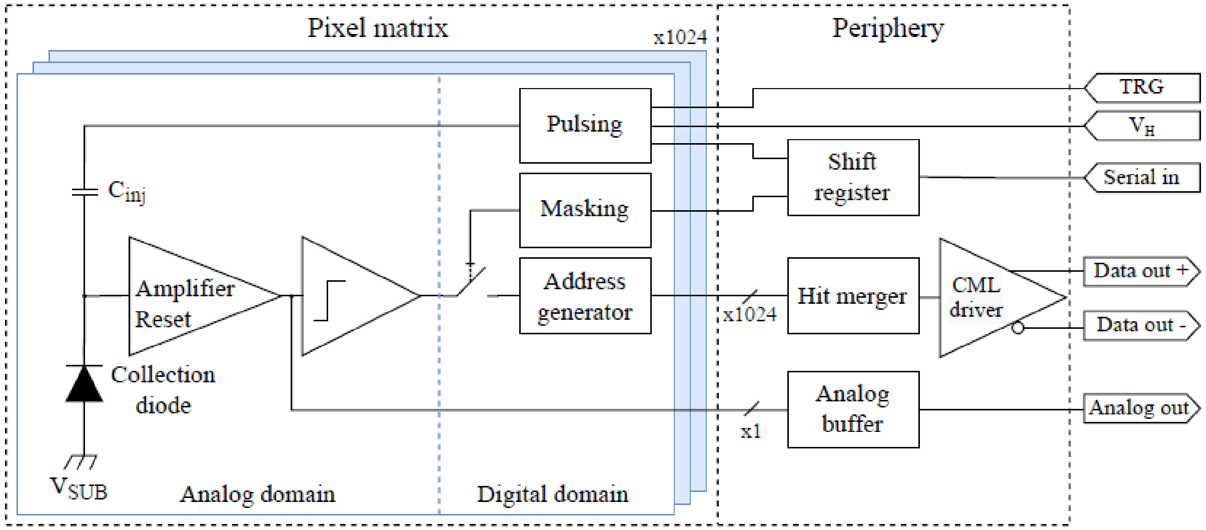
Chip on carrier card

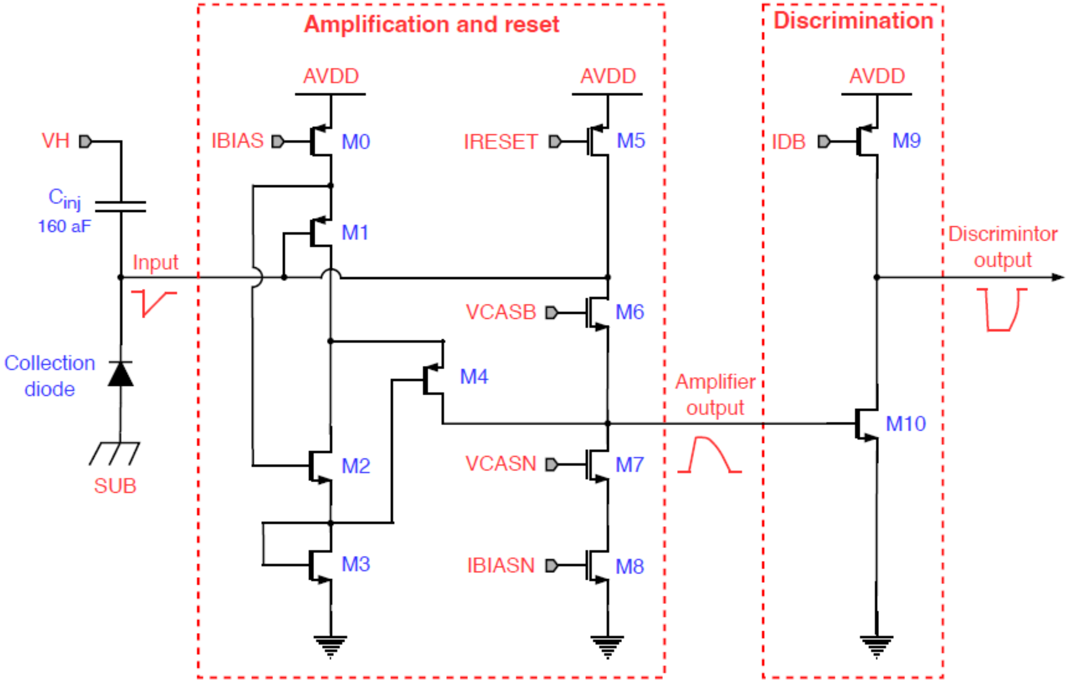


Consists of 32x32 pixel array – 1024 pixels in total



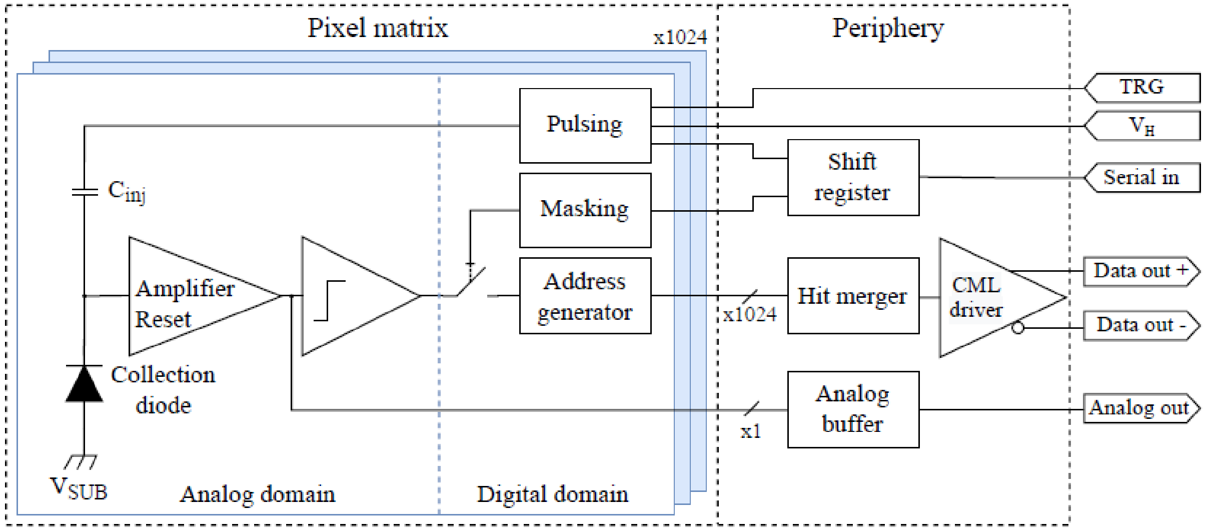
DPTS chip

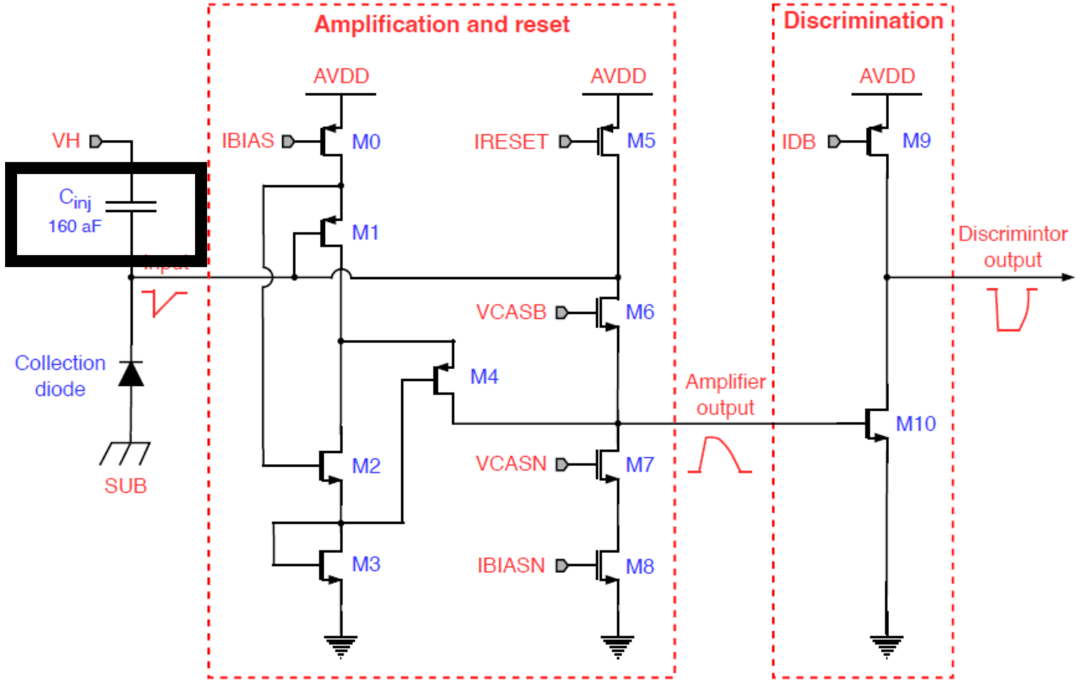




- The DPTS chip is controlled by a set of external reference currents and voltages.
- It is read out via a current mode logic (CML) output.
- The in-pixel front end amplifies, shapes, and discriminates the signal from the collection diode.
- A test circuitry can inject charge into the collection electrode.

DPTS chip





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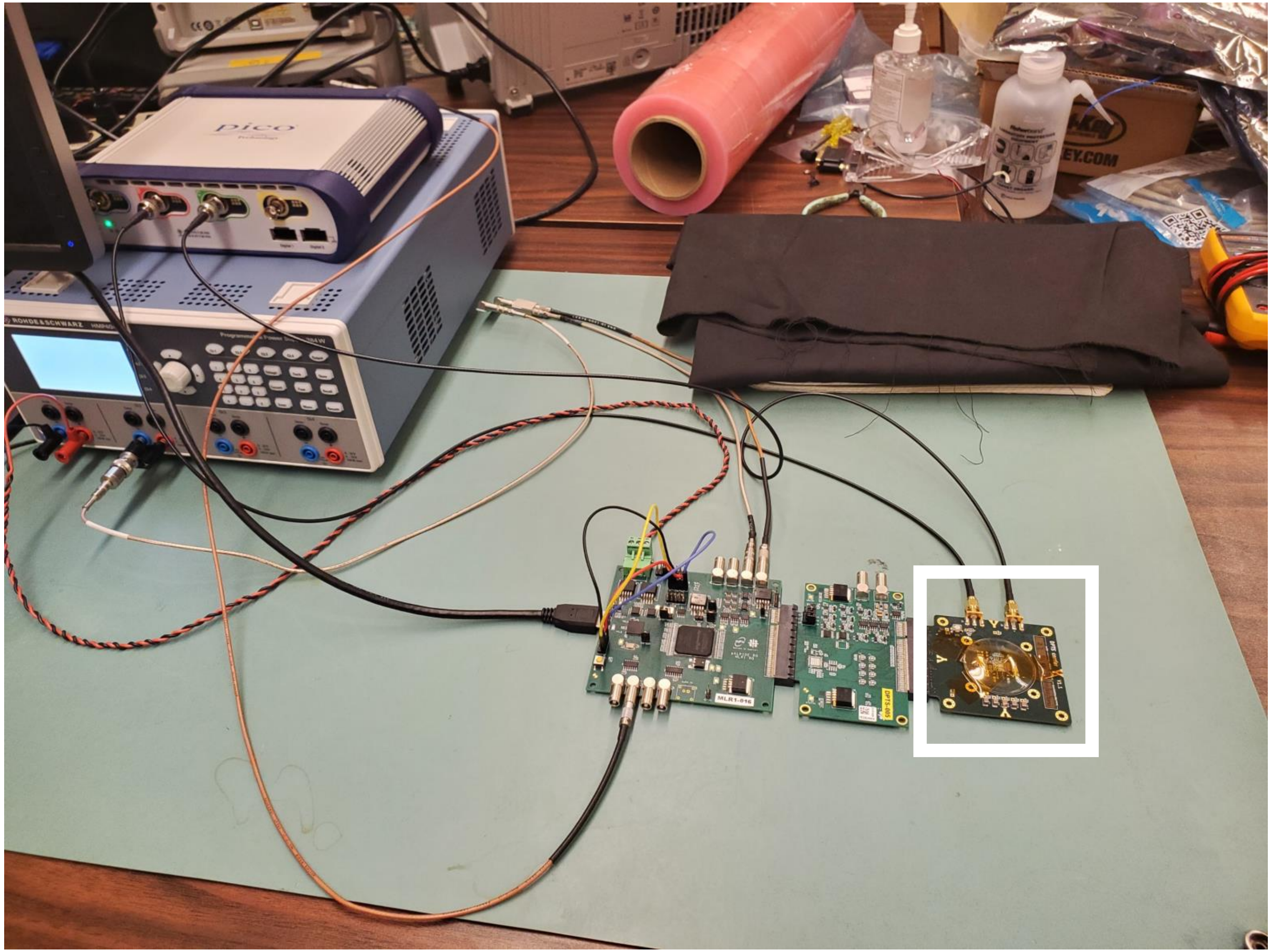
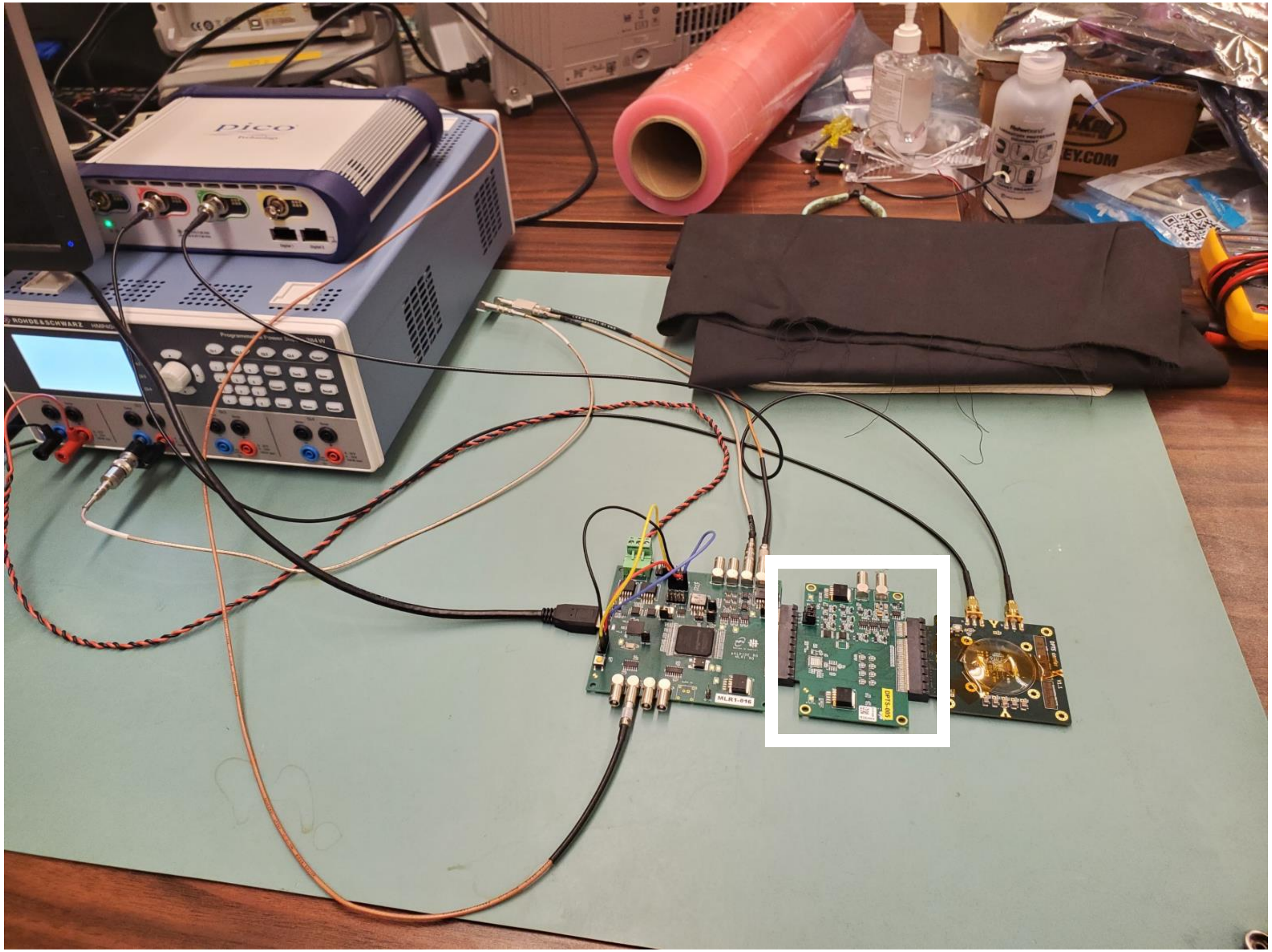
For 160 aF C_{inj}, we have V_H (mV) = Q_{inj} (e^-).

LBNL bench test setup



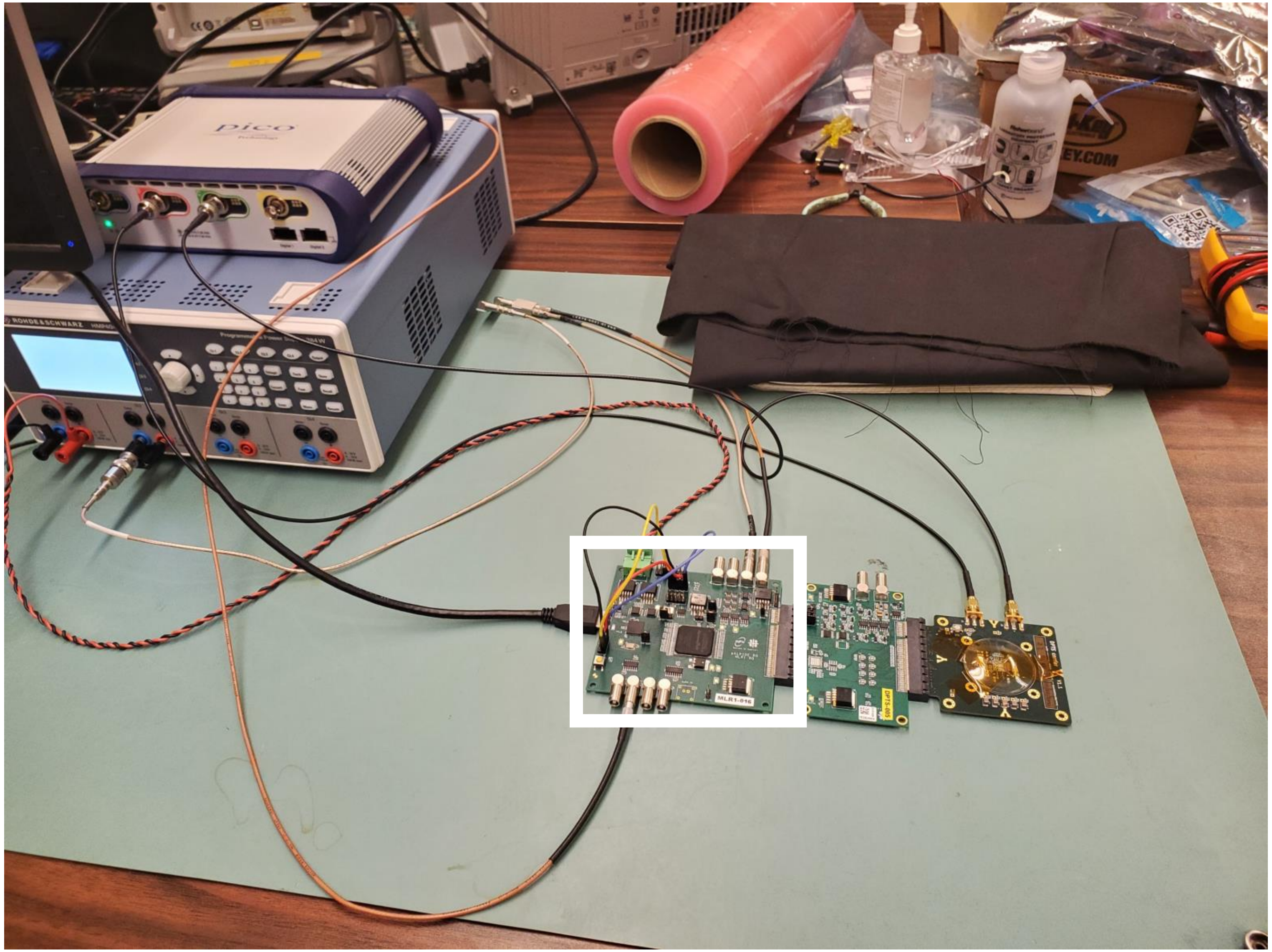
1. DPTS chip and carrier card

LBNL bench test setup



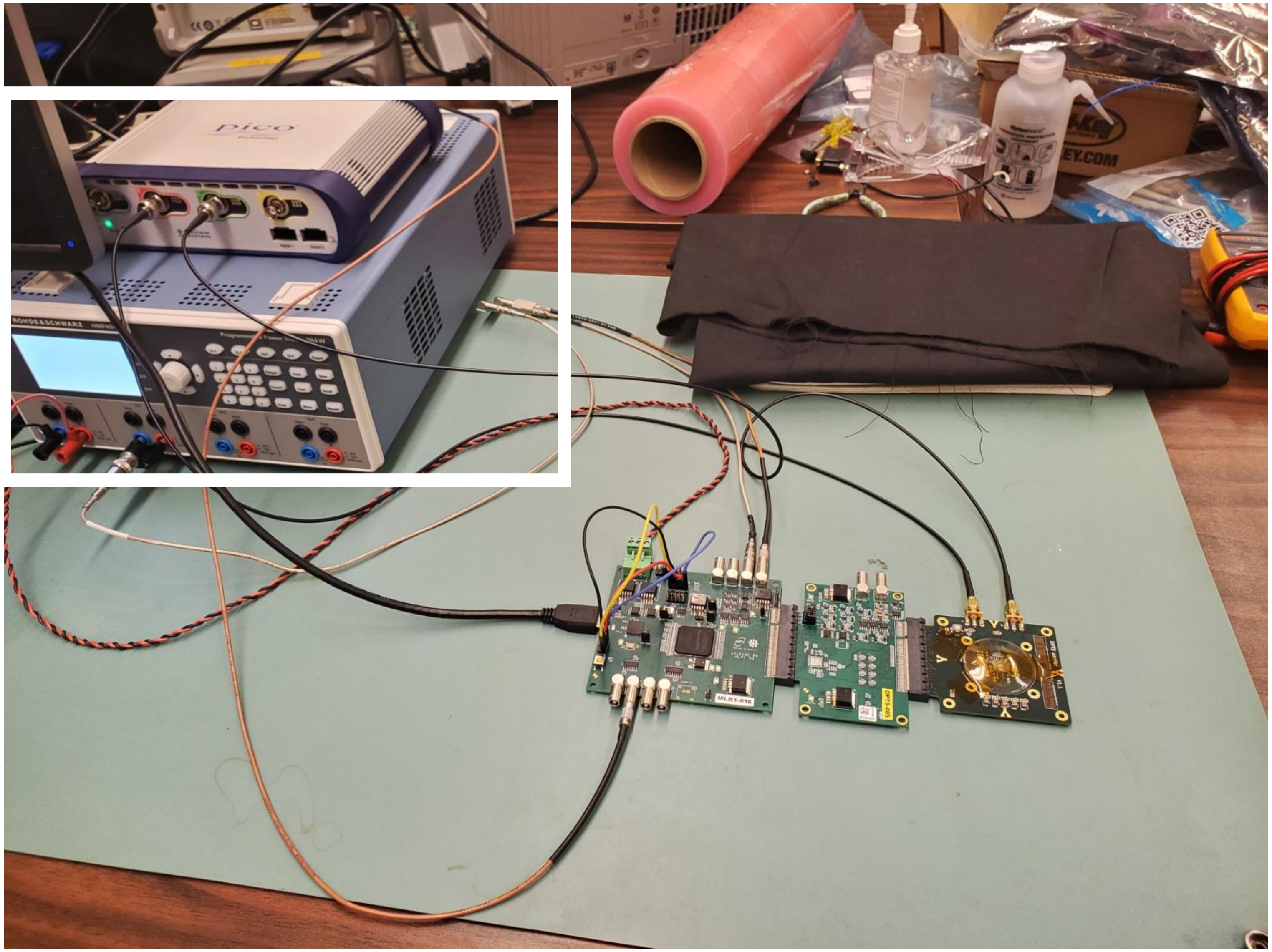
1. DPTS chip and carrier card
2. Proximity board

LBNL bench test setup



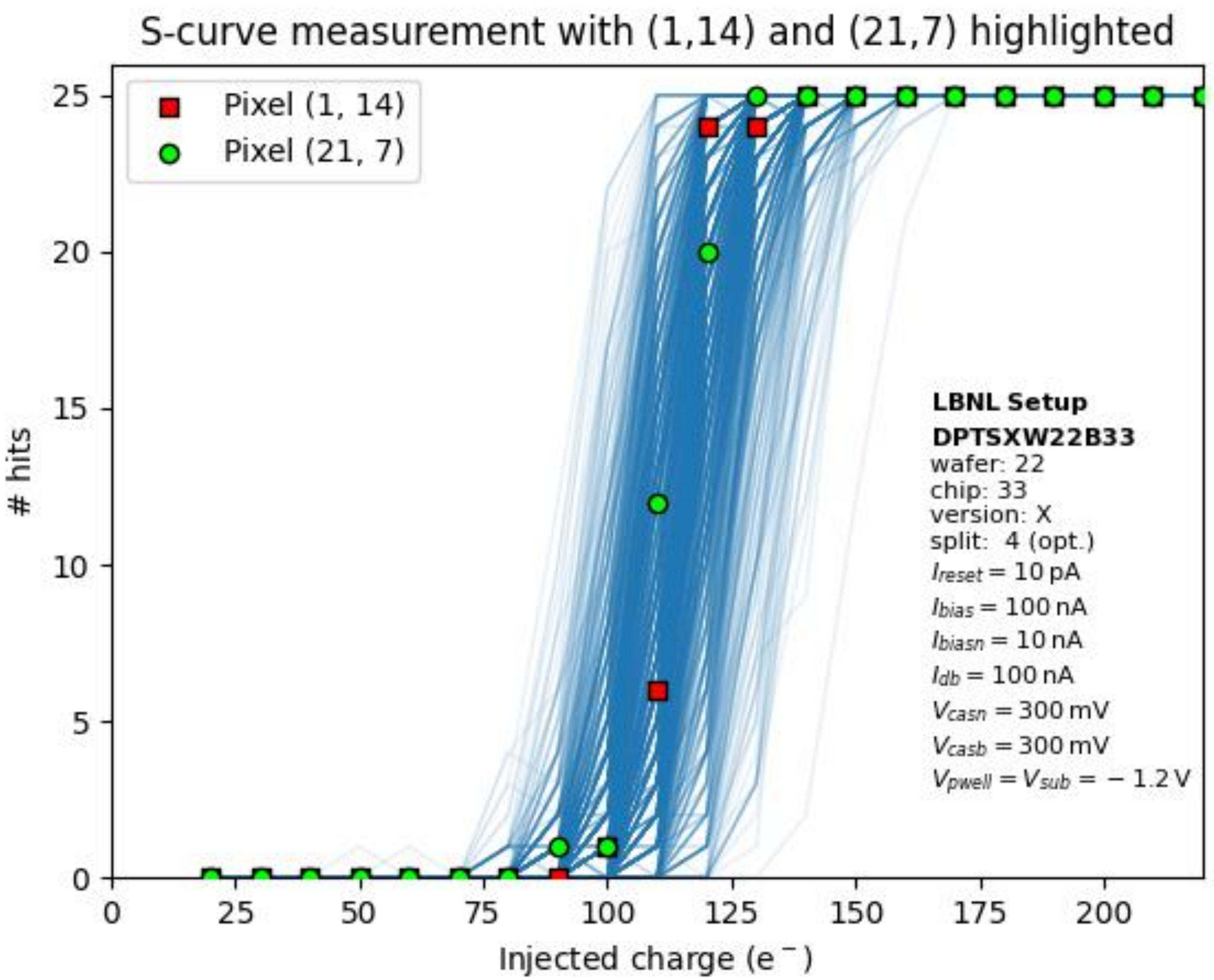
1. DPTS chip and carrier card
2. Proximity board
3. MLR1 DAQ board

LBNL bench test setup

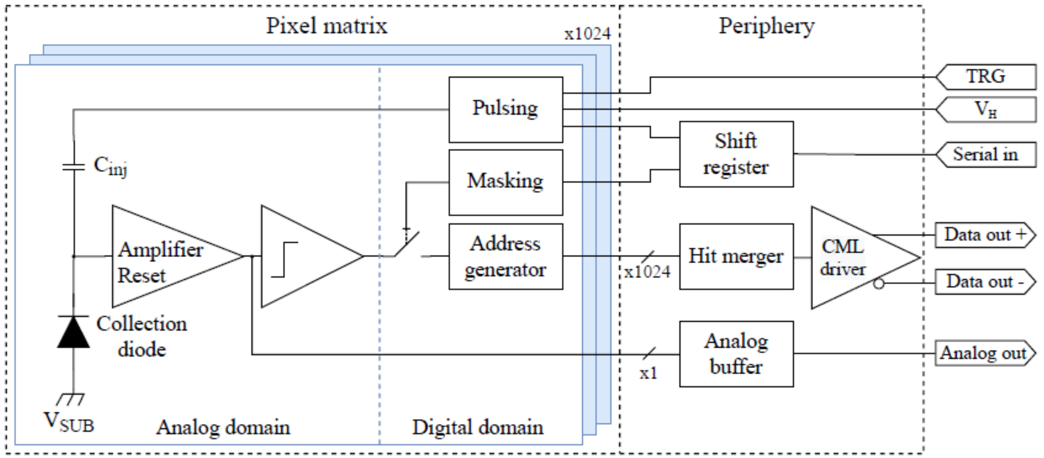


1. DPTS chip and carrier card
2. Proximity board
3. MLR1 DAQ board
4. Power supply and digital oscilloscope

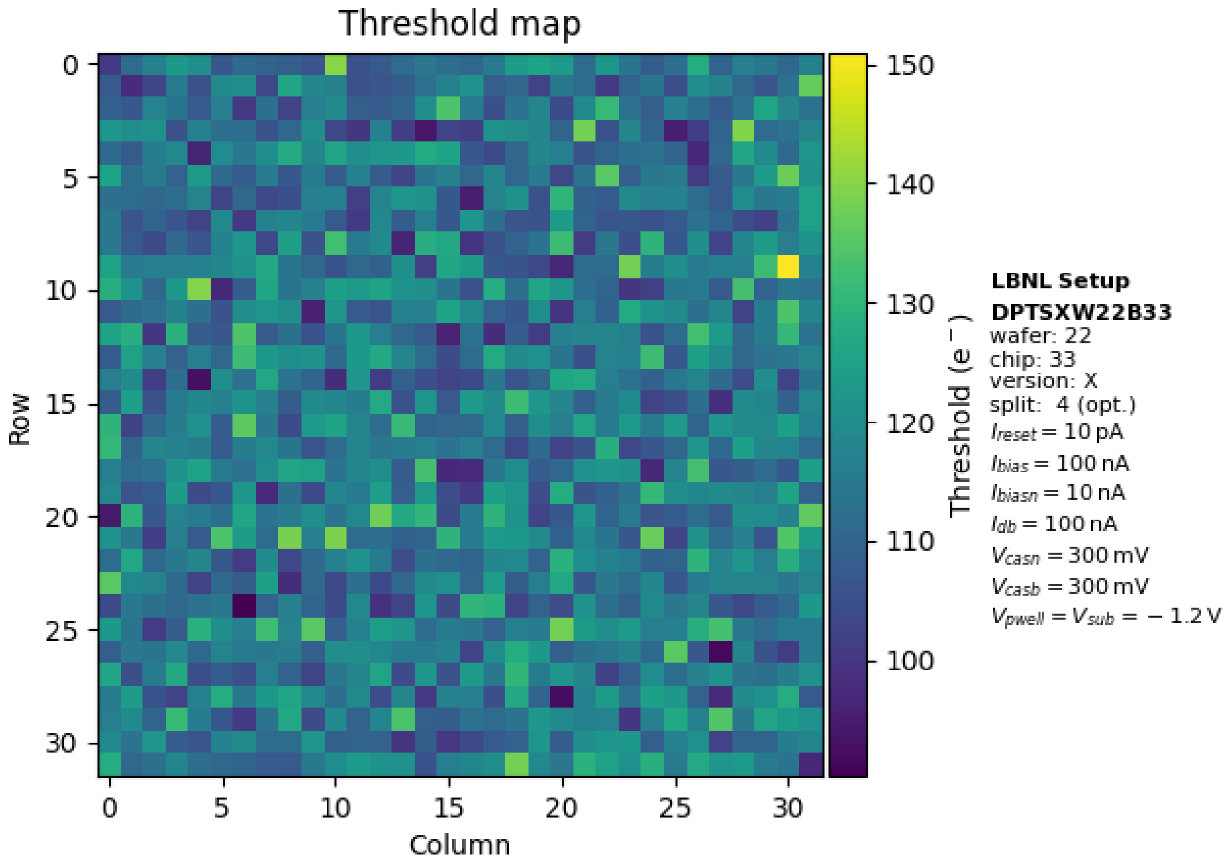
Threshold scan

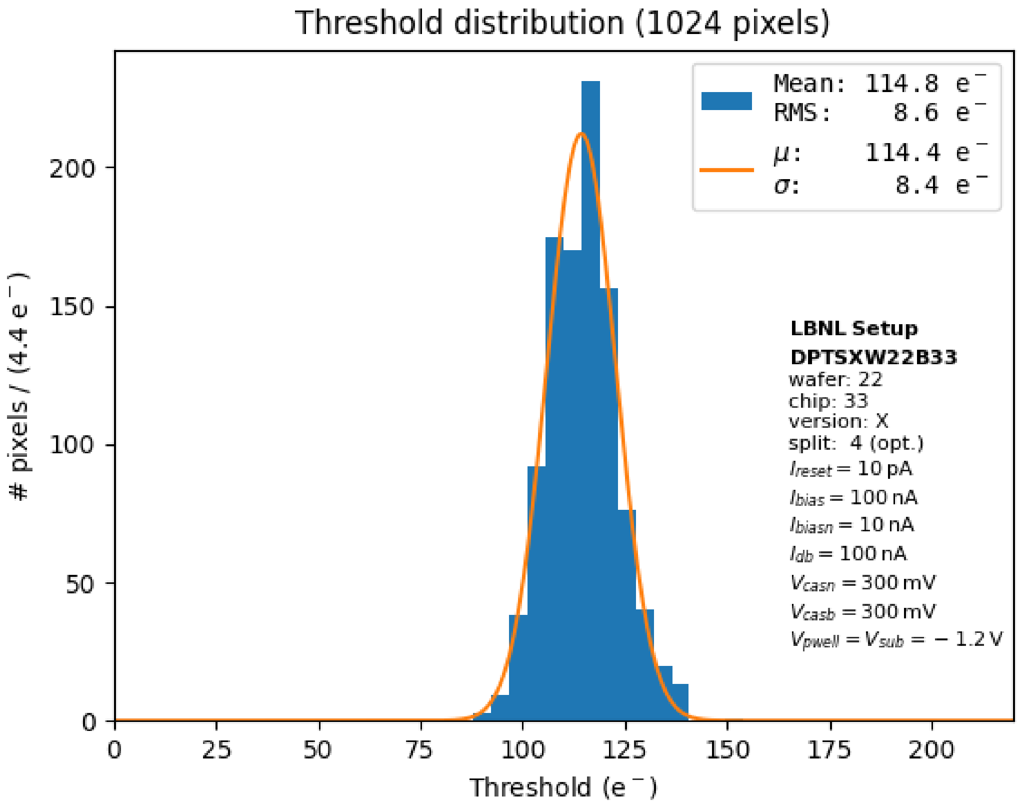


At a given V_H (i.e. injected charge), each pixel is pulsed 25 times and the number of hits is recorded. A hit requires two pulses to be captured by the scope – indicating the assertion and de-assertion of the discriminator pulse.



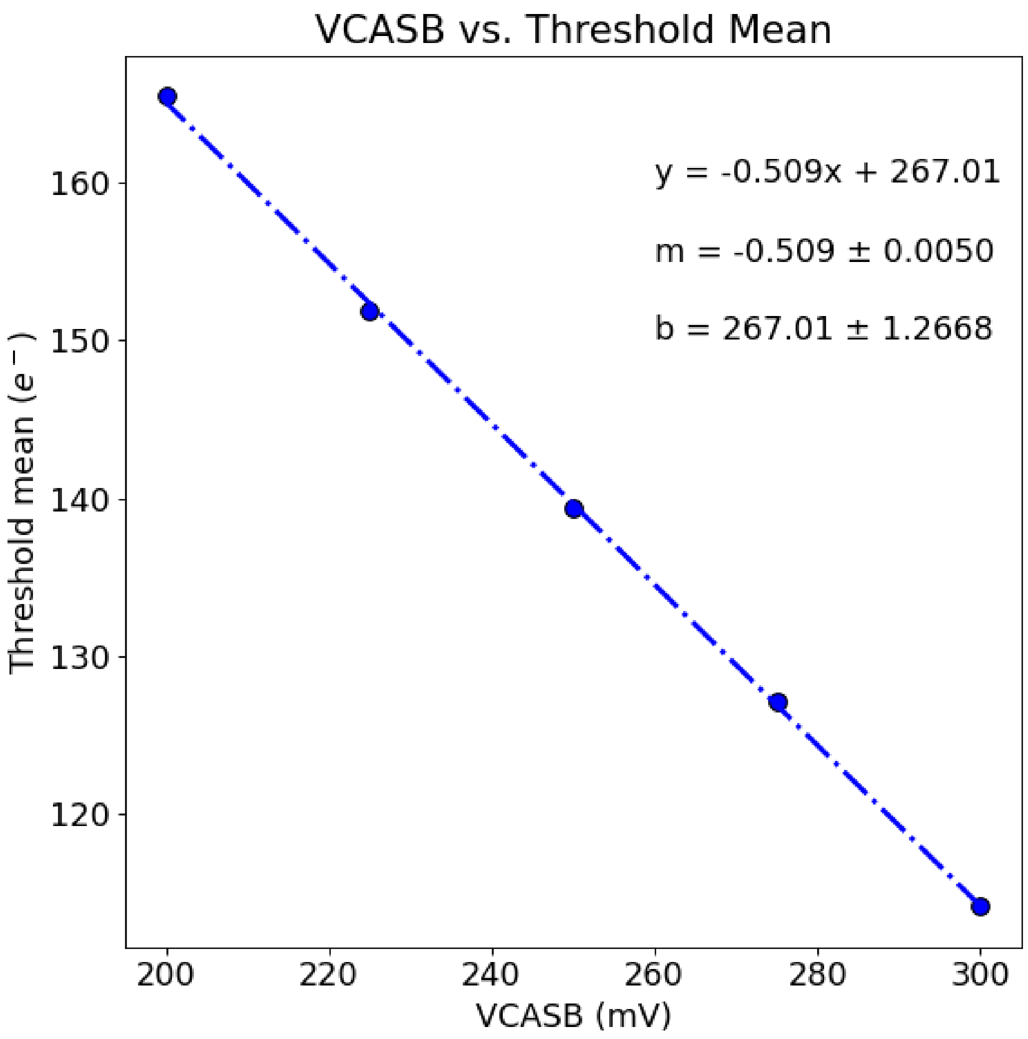
Threshold scan



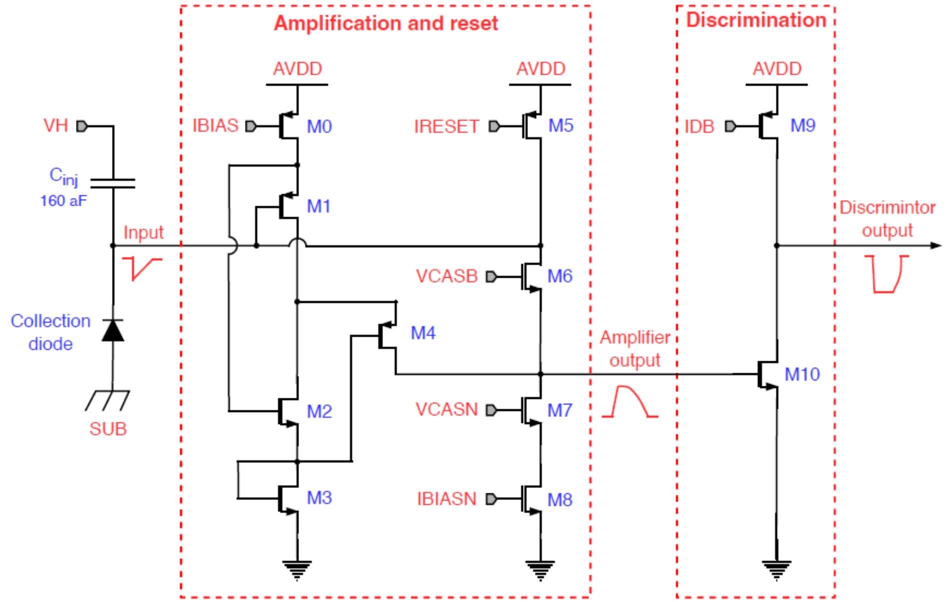


The threshold and noise can be determined from the S-Curve.

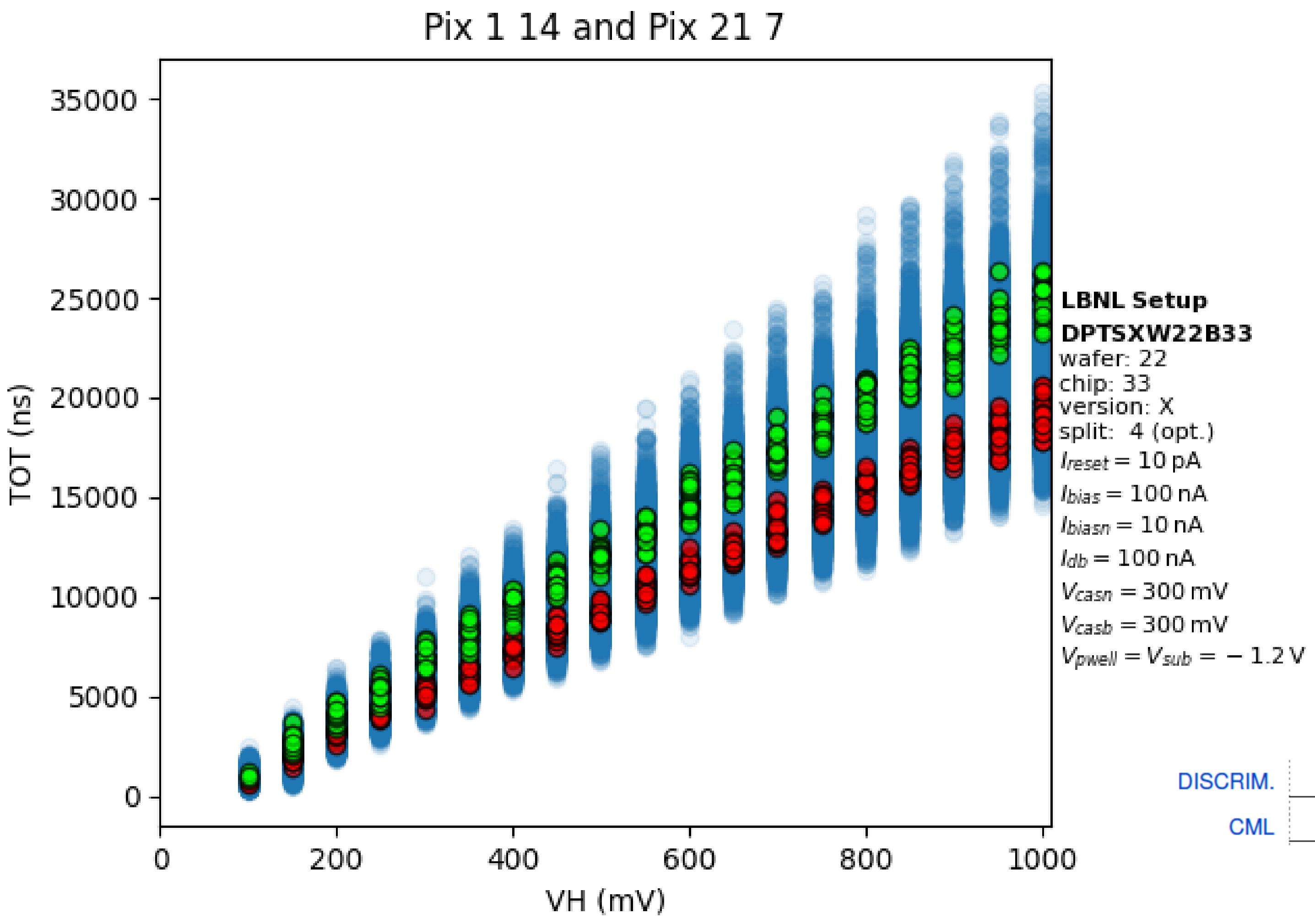
Threshold scan



We can control the threshold by adjusting the VCASB voltage.

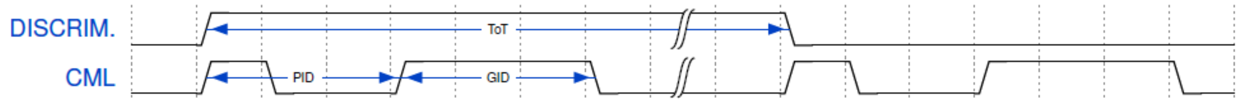


Time-over-threshold (ToT)

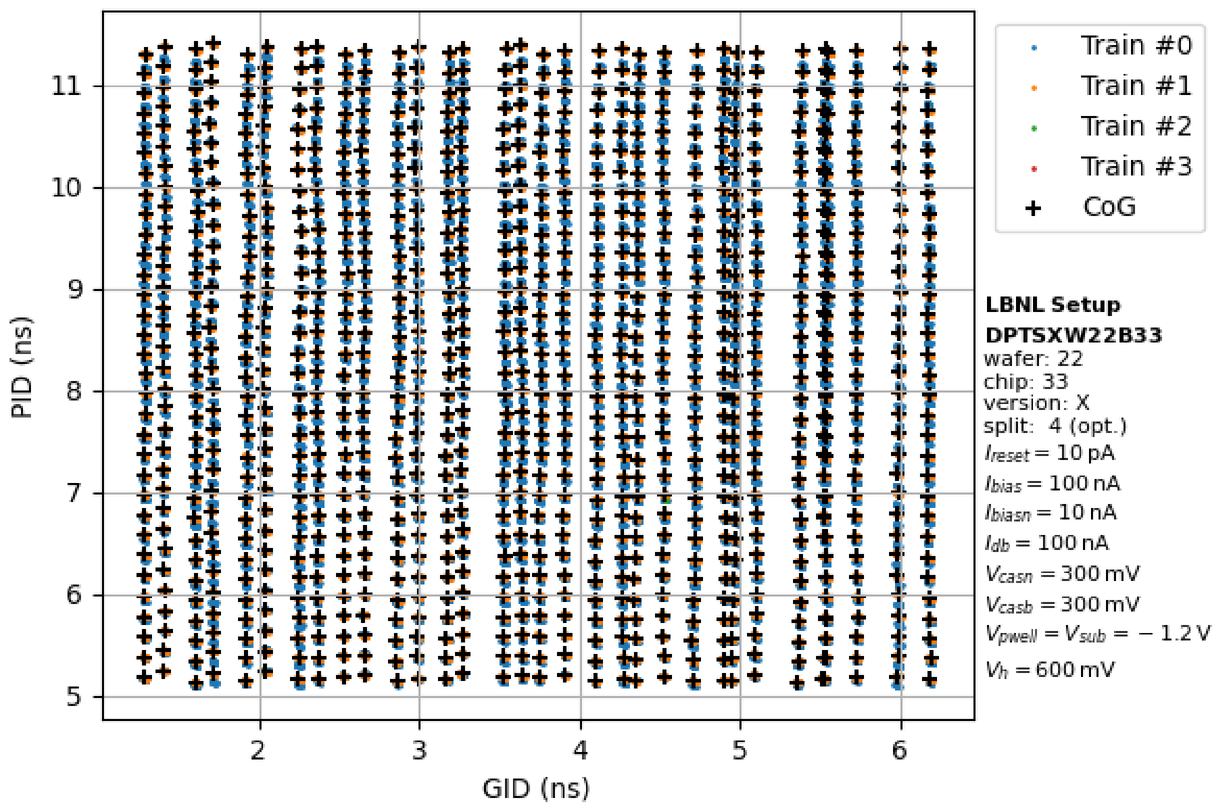


The ToT increases linearly with the total collected (injected) charge.

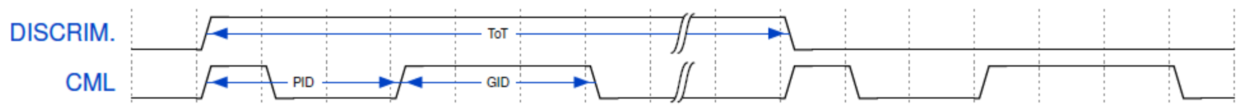
We observe a large pixel-to-pixel variation, which we hope to understand. See next talk by Oscar!



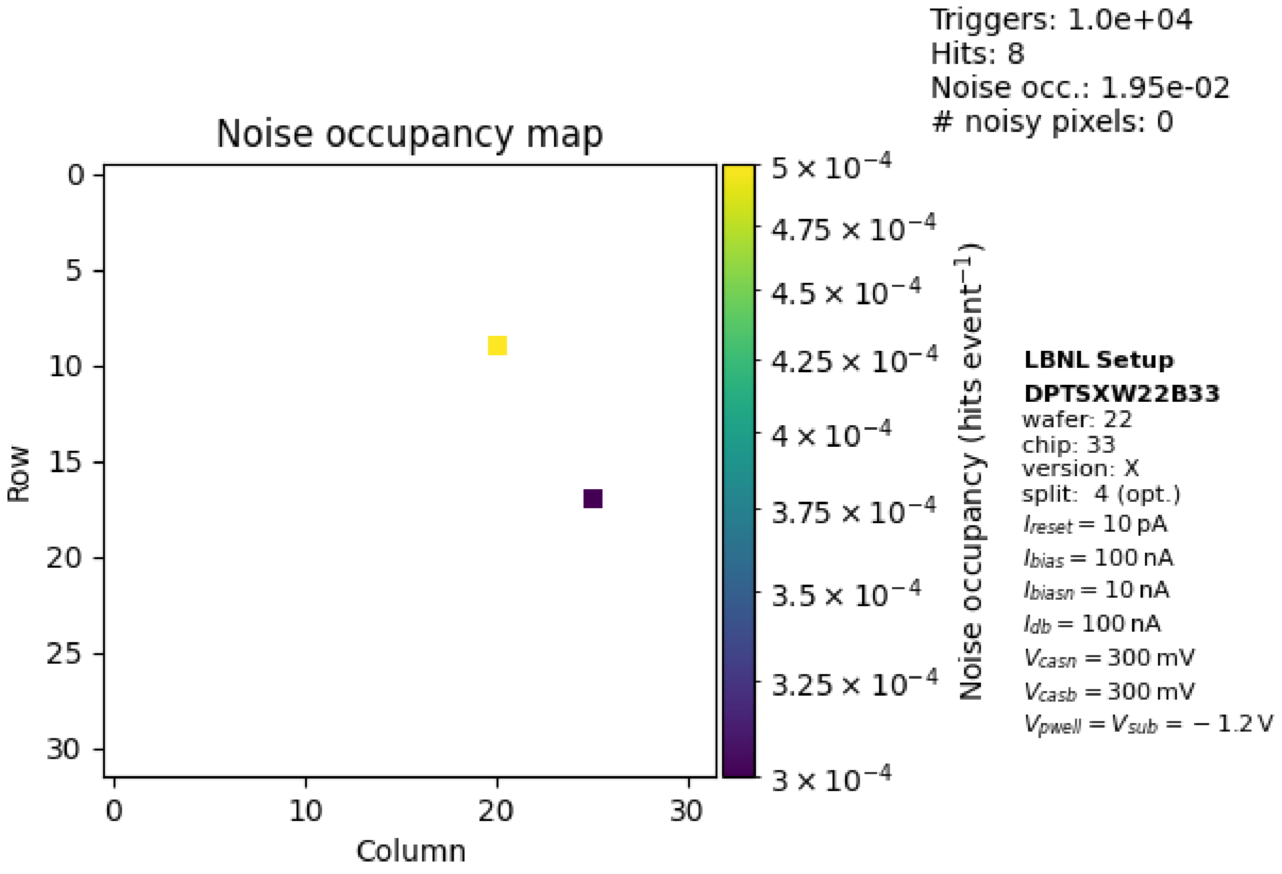
Pixel position decoding



In the case where we don't inject charge, we need a way to decode the pixel that fired based on the CML signal. This is encoded in the PID and GID times.



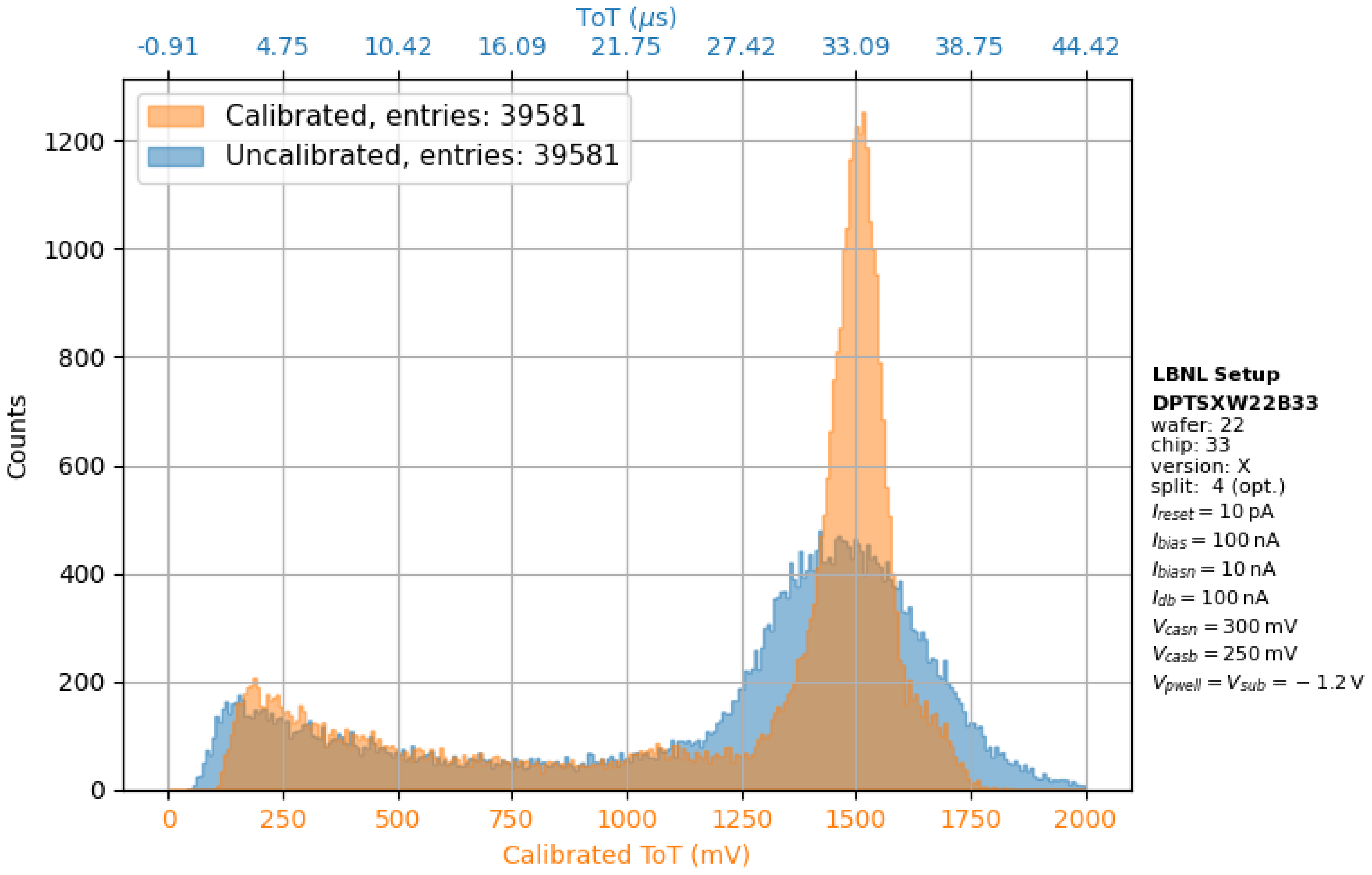
Fake hit rate check



The fake hit rate measures the number of hits seen in the absence of external stimuli. That is, we trigger on a clock and look for any pixel signals.

$$Noise\ Occ. = \frac{Hits}{(Triggers \times Pixels \times scope\ capture\ time)} = \frac{8}{(10{,}000 \times 1024 \times 40\ us)} = 0.0195\ per\ pixel\ per\ s$$

^{55}Fe source data



Collected 100k triggers with a ^{55}Fe source. After requiring events with a single pixel and applying some other cuts, about 40k events remain.

The main peak should be the K-alpha X-ray at 5.9 keV. Since it takes 3.6 eV to create an electron-hole pair in silicon, we would expect this peak to be at 1640 electrons. However, we see the peak at ~1510 electrons. Why do we see this shift?

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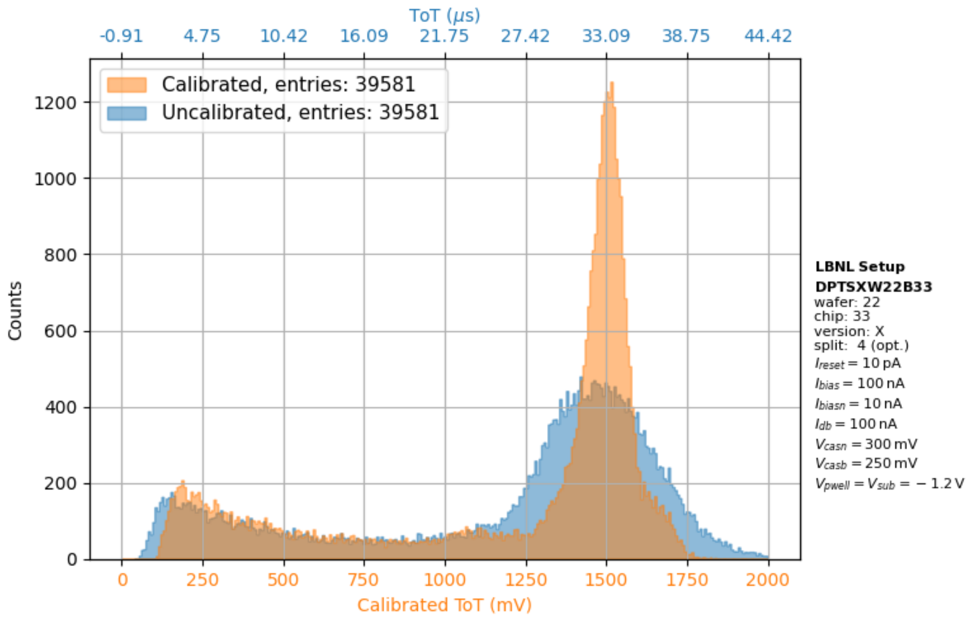

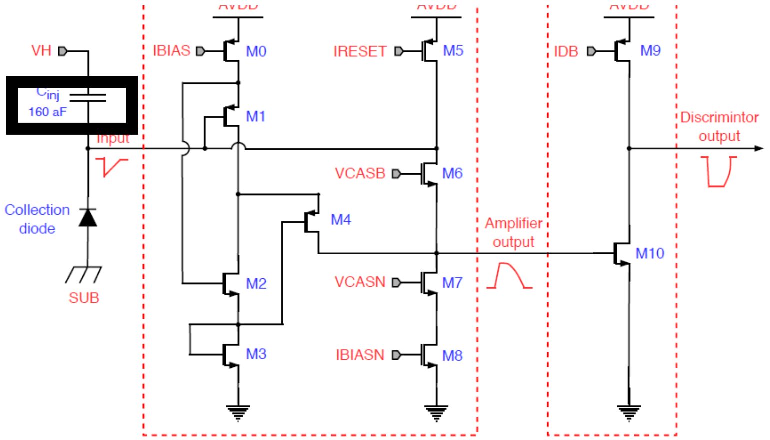

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The ToT calibration is based on the injected charge (set by the voltage V_H). The C_{inj} capacitance can differ from the design value.

Summary

- We have a working bench setup for the DPTS prototype chip.
- We have done some basic studies with injected charge to test the front-end electronics.
- We have also collected data using and ^{55}Fe source.
- We are currently focusing on studying the pixel-to-pixel variation of the ToT. See next talk by Oscar!